Chip-to-Board Micromachining for Interconnect Layer Passive Components

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***Abstract*—Integrated inductors are typically formed either on a chip or embedded in a package or board. In this work, we explore the possibility of forming inductors in the chip-to-board interconnect layer. The solderless technique of copper (Cu) electroplating bonding is used to simultaneously form inductor structures as well as chip-to-board interconnect. The use of the gap between the chip and substrate for inductors not only increases integration density, but also allows large magnetic cross-sectional areas to be achieved. To demonstrate the technology, a plating-through-mold method has been used in the establishment of tall interconnect or solenoid inductors. For demonstration of the electroplating bonded micro solenoid structures, three- and seven-turn (500 μm in height) inductors have been realized with measured inductances of 3.6 and 10.4 nH, and Q-factors of 71 and 55, respectively. As an alternative approach, a polymer-core-conductor method in which polymer posts coated with metal are electroplating bonded, has been developed. This approach reduces processing time in the fabrication of the tall metal structures. For the polymer core RF structures, three-, five-, seven-, and 10-turn inductors have been fabricated. These inductors have inductances of 4.2, 7.0, 9.6, and 13.6 nH, and Q-factors of 72, 64, 56, and 61, respectively.**

***Index Terms*—Chip-to-board interconnect layer, electroplating bonding technology, high frequency structure simulator (HFSS), polymer core method, solenoid inductor.**

I. Introduction

INTEREST in passive components for wireless hand held devices, such as cellular phones, PDAs, and so on, has led to much work aimed at improving performance, miniaturization, and cost effectiveness of these devices. Specifically, incorporation of inductors has been a key issue due to their large size, 3-D configuration (and associated fabrication complexity), and packaging compatibility, including electrical performance and mechanical reliability [1]–[4].

Several approaches have been taken to incorporate inductors into ultracompact systems. Using the hybrid mounting method, chips and inductors are individually packaged and mounted in a hybrid fashion on a printed wiring board (PWB) [5]. This discrete component packaging method limits the miniaturization of the system board size; in addition, increased parasitic effects caused by extended interconnection lines may occur. To achieve higher packaging density and reduced parasitics, passive components have been fabricated based on multichip modules (MCM) and flip-chip packaging. With this MCM approach, inductors have been fabricated in MCM-D (deposition of thin-film layers), MCM-L (lamination metal layer patterns within a PWB), and MCM-C (fabrication of multilayer structures by co-firing ceramic or glass/ceramic tapes) [6]–[8]. Fully integrated approaches (the on-chip method) involve the fabrication of inductors directly on the silicon substrate containing the active circuitry [9]–[11]. These approaches have the attractive feature that lead parasitics are minimized, facilitating high frequency operation.

An alternative to these methods is to form passive elements in the interconnect layer between the chip and the board. The conceptual approach of forming passive elements in general, and inductive components in particular, in the interconnect layer is driven by several factors. First, this region currently represents unexploited "real estate" (actually volume) that does not conflict with the valuable allocation of real estate on the surface of the chip or board. Second, since magnetic elements traditionally scale with volume as opposed to surface area, the utilization of this relatively large volume (while at the same time minimizing parasitics associated with discrete leads) for high-performance elements is very attractive. Third, fabrication of the passive elements in this region exploits the physical and electrical separation of this region from the relatively lossy silicon chip and other electrical components, thereby minimizing parasitic mutual inductance and magnetic coupling to the chip resulting in impedance mismatching and eddy current loss.

In this paper, the electroplating bonding technology is briefly reviewed and interconnect layer micro solenoid inductors using the electroplating bonding technology are numerically analyzed, designed, fabricated, and characterized as examples of chip-to-board micromachining. Although inductors are chosen as the test vehicle, other large-magnetic-cross-section applications such as antennas may benefit from this approach as well.

II. Technological Approach: Electroplating Bonding Technology

A variety of approaches can be taken to form passive elements within the interconnect layer. A straightforward approach is to utilize the solder interconnection metal itself for the formation of inductive components as well as for chip-to-board interconnect. However, the increasing environmental concerns and high temperature processing associated with lead-based or lead-free solders, coupled with the relatively high resistivity of solders

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(compared with, e.g., copper), drove the development of the electroplating bonding approach [12]. Similar approaches have been used in the past for transfer bonding of microelectromechanical system (MEMS) metallic structures from one substrate to another [13].

As used here, electroplating bonding is defined as the simultaneous electrical interconnection of multiple input-output leads from chip to substrate by means of electrodeposition. Although solder is commonly used in flip-chip approaches to mass-formation of vertical interconnect, the above-mentioned environmental and processing concerns have stimulated alternative approaches, such as conductive adhesives, although they have relatively high electrical resistivity [14], [15]. An attractive alternative to both solder and conductive adhesives that does not compromise conductivity or mechanical strength is to connect the chip to the substrate by electroplated metal such as electroplated copper, which provides high electrical and thermal conductivity and can be the same material with both upper and lower side bonding electrodes, thereby achieving mechanically robust and electrically improved interconnection. This approach also offers the possibility of creating passive and microelectromechanical structures in the interconnect layer during the bonding process.

Electroplating bonding structures can be formed by three steps. First, the metal structures on each substrate are formed by surface micromachining and conventional microelectronics electroplating processes. Second, the metal structures on a substrate are flipped and aligned. The aligning method can be the same as that of the flip chip process; however, in this fabrication, the alignment is performed manually under a stereoscope with a limited academic equipment situation. Third, the entire system is clamped together, immersed in the Cu electroplating bath, and the tips of the metal structures from each substrate are bonded with electrodeposition upon applied dc current. By controlling the gap between the substrates, this interconnect layer structural bonding approach has potential for high Q-factor passive components such as a solenoid inductor with a large magnetic cross-section. In this case, the magnetic cross section is ultimately the height of the solenoid inductors. The concept of metal plating bonding could be extended to or combined with currently studied Cu interconnect methods in semiconductor industry.

III. Solenoid Inductor Modeling

To evaluate the feasibility of this approach to inductor fabrication, typical rectangular-shaped solenoid inductors achievable by this method have been designed and their electrical characteristics are analyzed by a high frequency structure simulator (HFSS, Ansoft) [16]. The analysis is done in conjunction with analytical models, if available, to develop a range of phenomenological models applicable to the size ranges of inductors achievable using the electroplating bonding method. The HFSS simulation has performed with highly conductive copper structures of 5.8×10^7 [S/m] in conductivity. The inductor structures used in simulation, analyses and realization are designed with several different post heights (a_1) in the range of 250μm $\sim$ 600 μm, a fixed core width a of 550 μm, a fixed conductor width w of 50 μm, a thickness of 20 μm, and a pitch of

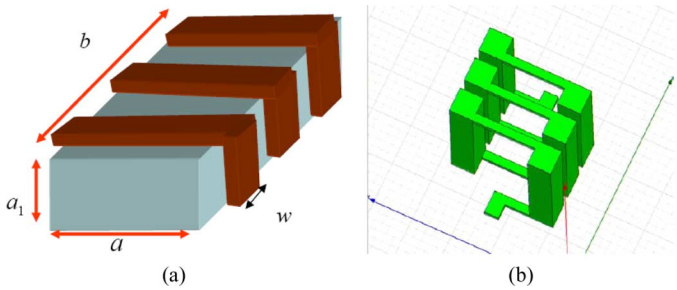

Fig. 1. Schematics of designed inductors for (a) Niwa's model (1) and (b) for HFSS.

250 μm as shown in Fig. 1. This range of post heights is determined by consideration of maintaining uniform electroplating bonding on the inner posts, together with constraints on high aspect ratio electroplated structures with plating-through-mold technology.

A. Inductance

An analytical equation for the inductance of a rectangular-shaped inductor has been developed by Niwa [16] and Grover [17] as

$$L = \mu_0 N^2 \left(\frac{a a_1}{b}\right) F \text{ for } a_1 < a \tag{1}$$

where N is the number of coil turns, F is a geometry factor for rectangular inductor, μ_0 is the permeability of air, a and a_1 are the side lengths of the inductor, and b is the core length as shown in Fig. 1(a). The inductances of a rectangular inductor with posts of different height are calculated and compared with the results of HFSS simulation for which the geometry shown in Fig. 1(b) has been used. The simulations are performed with- or without the presence of a PWB substrate with a typical relative permittivity of 4.3 and a loss tangent of 0.02. Fig. 2(a) shows that the inductance predicted by (1) agrees reasonably well with those of the HFSS simulation. Also, the presence of the substrate has little effect on the effective inductance [18].

B. Capacitance and Resonant Frequency

The capacitance associated with the inductor may influence the operating range, resonant frequency, and Q-factor. This capacitance can be subdivided into turn-to-turn capacitance and conductor-to-substrate capacitance. The turn-to-turn capacitance can be calculated by two methods. First, the capacitance equation for a parallel plate capacitor ($C = \varepsilon_o^* \mathrm{A/d}$, where ε_o is the dielectric constant of air, A is the area of the side wall facing the neighboring conductors or posts, and d is the spacing between conductors or posts) [19], [20] is utilized to form an analytical approximation. Second, the turn-to-turn capacitances of the inductors are extracted from simulation by considering the resonant frequency of the inductors modeled in the absence of substrates. In this approach, the capacitance is given by

$$C = \frac{1}{L \times (2 \times \pi \times \text{Resonant frequency})^2}. \tag{2}$$

The inductance and resonant frequency can be determined by S-parameter extraction. Fig. 2(b) shows the comparison of the

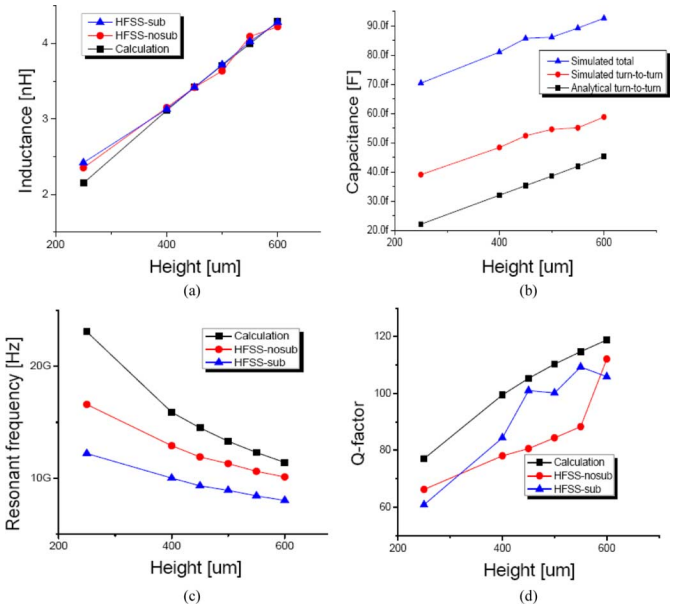

Fig. 2. Comparison of inductor characteristics of theoretical calculation, HFSS without a substrate, and HFSS with a substrate: (a) inductance, (b) capacitance, (c) resonant frequency, and (d) Q-factor.

capacitances. The analytical expression for turn-to-turn capacitance appears to be less than the simulation results by approximately a factor of 2. In the theoretical calculation, it was considered that the capacitance is due only to adjacent conductors. However, in the real device, additional capacitance contribution from non-adjacent conductors and fringing field may exist for the turn-to-turn capacitance. The conductor-to-substrate capacitance can also be estimated by comparison of the HFSS simulations for a non-substrate-influenced inductor and a substrate-influenced inductor. The conductor-to-substrate capacitance of the inductor on the substrate is approximately 30 fF as shown in Fig. 2(b). The resonant frequency of the inductor predicted by the combination of the inductance of (1) and the analytical parallel plate turn-to-turn capacitance approximation compared with HFSS results is shown in Fig. 2(c).

C. Resistance and Q-Factor

Many methods have been used to determine inductor resistance by Dowell [21], Perry [22], Bennet [23], and Ferreira [24]. In particular, Ferreira has utilized rectangular conductor structures for the calculation, which are more suitable for this microfabrication. The resistances of the inductors at a specific frequency (1.5 GHz) are calculated with various inductor heights. The resistance equation of Ferreira is

$$R_{\rm ac} = R_{dc}\frac{\xi(\eta)}{2}\left[\frac{\sinh\xi(\eta)+\sin\xi(\eta)}{\cosh\xi(\eta)-\cos\xi(\eta)} + \eta^2(2m-1)\frac{\sinh\xi(\eta)-\sin\xi(\eta)}{\cosh\xi(\eta)+\cos\xi(\eta)}\right] \quad (3)$$

where $\xi(\eta)$ is the thickness of the conductor line normalized with respect to the skin depth $\delta(\eta) = 1/\sqrt{\pi\mu\sigma f\eta}$, R_{dc} is the dc winding resistance, m is the number of winding layers in the inductor, η is the porosity factor [$= Nw/b$, where N is the number of inductor turns, w is the width of the conductor and b is the air core length as shown in Fig. 1(a)] [25]. The equation is divided into two dominant effects of ac resistance in the inductor: the skin depth effect [the first term of (3)] and the proximity effect [the second term of (3)]. In this paper, to achieve a more accurate result, we take into account the proximity effect with two different porosity factors (0.2 on upper and bottom conductors, and 0.75 on posts).

Once the resistance has been determined, the Q-factor can be predicted. The air-core inductor usually has been described by an equivalent circuit which has an ideal inductor L in series with a resistor R and in parallel with a capacitance C. The Q-factor for the equivalent circuit is shown as

$$Q = \frac{\omega L\left(1-\omega^2 LC - \frac{CR^2}{L}\right)}{R_{\rm ac}}. \quad (4)$$

Fig. 2(d) shows a comparison of Q-factors which are obtained by HFSS simulation and numerical calculation from (4). The Q-factors of the inductors on the PWB substrate are also obtained. The inductor height corresponding to a maximum Q-factor is 550 μm, i.e., the height which forms a square shape of the solenoid core cross section. The HFSS result of with-substrate structure shows that the Q-factor of structures taller than 550 μm is gradually degraded.

D. Figure of Merit

An advantage of the electroplating bonded inductor is that the inductor can be established with a large magnetic core cross-section since metal posts on both substrates are united to form a double-height inductor winding. For example, 500-μm tall micromachined Cu posts on both silicon and PWB substrates will yield a 1000-μm tall Cu solenoid inductor winding after electroplating bonding. Although achievable using other means, such tall inductors would otherwise require exacting processing conditions.

The simulated inductor designs are remodeled to take into account actual measurement conditions. To prevent structural damage due to the need for access of measurement probes, the inductors are modeled with longer access lines providing 200-μm extra conductor length and longer GND lines. Then, simulation results are compared with previous results. The addition of longer access and GND lines increases the inductance and decreases the resonant frequency as shown in Fig. 3. From combinations of the analytical and HFSS simulations, empirical equations for inductance, resonant frequency, and Q-factor as a function of height for various heights of solenoid inductors in the size ranges accessible by the fabrication technology are derived. In particular, for inductors of geometries in the range of 250 μm $\sim$ 600 μm post heights, the inductance, resonant frequency, and Q-factor are given by

$$L = 0.0052h + 1.353[\text{nH}] \quad (5)$$

$$f_{res} = 66.25h^{-0.3298}[\text{GHz}] \quad (6)$$

$$Q-\text{factor} = -0.002h^2 + 0.2728h + 23.298 \quad (7)$$

where h is the height of the inductors in microns.

From these results, a figure of merit (FOM) can be calculated to provide a guideline for determining the optimal height

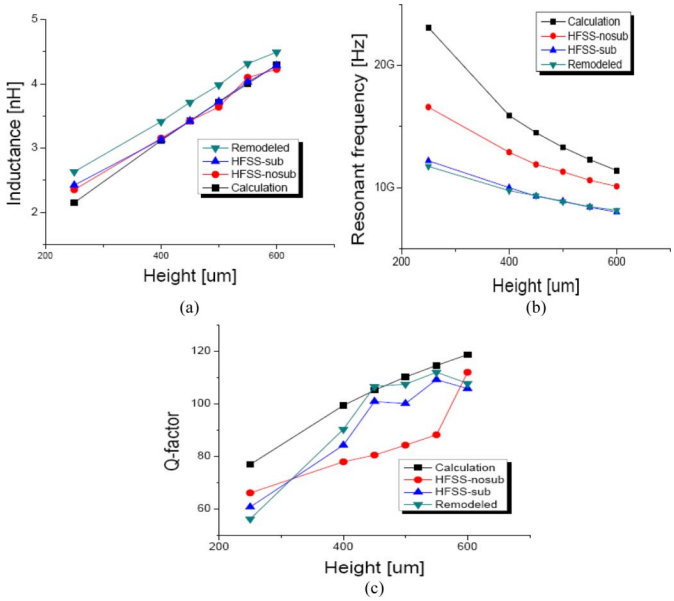

Fig. 3. HFSS results for remodeled structures.

of the inductors. The interconnect layer inductor is designed to have the highest values of inductance, resonant frequency and Q-factor. Thus, one FOM definition is

$$\text{FOM} = L \cdot f_{\text{res}} \cdot Q_{\max} \tag{8}$$

which from a combination of (5)–(7) becomes

$$\text{FOM} = -0.0088h^2 + 10.947h + 298.95 \tag{9}$$

where h is the height of the inductors in microns.

The equation gives a range of high performance inductor height of $(500\ \mu\text{m} \sim 600\ \mu\text{m})$ for a solenoid core width of 550 μm which is a useful guideline for fabrication of inductors of accessible geometries.

IV. Design and Fabrication

A. Design

The chip-to-board layer inductor requires fabrications on both the "chip-side" (typically Si) and the "board-side" (typically epoxy-glass composite). In this work, for ease of initial manufacturing, inductor fabrications are executed on glass and PWB substrates by a flip-chip method. The two substrates to be joined are a 2 cm $\times$ 2 cm glass substrate (as a chip-side surrogate) and a 5 cm $\times$ 5 cm epoxy-glass composite PWB. The transparent glass substrate enables easy alignment; however, in actual use, a conventional through-wafer alignment scheme such as used for flip-chip bonding could be employed [26]. The interconnect layer inductor system requires accommodation of measurement since the substrates obstruct access of measurement probes to electrical pads of the inductors (note that such access would not be required in actual application). The method used in this work is to remove the upper substrate (glass) by etching a sacrificial layer (2 μm aluminum) after electroplating bonding to provide probe access.

Two pairs of three-, five-, seven-, and 10-turn inductors (equivalent to 100 posts) have been designed with a 100-μm gap between the posts on the perimeter of a 1 cm $\times$ 1 cm area. The realized inductors have the same geometrical dimensions as the simulated structures. High aspect ratio posts are formed on both substrates using a photosensitive epoxy (SU-8, Microchem, Inc.) [27] and these posts are subsequently joined using electroplating bonding. The tall conductor posts are formed in two manners: 1) a plating-through-mold method and 2) a polymer core method. The CMOS-compatible plating-through-molded inductor, called hereafter the inductor with solid metallic core, requires a prolonged duration of plating, which can be a critical issue in manufacturable fabrication. Alternatively, the polymer-core-conductor method introduced by Yoon *et al.* [28], in which tall polymer scaffolds covered by electrodeposited metal layers are utilized for the electrical connection, has the potential to reduce the manufacturing time. Such polymer-core conductors are expected to have equivalent performance to their solid metal counterparts at high frequencies due to the skin effect. The distribution of charge carriers is usually described by an effective conductor thickness given by the skin depth δ

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{10}$$

where ω is the angular frequency of the electromagnetic wave, μ is the permeability of the conductor, and σ is the electrical conductivity of the conductor. There is little advantage to construct RF transmission lines or wires much larger than a few skin depths. In the polymer-core conductor approach, for GHz-range signals, a thickness of 5–10 μm of metal on the polymer cores satisfies the requirement of thickness exceeding a few skin depths recalling a skin depth of copper in 1 GHz is approximately 2 μm.

B. Fabrication of a Solenoid Inductor With Solid Metallic Posts

Micro structures (posts and connectors) on both substrates have been formed in the same fabrication sequence, except for an additional aluminum sacrificial layer deposition on the glass substrate. Fig. 4 shows microfabrication sequences of interconnect layer inductors. The establishment of the solid metallic post inductor begins with sputtering of a 2-μm aluminum sacrificial layer on the glass substrate for releasing the substrate at the completion of the entire fabrication process. A seed layer of Ti/Cu/Ti (30 nm/250 nm/30 nm) is then deposited for electrodeposition of conductors and vias on both substrates. On this layer, a polymer mold for Cu conductors designed 20 μm in thickness, 50 μm in width, and 550 μm in length is formed using SU-8 photosensitive epoxy. The mold was then filled using Cu electrodeposition. When the first epoxy mold is filled with electroplated Cu, a thick layer (250 μm) of epoxy is spin-cast on the sample again and patterned to create the mold for the via $(100\ \mu\text{m} \times 100\ \mu\text{m} \times 250\ \mu\text{m})$ with 250 μm turn pitch. This via mold is then filled with electroplated Cu. After the formation of the electroplated Cu structures, the polymers are removed by reactive ion etching (RIE, Plasma Therm, Co.). The prolonged duration of the RIE process reveals the woven PWB surface as shown in Fig. 5(a). In order to prevent damage of PWB due to long RIE process, an additional protection metal layer such as

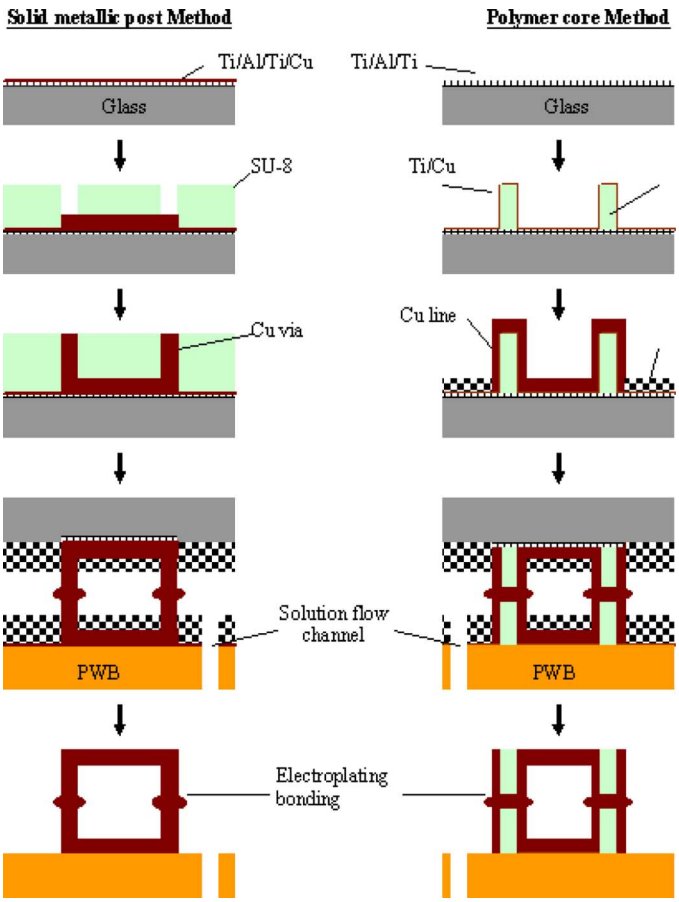

Fig. 4. Fabrication methods for interconnect layer inductors: (left) inductor with solid metallic posts, and (right) inductor with polymer-core-conductor posts.

Ti–Cu–Ti can be placed on top of the PWB before starting the process and can be removed in the last step using wet chemical etching. The seed layer and Al sacrificial layer in the fields of the glass substrate are then selectively etched by metal etchant and RIE, respectively. The seed layer and metal posts on both substrates are then selectively covered with negative NR9-8000 photoresist (Futurrex, Inc.) for preventing unnecessary metal growth on the substrate and metal posts. With the polymer covered substrates, preparation for electroplating bonding is deployed. First, a 1 mm diameter hole is drilled in the center of the PWB substrate to form an electroplating solution flow channel. The channel circulates the electroplating solution to achieve uniform concentration of electroplating solution in the system. The structures on both substrates are manually aligned, clamped together and electroplating bonded. During the electroplating bonding of the structures, lateral copper growing on the structures is controlled by the plating time. The lateral growth is approximately 20 μm. After the bonding process, to facilitate the measurement process, the glass substrate is detached by removing the 2-μm Al sacrificial layer and the Ti adhesion layer by wet etching. Fig. 5(a) shows the SEM pictures of the fabricated structures. The magnified picture of a bonded area is shown in the bottom portion of the figures. The completed electroplating bonded inductors have a height of approximately 500 μm as planned.

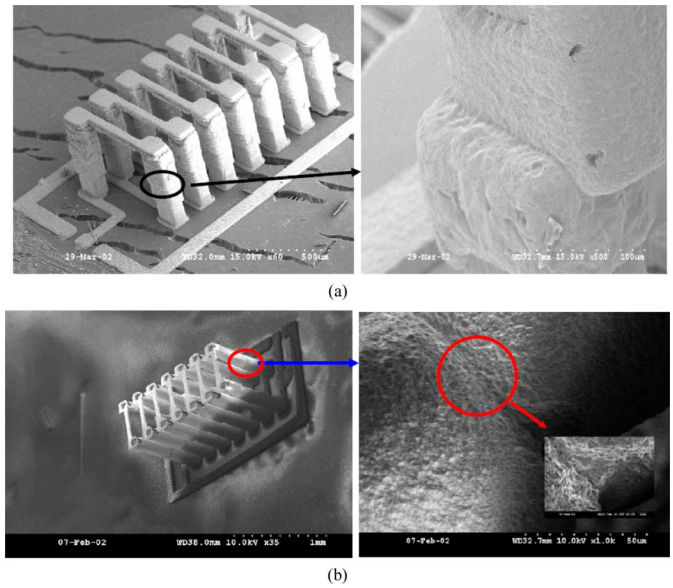

Fig. 5. SEM pictures of the interconnect layer inductors: (a) inductor with solid metallic posts and (b) inductor with polymer-core-conductor posts.

C. Fabrication of a Solenoid Inductor With Polymer-Core-Conductor Posts

The electroplating bonded inductor with polymer-core-conductor posts has the same fabrication sequence as the inductor with solid metallic posts except for the formation of conductors for posts. The Al sacrificial layer deposition and electroplating bonding process follows that of the inductor with solid metallic posts. Electrical connection and pad structures are formed on both substrates (PWB and 2-μm Al sacrificial layer deposited glass). 250-μm epoxy-core-conductor posts are patterned using negative SU-8 photosensitive epoxy and photolithography on both substrates. The patterned epoxy posts function as scaffolds of electrical connection of the inductors. A Ti/Cu/Ti seed layer is deposited over the polymer scaffolds and substrates for the subsequent electroplating step. For selective electrodeposition of the metal posts and conductor lines, negative photoresist NR9-8000 is coated in a thickness of 20 μm and patterned using proximity mode photolithography over the uneven substrate. The patterned NR9-8000 serves as an electroplating mold for electrode patterning both on the bottom surface and on the surface of the epoxy posts to a thickness of 20 μm. The 2-μm Al sacrificial layer in the fields of the glass substrate is then patterned with RIE. The planar portion of the seed layer, metal conductors, and bottom portion of the polymer-core-conductor posts are covered by NR9-8000 to prevent the deposition of copper on the PWB surface and conductors during electroplating bonding of the posts. Electroplating bonding of the structures is then performed as discussed previously. The electroplating bonding duration is approximately half hour. SEM figures of a fabricated seven-turn solenoid inductor with polymer-core-conductor posts are shown in Fig. 5(b).

Since electronic components or chips experience generation of heat during operation, attention should be paid to the mechanical stability of the polymer-core-conductor upon thermal loading. Reliability test for temperatures between 40 °C and

TABLE I
ELECTRICAL PROPERTY SUMMARY OF THE FABRICATED INDUCTOR SETS WITH POLYMER-CORE-CONDUCTOR POST METHOD

	No. of turns	L_{eff} (nH)	Q_{MAX}	SRF(GHz)
Set 1	3	4.4	71@1.9	Over 10
	5	6.1	59@1.6	6.2
	7	11.4	44@1.6	3.8
	10	-	-	-
Set2	3	4.2	72@2	8.6
	5	7.0	64@1.4	6.2
	7	9.6	56@1.3	4.6
	10	13.6	60@0.6	3.3
Set3	3	4.3	64@2.1	8.9
	5	6.6	60@1.7	6.1
	7	12.5	44@1.6	3.5
	10	-	-	-

147 °C with a period of 5 min has been performed for interconnects made of polymer-core-conductors and no failure during 5000 cycles has been observed [12].

V. CHARACTERIZATION

A set of solid metallic post inductors and three sets of polymer-core-conductor post inductors are prepared for characterization. Measurement is performed using a vector network analyzer (HP 8510) with Cascade Microtech's ground-signal-ground (G–S–G) probe (a tip pitch of 150 μm) after standard short-open-load-thru (SOLT) calibration. The calibration has been performed in the frequency range between 0.1 and 10 GHz with 0.05-GHz steps. The electrical properties of the fabricated inductor sets for polymer-core-conductor post inductors are summarized in Table I. The fabricated devices from each set show a little variation (approximately 10%) in inductance and resonance frequency in part due to geometrical variations during the fabrication process such as misalignment related to manual aligning, and non-uniform and rough metal growth from a laboratory-made copper plating system, both of which are expected to be reduced in a manufacturing environment. In the Q-factor performance, quite high Q-factors with little variation are observed for all devices from each set.

A. Characterization of a Solenoid Inductor With Solid Metallic Posts

Q-factor and self-resonance frequency of the inductors are analyzed using a lumped element circuit model for a two-port inductor [29]. The model consists of an ideal inductor in series with a resistor to account for the conductor loss, in parallel with a turn-to-turn capacitance. The dielectric loss and the parasitic capacitance generated by interaction with a substrate are also included in parallel with structural components on both ports.

The S-parameters of the two-port inductor are measured using an HP8510 network analyzer and transformed into effective inductance (L_{Eff}) and Q-factor using a software package of Advanced Design System (ADS, Agilent) [30]. Fig. 6 shows

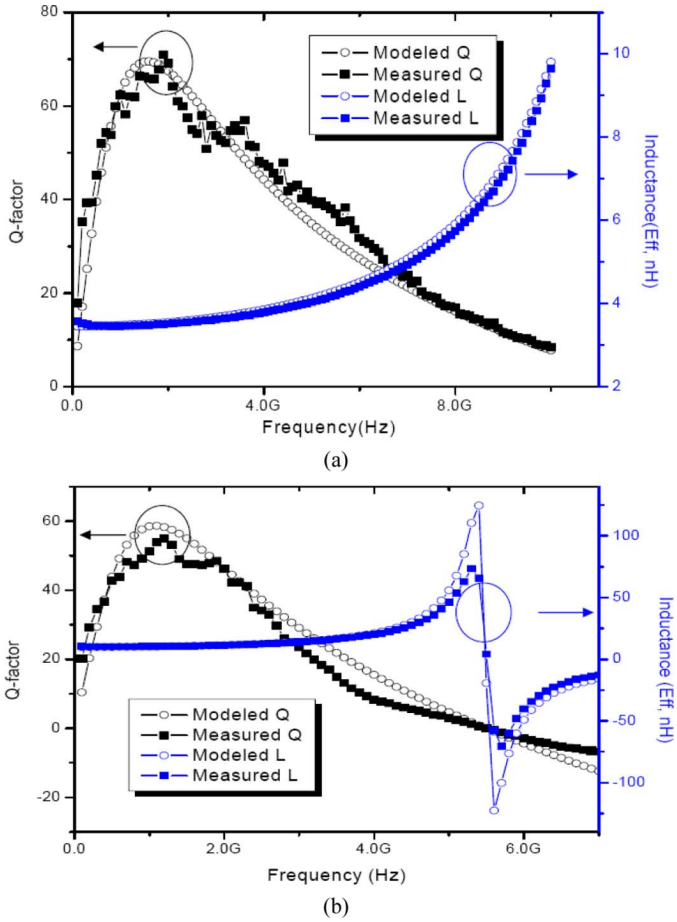

Fig. 6. Measured and modeled L_{EFF} and Q of (a) three-turn and (b) seven-turn inductors with solid metallic posts.

the measured and modeled effective inductances and Q-factors of the three-turn and seven-turn inductors. The effective inductance and Q-factor of the three-turn inductor are 3.6 nH and 71 at 1.9 GHz, respectively; meanwhile the seven-turn inductor has an inductance of 10.4 nH and a Q-factor of 55 at 1.2 GHz. The lumped parameters are extracted from the equivalent circuit model. The parameters for the three-turn and seven-turn inductor are 3.6 nH and 10.4 nH in inductance, 0.31 Ω and 0.71 Ω in resistance, 28 fF and 33 fF in turn-to-turn capacitance(C_0), 23 fF and 50 fF in substrate parasitic capacitance, and 6.5 kΩ and 12 kΩ in substrate resistance representing substrate related loss, respectively. The measured behavior of the inductor over the frequency ranges of interest is well described by Fig. 6 as shown by the close agreement between the measured and modeled curves. The measurements reveal that the electroplating bonded inductors produce much higher inductance for a given number of turns than previously-reported microfabricated solenoid air-core inductors [19], [28], [31], presumably due to the greater flux cross-sectional areas achievable in the interconnect layer.

B. Characterization of a Solenoid Inductor With Polymer-Core-Conductor Posts

The characterization of this style of inductor is done with the inductor set II whose electrical properties are summarized in

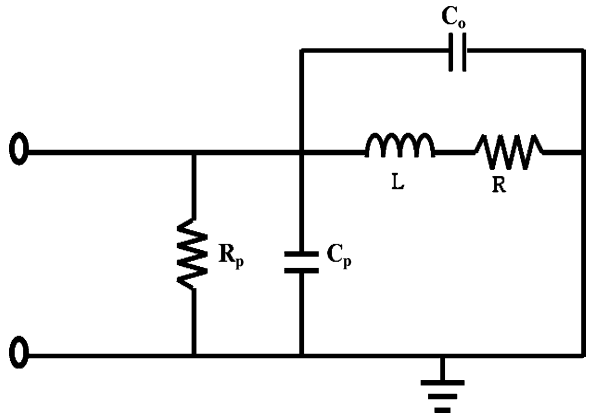

Fig. 7. Equivalent circuit model for an one-port inductor used for the performance evaluation.

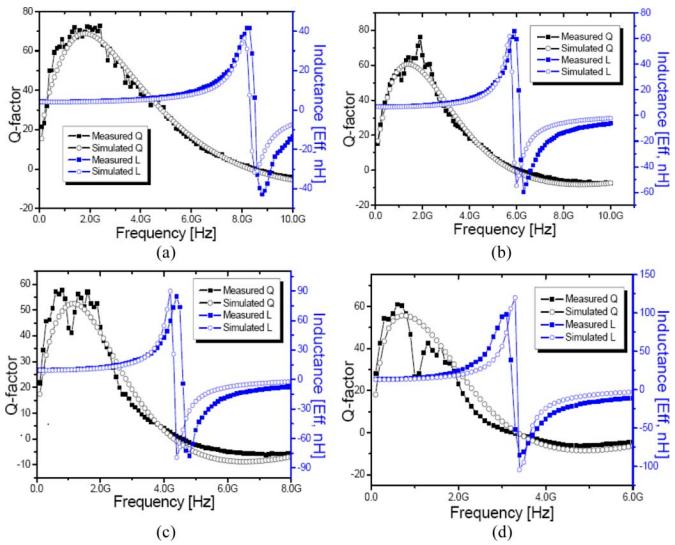

Fig. 8. Measured and simulated L_{eff} and Q of the inductors: (a) three-turn, (b) five-turn, (c) seven-turn, and (d) 10-turn inductors.

Table I. The characteristics of the interconnect layer one-port solenoid inductors with polymer-core-conductor posts are measured and analyzed in a similar fashion described in the previous section. The values are analyzed with a one-port equivalent circuit in Fig. 7. The circuit consists of an ideal inductor L in series with a resistor R to account for the conductor loss and in parallel with a structural capacitance (turn-to-turn capacitance C_0). The substrate loss and the parasitic capacitance caused by electrical interaction between the inductor and the substrate are represented by R_P and C_P, respectively. Moreover, we compare the measurement results with high frequency structure simulations by 3-D HFSS. Fig. 8 shows the measured and simulated effective inductances (L_{eff}) and the Q-factors of the fabricated inductors. Table II summarizes the performance of all fabricated and simulated inductors. The extracted lumped element values for the inductors are shown in Table III. The measured results agree very well with the simulated result except for the substrate capacitance. The difference of substrate capacitance could be attributed to the various factors during the fabrication processes, such as RIE etching, baking, immersion of the sample in the plating solution, etc.

TABLE II
INDUCTOR PERFORMANCE OF A SOLENOID INDUCTOR WITH POLYMER-CORE-CONDUCTOR POSTS

No. of turns		L_{eff} (nH)	Q_{MAX}	SRF(GHz)
3	Measured	4.2	72@2.0GHz	8.6
	Simulated	4.1	68@1.8GHz	8.4
5	Measured	7.0	64@1.4GHz	6.2
	Simulated	6.7	60@1.4GHz	5.9
7	Measured	9.6	56@1.3GHz	4.6
	Simulated	9.4	52@1.2GHz	4.4
10	Measured	13.6	60@0.6GHz	3.3
	Simulated	13.2	55@0.7GHz	3.4

TABLE III
SUMMARY OF EXTRACTED CIRCUIT PARAMETERS OF A SOLENOID INDUCTOR WITH POLYMER-CORE-CONDUCTOR POSTS

No. of turns		L_{eff} (nH)	R (Ω)	C_0 (fF)	C_P (fF)	R_P (kΩ)
3	Measured	4.2	0.4	45	38	8.5
	Simulated	4.1	0.39	47	42	8.5
5	Simulated	7.0	0.53	58	38	10
	Calculated	6.7	0.56	60	49	9.5
7	Simulated	9.6	0.68	70	55	10
	Calculated	9.4	0.74	73	71	10
10	Simulated	13.6	0.76	84	90	11
	Calculated	13.2	0.77	88	83	11

In addition, the extraction of electrical values can be helpful to infer the effect of each electrical component. The analytical expression of the inductor Q of the circuit in Fig. 7 is given by [32]

$$Q = \left[\frac{\omega L}{R}\right]\left[\frac{R_P}{R_P + R\left(1+\left(\frac{\omega L}{R}\right)^2\right)}\right]\left[1 - \frac{R^2 C}{L} - \omega^2 LC\right] \tag{11}$$

where C is the overall capacitance which is the sum of C_0 and C_P.

The first term, $\omega L/R$, accounts for the stored magnetic energy and the ohmic loss only, while the second and the third terms are attributed to the substrate loss and self-resonance factors, respectively. The second term, the substrate loss factor, takes into account eddy current losses due to magnetic flux interaction between the inductor and substrate. The third term describes Q-factor reduction due to coil self-resonance. For a simple example, we use analytical and HFSS simulation results of a three-turn inductor formed on a PWB substrate. Inductance, overall capacitance, and substrate resistance are considered as constant values ($L = 4.1$ nH, $C = 89$ fF, and $R_P = 8.5$ kΩ, respectively) in the frequency range of interest. On the other hand, the resistance of the coil is calculated by (3) as a function of frequency. Fig. 9(a) shows overprediction of Q-factor by the first term($\omega L/R$) in (11), and good agreement between the measured Q-factor and the analytical Q-factor when the full (11) is used. Fig. 9(b) shows the effects of the substrate loss

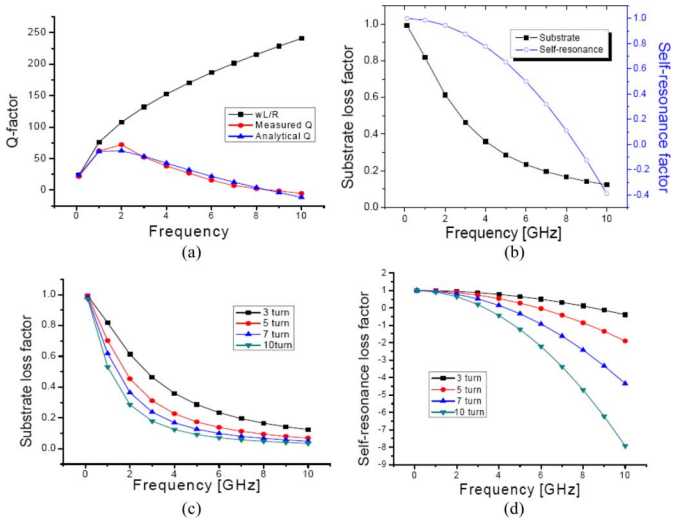

Fig. 9. Frequency response of inductors: (a) Q-factor and $\omega L/R$ term of a three-turn inductor, (b) substrate loss factor and self-resonance loss factor of a three-turn inductor, (c) substrate loss factor of the inductors, and (d) self-resonance loss factor of the inductors.

and self-resonance terms at higher frequencies. Fig. 9(c) and (d) show that the substrate loss factors and self-resonance factors become significant as the number of inductor turns is increased, resulting in lower Q-factors. Detailed analysis and modeling indicates that high inductances are achievable in the chip-to-board interconnect layer for all the fabricated inductors, which is in part due to the large magnetic energy storing capability associated with the large magnetic core cross-section in the give footprint in these examples.

VI. Conclusion

A high inductance, high quality factor, and packaging compatible electroplating bonded inductor for RF systems has been proposed and demonstrated. Different from conventional passive component implementation, these inductors reside in the interconnect layer between the chip and the substrate. This process is compatible with the standard back-end CMOS process. Fabricated structures have demonstrated that the electroplating bonded inductor can lead to real-estate savings on silicon or PWB substrates since structures can be formed in the gap between the substrates. The gap between a board and a chip and other geometrical dimension utilized in the experiment are in a few hundred microns for easy initial implementation without demanding accurate alignment tools in the university environment. The fabrication scheme could be easily scaled down to a gap and other characteristic dimensions of less than 100 μm (note that flip-chip bonding has a nominal gap of 100 μm) with advanced alignment tools and even shorter processing time and cost for the sake of manufacturability although it may require an advanced forced convection flow system for electroplating solution to effectively transfer mass to the central part of the bonded chip [12]. This technique provides a packaged system having Cu interconnection with improved electrical and mechanical characteristics due to short interconnect length resulting in reduced parasitics and potentially reduced substrate coupling, and atomic level bonding characteristic resulting from electroplating metal growth. The inductor characterization has been performed by the mathematical model, equivalent circuit model, and HFSS. A design guideline for a high performance inductor taking into account geometrical factors has been discussed. Two fabrication processes for tall post implementation are successfully demonstrated: a solid metallic approach using plate-through-mold, and a polymer-core-conductor approach using polymer scaffold formation and subsequent metal overcoat over it. The electrical properties of the inductors have been tested and characterized. The simulation results using a circuit model and a high frequency simulation tool give close agreement with the measured results. Inductors with solid metallic posts show high Q-factors of 71 and 55 for the fabricated three-turn and seven-turn solenoid inductors, respectively. Inductors with polymer-core-conductor posts show also high Q-factors of 72, 64, 56, and 61 for three-, five-, seven-, and 10-turn solenoid inductors, respectively, without noticeable degradation due to the encapsulated polymer scaffold post. Although inductors have been chosen as the test vehicle, other large-magnetic-cross-section applications such as antennas may benefit from this approach as well.

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References

[1] M. F. Davis *et al.*, "Integrated RF architectures in fully-organic SOP technology," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 136–142, May 2002.

[2] G. Morcan, T. Lenihan, J. P. Parkerson, L. Schaper, and S. Ang, "Electrical characterization of multilayered thin film integral passive devices," in *Proc. 48th Electron. Comp. Technol. Conf.*, 1998, pp. 240–246.

[3] H. M. Clearfield, J. L. Young, S. D. Wijeyesekera, and E. A. Logan, "Wafer-level chip scale packaging: benefits for integrated passive devices," *IEEE Trans. Adv. Packag.*, vol. 23, no. 2, pp. 247–251, May 2002.

[4] J. L. Young, "Wafer level and substrate level chip scale packaging," in *Proc. Int. Symp. Adv. Packag. Mater.*, 1999, pp. 232–235.

[5] C. Drevon, "From micropackages to MCMs up to 40 GHz for space applications," in *Proc. Packag. Interconn. Microw. mm-Wave Freq. Sem.*, 2000, pp. 8/1–8/4.

[6] R. C. Frye, "MCM-D implementation of passive RF components," in *Proc. IC.Package Design Integr. Symp.*, 1998, pp. 1000–1104.

[7] J. Zhao, R. C. Frye, W. W.-M. Dai, and K. L. Tai, "S parameter-based experimental modeling of high Q MCM inductor with exponential gradient learning algorithm," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 20, no. 3, pp. 202–210, Aug. 1997.

[8] P. Pieters *et al.*, "Accurate modeling of high-Q spiral inductors in thin-film multilayer technology for wireless telecommunication applications," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 4, pp. 589–599, Apr. 2001.

[9] J. Y. Park and M. G. Allen, "High Q spiral-type microinductors on silicon substrates," *IEEE Trans. Magnetics*, vol. 35, no. 5, pp. 3544–3546, Sep. 1999.

[10] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, "Surface micromachined solenoid On-Si and On-glass inductors for RF applications," *IEEE Electron Device Lett.*, vol. 20, no. 9, pp. 487–489, Sep. 1999.

[11] S. Jenei, S. Decoutere, S. Van Huylenbroeck, Guido, Vanhorebeek, and B. Nauwelaers, "High Q inductors and capacitors on Si substrate," in *Monolith. Integr. Circuits RF Syst. Dig.*, 2001, pp. 64–70.

[12] Y.-H. Joung, "Electroplating Bonding Technology for Chip Interconnect, Wafer Level Packaging and Interconnect Layer Structures," Ph.D. thesis, Georgia Inst. Technol., Atlanta, 2003.
[13] L.-W. Pan and L. Lin, "Batch transfer LIGA microstructures by selective electroplating and bonding," *J. Microelectromech. Syst.*, vol. 10, pp. 25–32, Mar. 2001.
[14] R. R. Tummala, Ed., *Microelectronics Packaging Handbook*. London, U.K.: Chapman & Hall, 1997.
[15] K. W. Oh and C. H. Ahn, "A new flip-chip bonding technique using micromachined conductive polymer bumps," *IEEE Trans. Adv. Packag. B*, vol. 22, no. 4, pp. 586–591, Nov. 1999.
[16] *"Ansoft, Version 8,"* Ansoft Corporation, Pittsburgh, PA, 2006.
[17] Y. Niwa, "A study of coils wound on rectangular frames, with special reference to the calculation of inductors," *Res. Electrotech. Lab*, no. 141, p. 133, Apr. 1924.
[18] F. W. Grover, *Inductance Calculation, Working Formulas and Tables*. New York: Van Nostrand, 1946.
[19] Y. J. Kim and M. G. Allen, "Surface micromachined solenoid inductors for high frequency applications," *IEEE Trans. Comp., Packag., Manufact. Technol.*, vol. 21, no. 1, pp. 26–33, Jan. 1998.
[20] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, "A physical model for planar spiral inductors on silicon," in *Proc. Int. Electron Devices Meeting*, 1996, pp. 155–158.
[21] P. L. Dowell, "Effects of Eddy currents in transformer windings," *Proc. Inst. Elect. Eng.*, vol. 113, pp. 1387–1394, Aug. 1966.
[22] M. P. Perry, "Multiple layer series connected winding design for minimum losses," *IEEE Trans. Power Apparat. Syst.*, vol. PAS-98, pp. 116–123, Jan./Feb. 1979.
[23] E. Bennet and S. C. Larson, "Effective resistance of alternating currents of multilayer windings," *Trans. Amer. Inst. Elect. Eng.*, vol. 59, pp. 1010–1017, 1940.
[24] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Trans. Power Electron.*, vol. 9, pp. 127–131, Jan. 1994.
[25] X. Nan and C. R. Sullivan, "An improved calculation of proximity-effect loss in high-frequency windings of round conductors," in *Proc. IEEE 34th Annu. Power Electron. Conf.*, 2003, vol. 2, pp. 853–860.
[26] A. R. Mirza, "One micron precision, wafer-level aligned bonding for interconnect, MEMS and packaging applications," in *Proc. 50th Electron. Comp. Technol. Conf.*, 2000, pp. 676–680.
[27] Fahrni, J. Brugger, P. Renaud, and P. Vettiger, "High-aspect-ratio, ultrathick, negative-tone near-UV photoresist for MEMS applications," in *Proc. IEEE 10th Annu. Int. Workshop (MEMS'97)*, 1997, pp. 518–522.
[28] Y.-K. Yoon, J.-W. Park, and M. G. Allen, "Polymer-core conductor approaches for RF MEMS," *IEEE J. Microelectromech. Syst. (MEMS)*, vol. 14, no. 5, pp. 886–894, 2005.
[29] C. P. Yue and S. S. Wong, "Design strategy of on-chip inductors for highly integrated RF systems," in *Proc. 36th Design Autom. Conf.*, Jun. 1999, pp. 982–987.
[30] *"Agilent Advanced Design System (ADS), 2002 User Manuals,"* Agilent Technology, Palo Alto, CA, 2006.
[31] J.-B. Yoon *et al.*, "High-performance electroplated solenoid-type integrated inductor (SI2) for RF applications using simple 3D surface micromachining technology," in *IEDM Tech. Dig.*, Dec. 1998, pp. 544–547.
[32] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

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