Ultra-Compact Power Conversion Based on a CMOS-Compatible Microfabricated Power Inductor with Minimized Core Losses

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Abstract

A CMOS-compatible microfabricated inductor is presented. The inductor consists of a planar spiral coil optionally sandwiched between upper and lower magnetic core layers. Core materials investigated include ferrite-filled polymer and electrodeposited nickel-iron permalloy ($Ni_{0.80}Fe_{0.20}$). Four core constructions were investigated: air-core (i.e., no magnetic material); lower permalloy core with upper air core; lower permalloy core with upper ferrite polymer core; and lower and upper permalloy core. In all cases with magnetic cores, a nominal magnetic air gap of 2 microns was utilized. As expected, the all-permalloy construction yielded the highest inductance. Inductors were characterized both by impedance analysis as well as in a prototype buck DC-DC conversion circuit. When the converter was operated at 5 MHz, peak efficiency of 82% and an efficiency of 80% at a load current of 2.5A and output voltage of 2V was obtained.

Introduction

Power converter technology, although widely used in modern electronic systems, has resisted full integration primarily due to the difficulty of integrating inductors on-chip. However, the incentive for smaller size and more parallelized fabrication processes are driving the development of a fully integrated, ultracompact power converters, based, e.g., on switching regulation topologies. [1] In addition, interest in ultracompact DC/DC power conversion is accelerated due to two emerging functional trends in power management: a shift towards highly distributed supply voltage generation, with a higher-voltage distribution bus; and, a shift from larger, system-capable power supplies towards smaller, faster-switching power supplies sized only to supply subsystems. [2][3] These trends are exhibited in modern portable electronics, where principal power consumers draw high currents at low voltages, present sharp load transients, and each subsystem operates on a different supply voltage.

Ultracompact, fully on-silicon integrated DC/DC conversion fits both of these trends extraordinarily well. The passive capacity reduction allowed by the latter trend and the concomitant decrease in physical size makes single-chip converters feasible, while the demand presented by the former justifies research and development efforts. In the past, obstacles associated with fabrication of suitably performing inductors as well as adequately lossless and fast switching integrated circuits (ICs) have precluded the development of such a converter.

Of the principal components of a DC/DC converter, shown in Figure 1, the inductor has proven to be one of the most difficult to integrate into a single-die, microfabricated solution. Significant research applicable to power inductor integration has been done in various fields: electrodeposited magnetic materials for recording heads, integrated air-core inductor technology for RF systems, and stand-alone power inductor microfabrication. However, no technique fully compatible with post-CMOS processing has been presented for integrating into a multiwatt-output fully integrated DC/DC converter power inductors of suitable performance.

At switching frequencies on the order of 5 MHz, inductors not incorporating some sort of core material are regarded as insufficient for DC/DC conversion [2][3]. Switching frequencies over 100 MHz can enable use of coreless inductors [4][5], but with current IC technology, switching

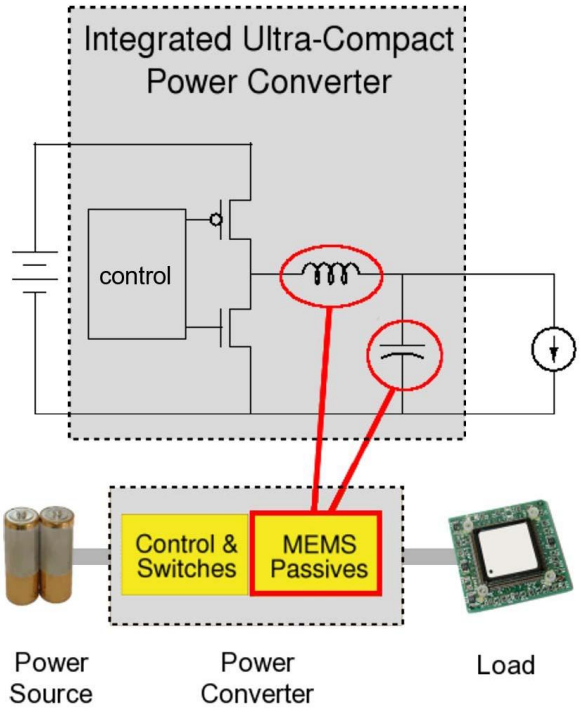

Figure 1. Schematic illustration of electronic system incorporating power conversion for voltage supply. The highlighted components would be integrated into a single silicon die to produce and ultra-compact power converter.

losses at such frequencies can be prohibitive. So, microfabrication-compatible magnetic materials are prerequisite for a practical converter, and, in fact, present the key obstacle apparent to the achievement of a fully integrated converter.

Two basic types of core material have been investigated for this purpose: ferrites, mainly MnZn- and NiZn-based; and electrodeposited alloys, mainly Ni-Fe-based alloys. Both classes of materials introduce crippling limitations; conclusions drawn in [2] suggest that B-H hysteresis losses inherent in ferrites present unacceptable power losses, while the electrodeposited alloys, highly conductive, require very thin (<10 μm) laminations to avoid unacceptable eddy current losses. Previous achievements of integrated DC-DC converters have required high-temperature annealing [6][7] to properly condition magnetic core materials. The most relevant power inductor research has not yet produced a fully integratable inductor incorporating provisions for core loss controls. Park et al. introduced laminations which successfully reduced eddy current loss in alloy cores [8], but their approach was not batch-fabricated. Saidani et al. [9] and Brandon et al. [10] have developed fully-microfabricated, alloy-core inductors, but did not introduce core laminations or any other eddy current loss control features.

This paper presents a technique for fully CMOS-compatible fabrication of on-silicon inductors that incorporate both high-permeability magnetic alloy cores and laminations to address core losses. Also we present characterization of completed inductors and operation of the inductors in a prototype DC/DC conversion system. Using the developed fabrication technique, cores incorporating both plated NiFe alloy and MnZn ferrite are investigated in this research; further, the procedure is developed specifically to incorporate laminations in the NiFe cores to minimize eddy current losses. While the exact lamination size required will depend on the exact properties of the NiFe alloy resulting from the electrodeposition process, which may change depending on functional requirements or other optimizations, the procedure developed allows laminations of practically arbitrary, photolithography-limited size.

The technical discussion opens with a description of the structure of the fabricated inductors and the various core constructions. Then, the steps performed to build the inductors are described in detail, and the finished devices are presented. The electrical characterization data for inductors of different core constructions are shared and discussed, along with encouraging results from a prototype DC/DC converter using one of these inductors as the main energy storage element. Finally, general conclusions and future directions are drawn.

Inductor Structure

The featured design variable for this research is inductor core construction; most other design decisions were firmly constrained by the essential requirement that the inductors ultimately be fabricated on top of a completed CMOS die. This provided both a target footprint and a limited set of core materials and processes. The need for maximally thick metal layers in light of a low thermal budget (~300°C maximum) clearly dictated that electrodeposition should be used to deposit the principal metal layers. In general, chemical vapor deposition (CVD) and plasma-enhanced chemical vapor deposition (PECVD) deposition processes were also prohibited, though a low-temperature SiO_2 PECVD deposition process was found to be feasible.

Planar, rectangular spiral geometry was chosen as a well-tested technique for maximizing inductance per area, and a nominal inductor size of 6 mm × 6 mm was selected. Within these parameters, the number of turns was varied as an inductance vs. coil resistance tradeoff. However, a four-turn design was qualitatively selected as a most likely candidate for integration, and all extended characterization was performed with four-turn inductors.

Four different core constructions, incorporating two different core materials, were investigated. Figure 2 illustrates these four constructions, in the context of the essential magnetic field structure present in an operating inductor. The magnetic circuit enveloping the conductor turns is the central concept, and the core constructions are classified according to the composition of this circuit: all-permalloy (AP) core having permalloy along the entire circuit; half-permalloy (HP) core having permalloy only along the bottom half of the circuit; half-ferrite (HF) core having a ferrite/polymer composite along the top half of the circuit; and an air core which lacks any core material whatsoever.

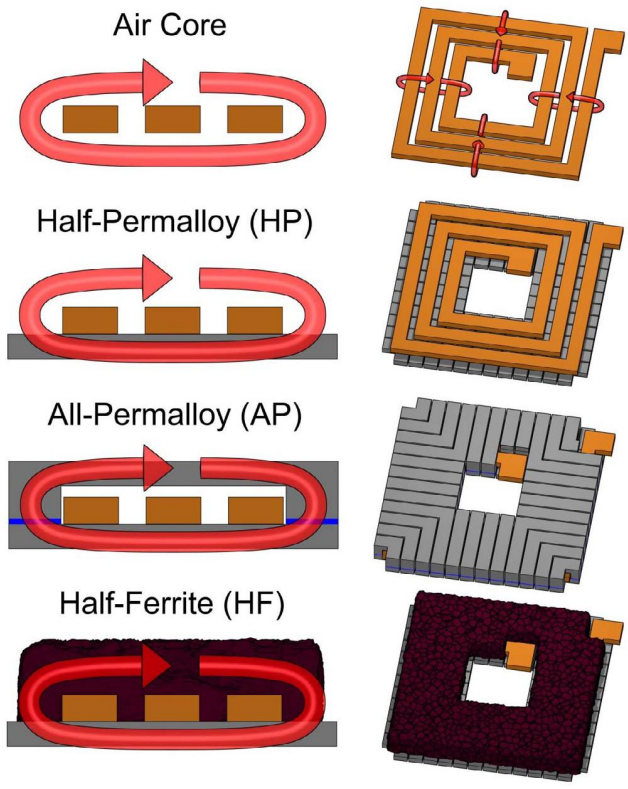

Figure 2. Cross-section and perspective views of the four investigated core constructions. In all diagrams, the translucent red arrow represents the magnetic field produced by current in the coil.

Inductor Fabrication

The inductors were built principally as a series of three depositions: a bottom permalloy layer, then a copper coil layer, and finally a top permalloy or ferrite composite layer to complete the magnetic circuit. Naturally, the half-permalloy construction omits the last step and the air-core construction omits all but the copper coil. Clearly, though, all conductive (i.e. all electrodeposited) layers must be insulated from each other, since either the top or bottom permalloy layers would certainly short adjacent copper lines to each other. Additionally, formation of the electrodeposition molds over severe topologies, such as the bottom permalloy laminations, tended to introduce shadowing-related liabilities into the process. Thus, between electrodeposited layers, electrical insulation was absolutely necessary, and some degree of planarization was strongly preferred.

The optimized process is detailed in Figure 3. A 25 µm-thick NiFe layer is grown on top of the thermally grown oxide. A low-temperature PECVD 1 µm SiO_2 deposition is used to provide electrical insulation, followed by an unpatterned application of SU-8, to seal pinholes in the SiO_2 and provide planarization for the copper plating mold lithography. After a thick copper conductor layer is subsequently electrodeposited, the half-permalloy inductor is complete. Figure 4 shows several views of completed half-permalloy inductors. Optionally, the ferrite composite may be screen-printed to make a half-ferrite inductor.

Several more steps are required to produce an all-permalloy inductor. Most importantly, the copper layer must be electrically insulated from the top NiFe layer. This is done with a 2 µm parylene layer. However, to ensure control over the magnetic air gap, the SiO_2 and SU-8 covering the lower NiFe layer must first be removed with a reactive ion etch (RIE) step, using CHF_3 and O_2 gases. With that done, the parylene film thickness directly sets the air gap, and thus allows excellent controllability. After deposition of the top permalloy, the parylene is removed from the copper with a (CHF_3 / O_2) RIE, simply using the top permalloy as the etch mask for a self-aligned process. Figure 5 shows scanning electron microscope (SEM) photographs of completed all-permalloy inductors.

The all-permalloy process included no planarization after the copper coil layer, which introduced a nontrivial amount of difficulty into the lithography process for the top NiFe mold. Typically, for all electrodeposited layers, sub-optimal mold lithography resulted in unintended, very thin layers of metal connecting neighboring metal pieces. Even a single such failure in the copper coil layer could clearly render an entire inductor useless. However, the presence of these thin connections within in the permalloy layers would only render the affected core laminations partially ineffective, so the unplanarized topology prior to top permalloy deposition was tolerable.

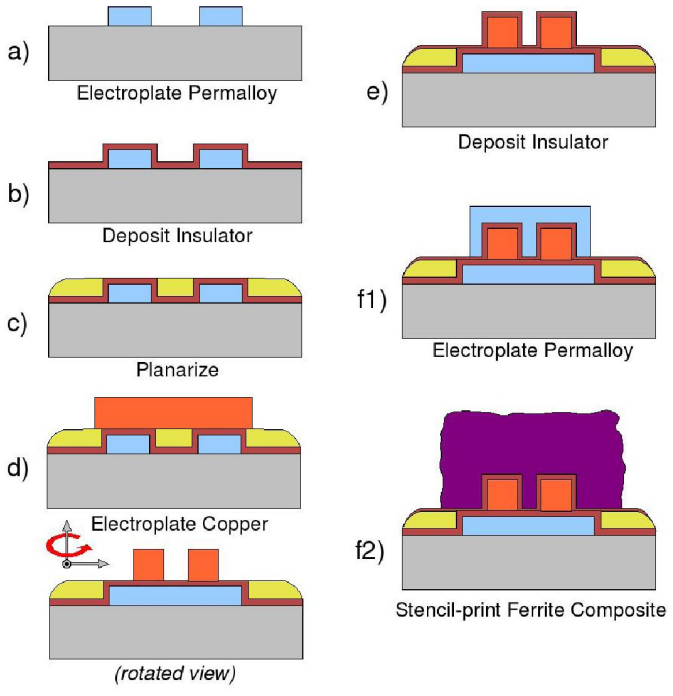

Figure 3. Fabrication process for inductors. Step d) represents a completed half-permalloy inductor, while steps f1) and f2), respectively, represent completed all-permalloy and half-ferrite inductors.

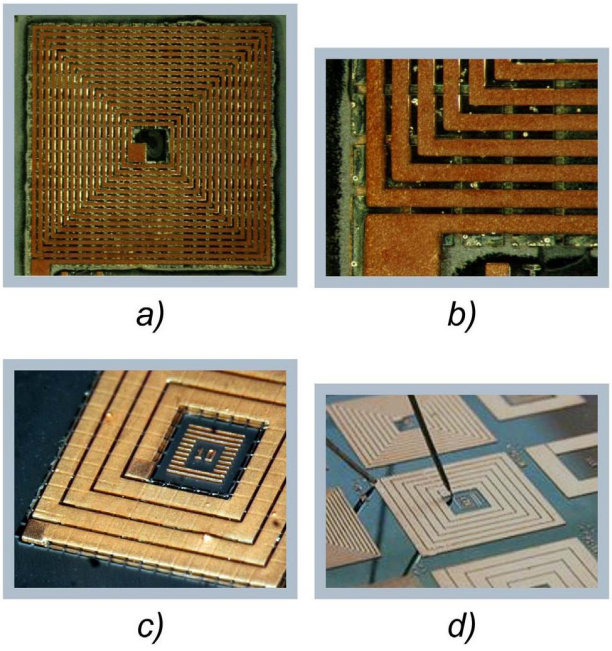

Figure 4. Half-permalloy inductors. a) and b) show a 19-turn inductor, c) shows the four-turn inductor characterized, and d) shows an inductor undergoing component-level characterization with a HP 4194A impedance analyzer. gap and presents a more severe topology over which the top NiFe layer must be electrodeposited.

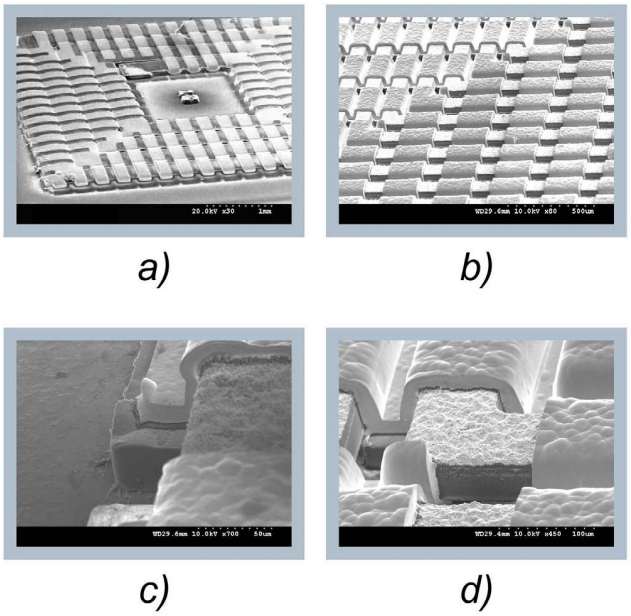

Figure 5. SEM Images of all-permalloy inductor. Due to a smaller gap between copper lines, the inductor pictured in a) exhibits better planarization between the copper and top NiFe layers. In contrast, the inductor in b), c), and d) has a much larger gap.

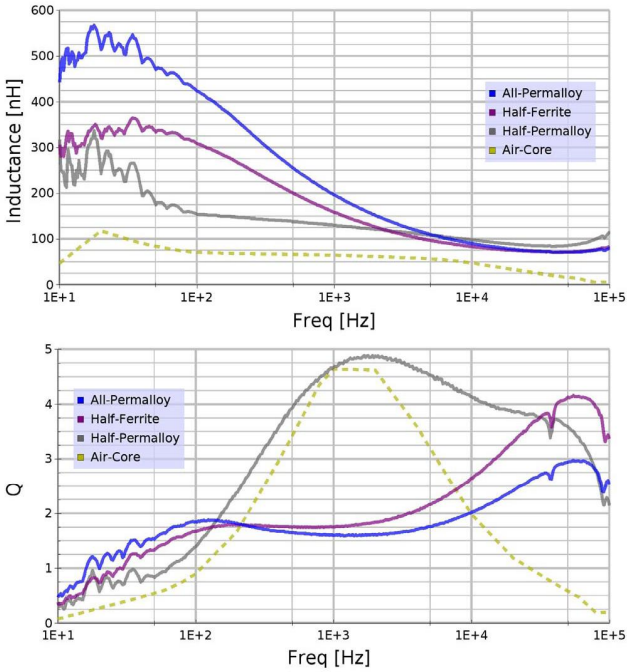

Figure 6. Component-level characterization results. Not surprisingly, the all-permalloy inductor shows the largest inductance. It is believed that eddy currents lower the Q for the all-permalloy inductor, but B-H hysteresis losses lower the half-ferrite inductor's Q. Note that around 10 MHz, the half-ferrite inductor has approximately the same inductance as the half-permalloy, but a lower Q.

Inductors of all four varieties were fabricated on test-grade silicon wafers (550 µm, 1-10 Ω-cm, p-type) with 1 µm of thermal oxide. For all electrodeposition steps, Futurrex NR2-20000P thick negative photoresist was used as the plating mold. In all cases, a sputtered Ti(300 Å) / Cu(3000 Å) / Ti(300Å) metallization was used, unpatterned, as the seed layer and etched away, unmasked, immediately following mold removal. A plating current density of 10 mA/cm^2 was used for plating of both copper and NiFe.

The ferrite composite core material consisted of SU-8 (Microchem, Inc., http://www.microchem.com) filled with a ground MnZn ferrite powder (Ferrite Loading Powder 73399, Steward, Inc., http://www.stewardmaterials.com). The ferrite powder, with an initial mean diameter of 10 µm, was ball-milled for 72 hours to reduce particle diameter for improved rheology and fill factor. During the ball-milling process, the ferrite powder was immersed in Thinner P (Microchem, Inc.), an SU-8-compatible solvent, so that the ball-milled slurry could be immediately mixed with SU-8. This avoided a separate milling solvent separation step and also promoted solvent-particulate bonding and, consequently, optimum filler-matrix interspersion.

Due to Thinner P's strong SU-8 compatibility and high volatility at room temperature, the viscosity of the uncured composite could be easily tailored over a very wide range by either addition or evaporation of Thinner P. This controllability allowed the use of ordinary stencil-printing processing to deposit the top half of the magnetic core for the half-ferrite inductors. The stencils were cut from 1mm-thick Mylar sheets.

The final ferrite polymer composite consisted of 95% ferrite powder, by weight, and exhibited a solidly opaque, black appearance. Though SU-8 cross-links very nicely under UV exposure, the extreme fill ratio of our composite precluded significant photo-cross-linking. However, with excess solvent evaporated, the composite was sufficiently viscous to hold its stenciled form for the 8-hour, 130°C cure necessary to ensure SU-8 cross-linking in the absence of UV exposure.

Component-Level Characterization

Completed inductors were characterized in two different ways. First, a HP 4194 Impedance Analyzer was used to measure inductance and quality factor (*Q*) as a function of frequency. Second, a finished four-turn inductor was used in conjunction with a custom DC/DC converter IC to implement a functioning buck converter

The impedance analyzer frequency was swept from 10 kHz to 100 MHz, approximately centered on the expected switching frequency range of 1 to 10 MHz. The HP 4194's open-circuit and short-circuit compensation features were used to minimize the impact of measurement parasitics. Figure 6 shows the results, comparing all four inductor constructions.

As expected, the air core inductor, possessing no energy-storing core material, showed the lowest inductance. The addition of the bottom NiFe layer for the half-permalloy case produced a dramatic increase in inductance. A similar yet lesser increase is apparent with the addition of the top NiFe

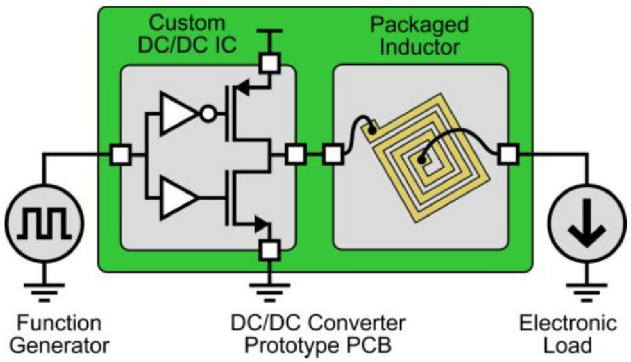

Figure 7. In-system characterization schematic. Though the system was packaged as a PCB, the DC/DC IC was built using typical CMOS technology, and is thus representative of the circuitry that would be used in a practical integrated converter.

layer. All permalloy-based inductance increases tended to vanish at higher frequencies, and this is attributed to decreasing usable core volume due to the skin effect. In contrast, the ferrite core material, as an electrical insulator, is expected to exhibit effectively no skin effect losses. This expected behavior is readily seen in the graph, as the apparent inductance gain associated with the addition of the ferrite core does not decrease with increasing frequency.

In-System Characterization

The impedance analyzer results suggest these inductors should perform well in a MHz-switching DC/DC converter. To verify this, the additional step was taken of including a 4-turn all-permalloy inductor in an operating DC/DC buck converter circuit. A schematic of the in-system characterization is shown in Figure 7, and an oscilloscope capture of the key waveforms of the operating system is shown in Figure 8.

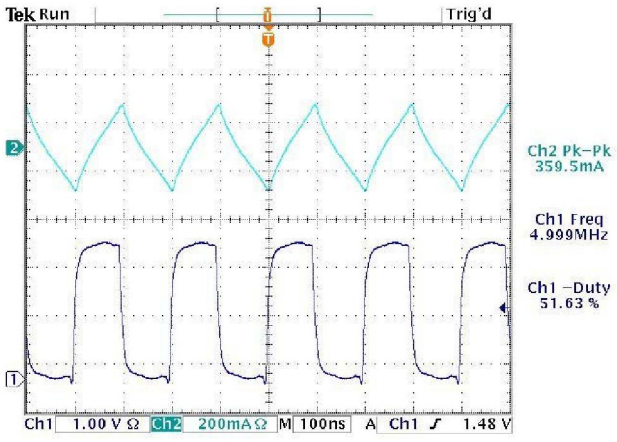

Figure 8. Waveforms showing operation of prototype DC/DC converter. The top trace (200 mA/div) is inductor current. The bottom trace (1 V/div) is the switched output voltage, taken at the node joining the inductor and the DC/DC IC's output transistors.

Though this system is a prototype, printed circuit board (PCB) based DC/DC converter, without autonomous control or dynamic optimizations such as soft switching, it accurately estimates the electrical behavior of a fully integrated DC/DC converter. The custom DC/DC IC was fabricated using CMOS technology and design rules similar to that which might be used in a practical converter. Additionally, an electronic load (Kikusui PLZ164W) was used to simulate a typical IC load. Thus, except for PCB-related parasitics, the critical components of the power switching path – the power switches, the inductor, and the load – were highly representative of a fully integrated converter scenario.

PCB interconnect parasitics, and the associated losses, were not calibrated out of the efficiency measurements However, the inductor was wire-bonded into a ceramic DIP package for attachment to the PCB. This introduced significant DC resistance, around 120 mΩ, and the corresponding I^2R loss is factored out of the presented efficiency results.

The supply voltage for the prototype converter was 3 V, and the output voltage was 2 V. Two different switching frequencies, 1 MHz and 5 MHz, generated as square wave outputs from a function generator, were used. By varying the duty cycle of the square wave switching signal, the output current was swept from 0 to 2.5 A, for a maximum output power of 5 W. At each test point, converter efficiency was measured, as the power delivered to the electronic load divided by the power output by the 3 V input supply. Figure 9 presents the complete characterization results. The peak efficiency for 5 MHz switching was 82%, and the peak efficiency for 1 MHz switching was 79%.

Conclusions

In light of the principal concerns and requirements related microfabricated inductors for integrated, ultracompact power conversion, an inductor fabrication process meeting such needs is presented. The inductors are also designed around the concept of controlling core losses at expected MHz switching frequencies. The inductors offer the use of ferrite or Ni/Fe alloy cores, and for the latter case include provisions

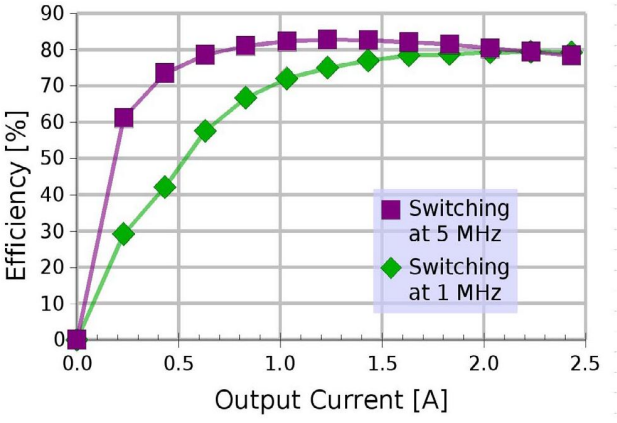

Figure 9. In-system characterization results. The lower-amplitude AC current at the faster switching frequency is credited with the increase in efficiency

for core laminations to reduce eddy current losses. As well, no high-temperature processes are required, which grants maximum processing compatibility with completed CMOS wafers. This makes our inductor an optimum candidate for integration onto a silicon die to produce an ultracompact DC/DC converter.

Finished inductors were tested individually, to show their performance at expected frequencies, and in a PCB-based prototype DC/DC converter to prove their usability for voltage conversion. Future development work for this inductor includes integration-oriented tasks such as CMOS-inductor interconnect development, as well as device-oriented tasks such as core alloy magnetic properties and lamination geometry optimization.

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