Thermomigration-Based Junction Isolation of Bulk Silicon MEMS Devices

Charles C. Chung and Mark G. Allen, *Senior Member, IEEE*

***Abstract*—Electrical isolation of bulk-micromachined single crystal silicon (SCS) microelectromechanical systems (MEMS) devices is demonstrated using through-wafer junction isolation. Through-wafer junctions of alternating n-type and p-type silicon (npn junctions) are fabricated using "temperature gradient zone melting" (TGZM) or thermomigration of aluminum in n-type silicon. The npn regions electrically isolate various regions of the SCS from one another by acting as series connected backbiased diodes. Thermomigration is a potentially high throughput process that is consistent with batch fabrication principles. Practical demonstration of this technique is shown by fabricating and testing a full wafer thickness ($\sim$300 μm) electrostatic actuator fabricated from a single silicon wafer, and driven at 360 Vpp at resonance of 1933 Hz. Breakdown voltages of single thermomigrated npn junctions in excess of 189 V with leakage currents less than 70 nA were measured. For multiple junctions in series, overall breakdown voltages greater than 1500 V were demonstrated. Compatibility of thermomigration with standard p-channel metal–oxide–semiconductor (PMOS) transistors is also demonstrated. [1345]**

***Index Terms*—Bulk micromachining, deep reactive ion etching (DRIE), diodic isolation, electrical isolation, inductively coupled plasma (ICP), junction isolation, temperature gradient zone melting (TGZM), thermomigration.**

I. Introduction

BULK-MICROMACHINED, single crystal silicon (SCS), microelectromechanical systems (MEMS) devices enjoy a number of advantages including:

— good material properties, such as an absence of internal stress, relative immunity from material fatigue, and high Q-factors in mechanically resonant structures;

— large thicknesses in the device components with dimensions ranging up to the thickness of the wafer (hundreds of micrometers thick);

— natural integration with microelectronic components.

With the introduction of deep reactive ion etching (DRIE) technologies, single crystal silicon structures hundreds of micrometers tall with 40:1 aspect ratios are reliably reproducible [1]. This has vastly expanded the accessible design envelope for bulk-micromachined SCS MEMS devices. However, because these devices are fabricated from a single piece of silicon, all the components are electrically connected through the bulk. In order to support voltage gradients, an electrical isolation scheme is necessitated.

In the past, there have been three general approaches to electrically isolating bulk-micromachined actuators in SCS. The first approach involves physically separating each piece in silicon by etching gaps between the parts to be isolated and attaching the individual parts to a handle wafer to hold the separated pieces in position relative to one another [2], [3]. This approach has been widely used; however, the handle wafer often presents difficulties in the final structure. For example, for active electromechanical devices on a moving platform, the handle wafer adds a great deal of bulk, mass, and asymmetry to the platform.

The second approach is similar, i.e., intervening silicon is removed to electrically isolate various regions; however, instead of leaving a gap, the intervening gaps are backfilled with an insulating material, typically silicon dioxide or doped polysilicon, to restore the mechanical integrity of the wafer [4], [5]. This approach is also very popular; however, it scales in difficulty with increasing thickness and aspect ratio. Moreover, the mechanical characteristics of the overall device additionally depend on the backfilled material and the interface between the backfill and bulk silicon, which typically have poorer mechanical properties than the original silicon.

The third approach is to use the bulk-etched silicon as a mechanical material, and then to add electrically isolated films to the silicon for the electrical subsystem, such as in the SCREAM process [6]. To accomplish this, the microdevice is first bulk-etched from the silicon. An insulating layer is either grown or deposited on the bulk-etched structure. Finally, to make the surface electrically active, conductive layers, such as metallic films, are deposited onto the sidewalls of the microstructure as well as the top surface. This approach requires metallization of the sidewalls, which scales in difficulty with increasing aspect ratio.

An alternative to these approaches is to take advantage of the semiconducting properties of silicon to form diodic isolation. This approach is widely used in microelectronic devices and is referred to as "junction isolation" or "diodic isolation," [7], [8] due to the fact that npn or pnp regions are fabricated, thereby creating two series-connected backbiased diodes that electrically isolate one region from another. This approach has the advantage of electrically isolating various parts of the silicon while retaining the original mechanical integrity of the single crystal material.

However, junction isolation has not been employed as an electrical isolation scheme for bulk silicon MEMS devices, primarily because in order to achieve isolation, it is necessary to dope the silicon through the entire thickness of the etched device, which may be hundreds of micrometers thick. Typical

Manuscript received May 19, 2004; revised February 27, 2006. The work of C. C. Chung was performed while he was with Georgia Institute of Technology, Atlanta. Subject Editor D.-I. Cho.

C. C. Chung was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA. He is now at LV Sensors, Emeryville, CA 94608 USA (e-mail: cccatl@yahoo.com).

M. G. Allen is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: mark.allen@ee.gatech.edu).

Digital Object Identifier 10.1109/JMEMS.2005.879685

methods for doping silicon such as diffusion or ion implantation are inadequate to achieve such large junction depths.

However, the doping of silicon with junction depths on the order of hundreds of micrometers has been demonstrated in a process known as "temperature gradient zone melting" (TGZM) or "thermomigration" [9]. In this process, a thermal gradient is imposed through the thickness of the wafer, and dopants deposited on the cooler side propagate along the thermal gradient either until the opposite face is reached or until the dopant material is exhausted.

TGZM may be employed in fabricating junction isolated bulk-micromachined devices, e.g., by propagating a p-type dopant through n-type silicon. This fabricates npn or pnp regions through the thickness of the wafer, across which current is unable to pass (except for a leakage current) up to the diodic breakdown voltage. The npn or pnp regions allow the bulk silicon to sustain a voltage drop across the junction isolation, thereby enabling electromechanical functionality without compromising the mechanical integrity of the wafer.

II. Temperature Gradient Zone Melting (TGZM)

TGZM, or thermomigration, was first applied to semiconductor processing in 1955 by Pfann [9]. From 1973 to 1981, Anthony and Cline [10], [11] investigated this process for various solvent/solute systems. In the early 1990s, thermomigration was applied to the fabrication of three-dimensional (3-D) integrated circuits [12] and intracortical electrode arrays [13]–[15].

TGZM may be performed with many solvent/solute systems. In the application of junction isolating bulk-micromachined, SCS structures, n-type silicon was chosen for the bulk or solute, and aluminum was chosen as a p-type dopant or solvent because of its relatively high-diffusion coefficient in silicon.

TGZM is typically performed by first depositing and photolithographically patterning a dopant, e.g., aluminum, on one side of a silicon wafer. The other side of the wafer is then radiatively heated to approximately 1000 °C. As a result of the one-sided heating, a temperature gradient is established through the thickness of the wafer. Once above the eutectic point, the aluminum melts and dissolves some of the silicon at the surface. The resulting droplet follows the thermal gradient towards the hot surface. As the droplet moves, the warmer side of the droplet dissolves more silicon, and the cooler side of the droplet resolidifies epitaxially; the resolidified material has an aluminum concentration determined by the solid solubility limit for aluminum in silicon at the solidification temperature, approximately 2×10^{19} cm^{-3}[16]. The process is highly anisotropic and relatively fast, with droplets traveling through a 300-μm-thick wafer in less than 10 min.

When appropriate patterns of aluminum are thermomigrated through n-type silicon, npn regions are created through which current (except for a diode leakage current) is unable to pass, up to the breakdown voltage of the reverse-biased diodes. The npn regions allow a voltage drop across the junction isolation [e.g., between regions 1 and 2 of Fig. 1(d)] to be sustained without compromising the mechanical integrity of the wafer.

In this paper, the smallest achieved 300-μm-deep junctions are 50 μm in lateral width with the available equipment. Higher temperatures allow narrower junctions with 35 μm demonstrated in the literature. [15]

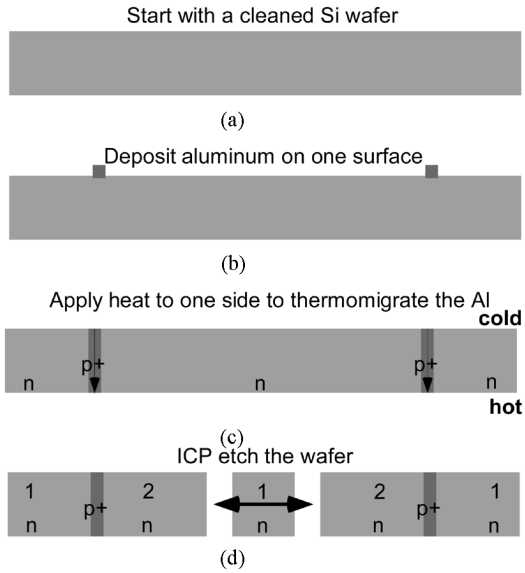

Fig. 1. Process flow for junction isolated, bulk-micromachined, SCS microdevices via thermomigration. (a) The n-type silicon wafer with a resistivity of 1–30 Ω-cm is cleaned. (b) 5 μm of aluminum is evaporated and patterned lithographically. (c) The sample is thermomigrated by heating one side. The aluminum propagates through the wafer along the thermal gradient from the cooler side to the hotter side. (d) The wafer is etched using ICP-RIE. Regions 1 and 2 are now electrically isolated up to the breakdown voltage and leakage current.

III. Fabrication Process

An overview of the process flow is presented in Fig. 1. To prepare the wafer for the thermomigration process, a prime grade, n-type, $\langle100\rangle$, $2''$ diameter, 300-μm-thick, SCS wafer with a resistivity of 1–30 Ω-cm is cleaned using a standard peroxide-based organic and ionic cleaning procedure. The wafer is then metallized with 5 μm of aluminum. The aluminum is patterned photolithographically and etched in a solution of phosphoric, acetic, and nitric acids (PAN etch) at 50 °C.

To perform the aluminum thermomigration, a CVC products filament evaporator was adapted by replacing the filament normally used to evaporate metals with a heating element made of a 60 mm × 100 mm × 125 μm tantalum sheet.

The silicon wafer is inserted into a vacuum chamber and placed as close to the filament as possible without touching the heating element (several millimeters). The wafer side with the aluminum faces away from the filament. A thermal compensation ring is placed around the silicon. The purpose of the ring is to reradiate heat into the edge of the silicon wafer. This reduces the radial temperature gradient that arises from radiative cooling at the edge of the wafer. Reduction of the radial thermal gradient increases the usable area of the thermomigrated wafer. Without the ring, the usable thermomigrated area is approximately 1 cm^2, while with the ring, that area increased to approximately the entirety of a $2''$ wafer.

A strong radial component in the thermal gradient induces npn geometries with a strong radial component. This results in npn junctions that are not perpendicular to the surface of the

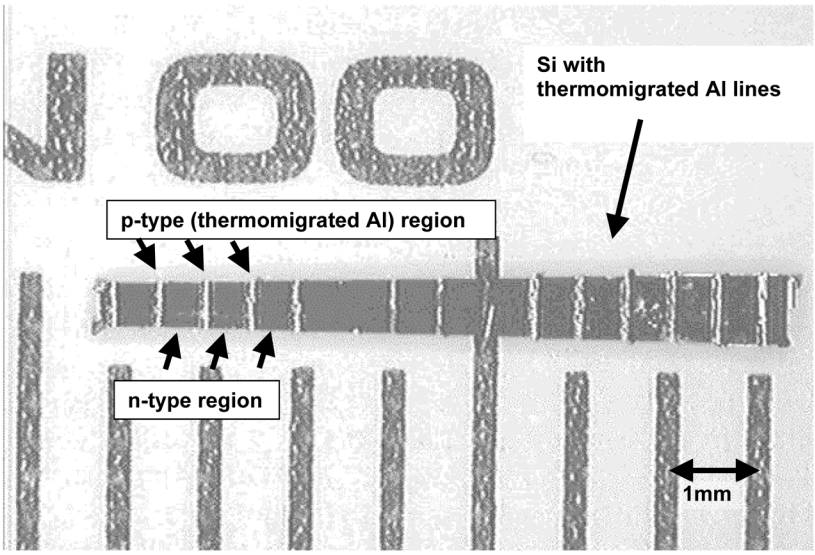

Fig. 2. I–V characterization test structure. Each tick on the ruler is 1 mm. There are 12-npn junctions on this structure. Each p-doped area is 100 μm wide and separated by 500 μm of lightly doped n-type silicon.

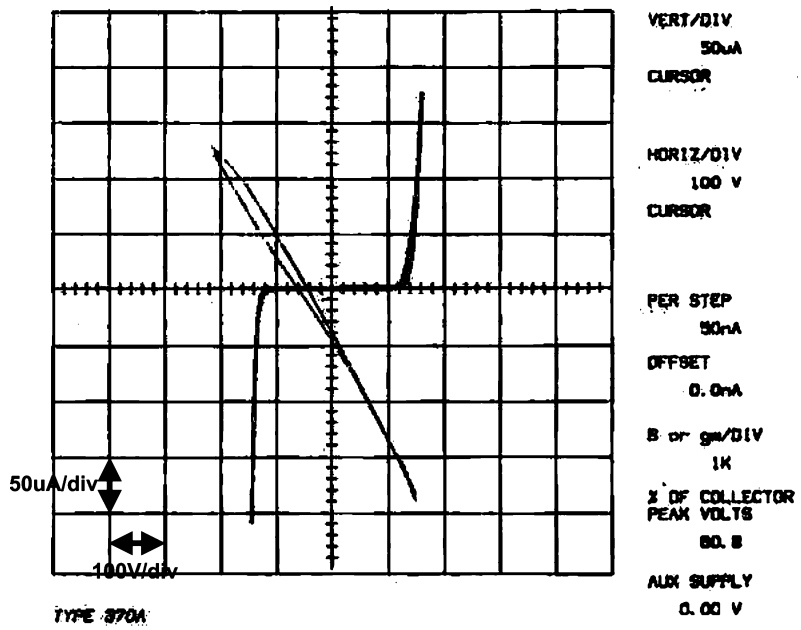

Fig. 3. Example I–V curve from one of the 12-npn junctions. The breakdown voltage is ± 140 V with a leakage current of less than 10 μA at voltages less than breakdown.

wafer. Nonperpendicular junctions can cause a number of difficulties. For example, some of the aluminum may travel laterally into other, unintended, parts of the device. Another difficulty is that nonvertical npn junctions have reduced breakdown voltages compared to vertical junctions.

The ideal thermal compensation ring would have emission and absorption characteristics identical to silicon such that it would reach a thermal steady-state at the edge of the wafer that would be exactly like the center of the wafer. As a result, the thermal compensation ring was constructed of silicon as well, and both the thermal compensation ring and the silicon wafer were heated so that the two would behave thermally as closely as possible as one continuous piece of silicon. For a $2''$ wafer, the thermal compensation structure was 60 mm $\times$ 60 mm $\times$ 700μm with a circular hole in the middle with a radius of 26 mm to accommodate a 25.4-mm radius, 300-μm-thick Si wafer. The thermal compensation structure was purposely made slightly thicker than the 300-μm-thick silicon wafer to increase the fraction of photons that are captured and exchanged with the wafer edge.

On the other side of the filament from the silicon wafer and thermal structure, a reflector made of three layers of polished tungsten is placed closely to the heating element. The reflector returns photons to the filament that would otherwise be lost. This boosts overall efficiency and ensures more of the available power is directed into the silicon wafer.

Once the heating element, silicon wafer, thermal compensation structure, and reflector are in the chamber, the chamber is

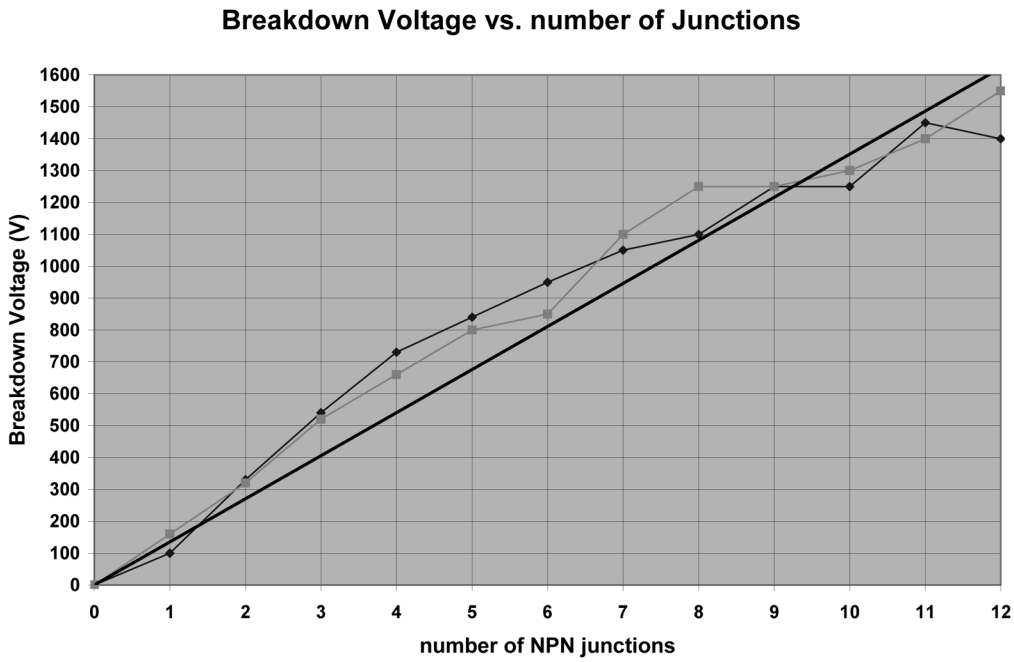

Fig. 4. Multiple npn junctions arranged in series increases the overall breakdown voltage with 12-npn junctions having an overall breakdown voltage of -1550 and $+1450$ V. The graph shows breakdown voltage as a function of the number of npn junctions. The breakdown voltage increases roughly linearly with each junction contributing 138 V on average. Breakdown voltages of 189 ± 37 V per junction have been achieved with improved processing.

closed and a vacuum established $< 2 \times 10^{-6}$ torr. 360 A at 5 V is then applied across the heating element, with the heating element reaching approximately 1200 °C. The heating element radiatively heats both the wafer and thermal structure to an average temperature of approximately 1000 °C from one side. The opposite side of the wafer is allowed to cool radiatively.

Since one side of the wafer is radiatively heated, and the other side radiatively cooled, a thermal gradient is established and the aluminum thermomigrates through a 300-μm wafer within 1.5 h. Shorter process times are possible with higher average temperatures. Given the available equipment, the thermomigration process was power limited. As a result, a tradeoff between thermomigrated area and average temperature needed to be made. If smaller thermomigration areas were chosen, the power was more concentrated and higher average temperatures for the thermomigration were possible. Under these conditions, aluminum may be driven through a 300-μm wafer in less than 10 min. However, if larger thermomigration areas were needed, the available power was distributed over a greater area, which drops the average temperature and increases the process time. With sufficiently sized power sources, both large area and high temperatures may be achieved for quick thermomigration of large wafers.

After the thermomigration, the filament is switched off, and the chamber is allowed to cool for 10 min. The chamber is then vented with nitrogen and the sample is allowed to cool another 10 min in nitrogen atmosphere.

Once the aluminum is thermomigrated through the silicon, the excess aluminum and the heat damaged silicon must be removed, since both reduce the breakdown voltage of the junction. Other groups have reported success with lapping these materials [13]–[15]; however, the wafers were prone to fracturing due to the mechanical loads of this step, resulting in poor overall yield. Instead, the silicon and aluminum were etched in a solution of

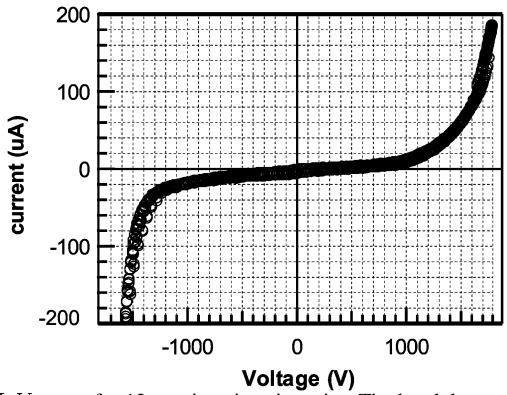

Fig. 5. I–V curve for 12-npn junctions in series. The breakdown voltage for 12-npn junctions is -1550 and $+1450$ V with a leakage current at less than 10 μA for voltages less than breakdown. Leakage currents as low as 68 ± 8 nA have been achieved with improved processing.

$HF : HNO_3 : H_2O$ at a ratio of $20 : 50 : 35$ for 3 min. This solution preferentially etches heavily doped silicon. Since this solution etches the silicon as well as the aluminum, the overall thickness of the wafer is typically reduced from 280–200 μm. The replacement of the lapping process with a chemical one allowed process compatibility of the thermomigration process with integrated circuitry, which will be discussed later.

The sample is then optionally stained with 99% HF and 1% HNO_3, which darkens the aluminum-doped areas, and facilitates alignment to the thermomigrated aluminum-doped silicon regions.

Once the npn regions are fabricated, to form the bulk-micromachined structure, the thermomigrated wafer is deep reactive ion etched. A photoresist mask is used and the wafer is etched using the Bosch process [17]. Both the n-type silicon and the Al-doped silicon are etched using the standard Bosch process; however, the Al-doped silicon etches at about half the rate of

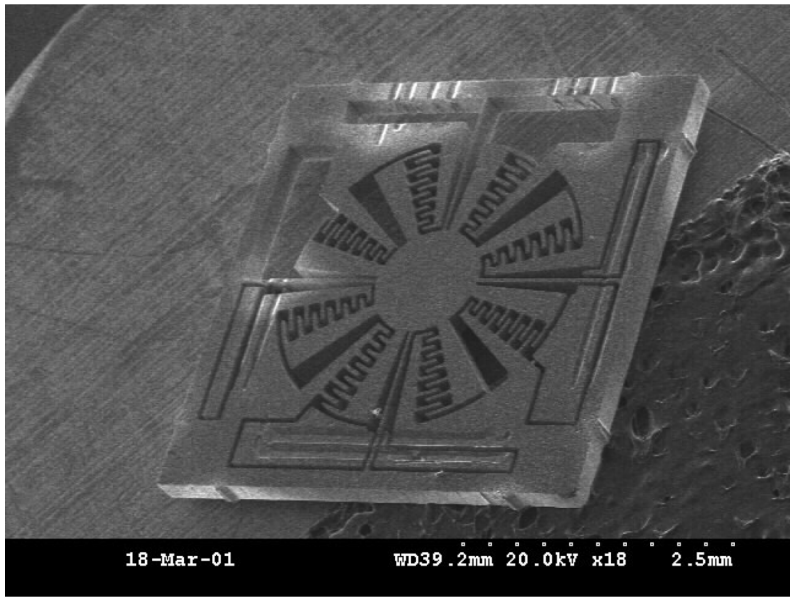

Fig. 6. SEM of the demonstration rotary actuator. The overall chip dimensions are 4.5 mm × 4.5 mm × 200 μm. The beams measure 30μm×1.5 mm× 200μm. The chip is electrically divided into an inner and outer portion by the Al thermomigrated npn junctions. There are two npn junctions on three of four beams, and there are four npn junctions on the edge of the chip on each side of the beam.

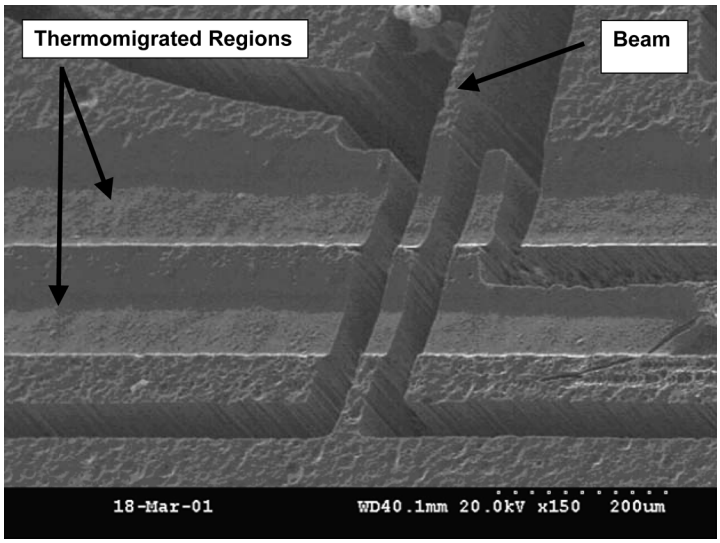

Fig. 7. Closeup of the thermomigrated area on one of the beams. The p-doped silicon regions are smoother and "indented" in comparison to the surrounding n-type silicon. The p-dope regions are 75 μm wide.

the lightly doped n-type silicon. The etch-rate mismatch can be reduced by taking advantage of reactive ion etch (RIE) lag, i.e., the etched areas around the Al-doped silicon are made larger to increase the etch rate. Although a detailed examination of this process was not undertaken, it was empirically determined that this approach was satisfactory for etches extending through the thickness of the wafer.

After the inductively coupled plasma (ICP) etch, the remaining photoresist was removed with acetone and the wafer was cleaned with a solution of NH_4OH, H_2O_2, and H_2O. Fig. 2 shows a photomicrograph of fabricated test structures.

IV. Isolation Characterization

Because junction isolation uses two series connected backbiased pn junctions, there is a finite voltage that the junction can sustain before breakdown occurs, i.e., the "breakdown voltage."

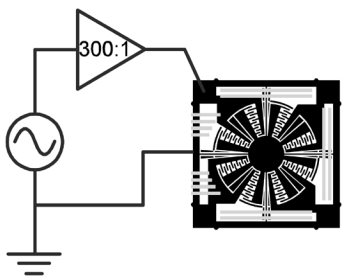

Fig. 8. Electrical model for the demonstration actuator. The actuator is divided electrically into an inner and outer portion. The inner part (the "rotor") is connected to ground. The outer part (the "stator") is driven by a sinusoidal signal from an HP 33120 A function generator that is amplified 300:1 by a Trek 50/750 high-voltage amplifier.

Furthermore, there is a small current that flows from one side of the npn junction to the other, i.e., the "leakage current." These

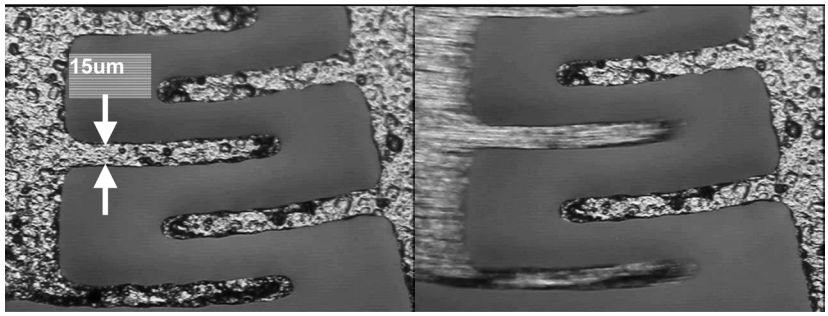

Fig. 9. Photomicrograph of the rotary comb drive. (a) Fingers are stationary. The finger width is 15 μm and the spacing is 25 μm. (b) Comb drive is moving (note the blurriness of the left side of the comb drive) at resonance at 1933 Hz. The actuator is driven at just under breakdown at 360 Vpp. The fingers displace approximately 0.5°.

phenomena affect the electromechanical performance of the device, and are characterized.

To measure breakdown voltage and leakage current, a sample with multiple numbers of thermomigrated aluminum npn junctions was fabricated (Fig. 2). The aluminum-doped silicon regions are 100-μm-wide and separated by 500 μm of n-type silicon. Stainless steel probes were contacted to the n-type regions of the silicon. Current-voltage characteristics (from a Tektronix 370 A curve tracer) across each junction as well as across multiple junctions were measured.

An example I–V curve from one of the 12-npn junctions is shown in Fig. 3. The curve exhibits a breakdown voltage occurring at $\pm$140 V. At voltages less than breakdown, the leakage current is less than 10 μA.

There are several mechanisms for the voltage breakdown; however, the dominant effect for thermomigrated junctions, where one side is heavily doped and the other is lightly doped, is avalanche breakdown.

For avalanche breakdown, the breakdown voltage is inversely linear with doping concentration of the more lightly doped side. For TGZM fabricated npn junctions, the doping concentration of the p-doped region is set by the solid solubility limit of aluminum in silicon at the thermomigration temperature. At an average temperature of 1000 °C, the solid solubility limit of Al in Si is approximately 2×10^{19} cm^{-3}. In contrast, the n-doped region is set by the silicon wafer's manufacture. Wafers with extremely light doping concentrations may be purchased, with resistivities exceeding 100 Ω-cm. For 1 Ω-cm resistivity n-type silicon, the theoretical breakdown voltage is calculated to be 184 V [8]. This calculated figure is significantly higher than the measured 140 V. The difference is mostly due to fabrication nonidealities in these early test structures. Later TGZM fabricated structures exhibit breakdown voltages closer to the theoretical limit.

Multiple npn junctions arranged in series are tested to see if breakdown voltages increases across multiple junctions. Fig. 4 shows that the breakdown voltage increases roughly linearly with the number of npn junctions. Each npn junction contributes an average of 138-V breakdown voltage to the total, with a total breakdown voltage of -1550 and $+1450$ V for 12-npn junctions. Fig. 5 shows the I–V curve for 12-npn junctions. At voltages less than breakdown, the leakage current remained less than 10 μA.

Due to gradual refinements in the thermomigration process, junctions with breakdown voltages of 189 $\pm$37 V and leakage currents of 68 $\pm$8 nA have been fabricated. This would imply a direct current (dc) power dissipation of 12 μW. The increased breakdown voltage and decreased leakage current are primarily due to more vertical npn junctions and more complete removal of excess Al and heat damaged Si.

V. Actuator Demonstration

Using the aforementioned process, an actuator was fabricated to demonstrate the practical application of this technique to a bulk-micromachined, junction isolated, electrostatic actuator fabricated from a single silicon wafer. A scanning electron micrograph (SEM) of the front of the device is shown in Fig. 6 and a closeup of the thermomigrated region is shown in Fig. 7. The width of the aluminum-doped silicon region is 75 μm. The overall chip dimensions are 4.5 mm $\times$ 4.5 mm and the beam dimensions are 30μm$\times$ 1.5 mm $\times$ 200μm.

The actuator is a rotary device that is divided electrically into an inner and outer portion by the thermomigrated aluminum. Three of the four beams have two thermomigrated areas each. The fourth beam is electrically connected to the edge of the chip, and a region on the edge is electrically isolated from the rest of the chip by four thermomigrated areas (the top edge of the device in Fig. 6).

The actuator is composed of eight radial comb drives. The comb fingers are 15 μm in width with a gap of 25 μm.

The demonstration actuator is contacted on a probe station with a tungsten probe contacting the stator and another probe contacting the rotor (Fig. 8). The probes are driven by a Trek 50/750 high-voltage amplifier at 300 : 1 voltage amplification. The amplifier, in turn, is driven by an HP 33120 A function generator with a sinusoidal signal output. A Tektronix 2221 oscilloscope is connected in parallel to the probes to monitor the voltage across the demonstration device. The actuator is driven at resonance just under junction breakdown at 360 Vpp at 1933 Hz. At this voltage, the actuator displacement was measured optically to be approximately 15 μm at a radius of 1.5 mm ($\sim$0.5°).

A closeup of one of the fingers of the interdigitated electrostatic actuator is shown in Fig. 9. In Fig. 9(a), the finger is shown

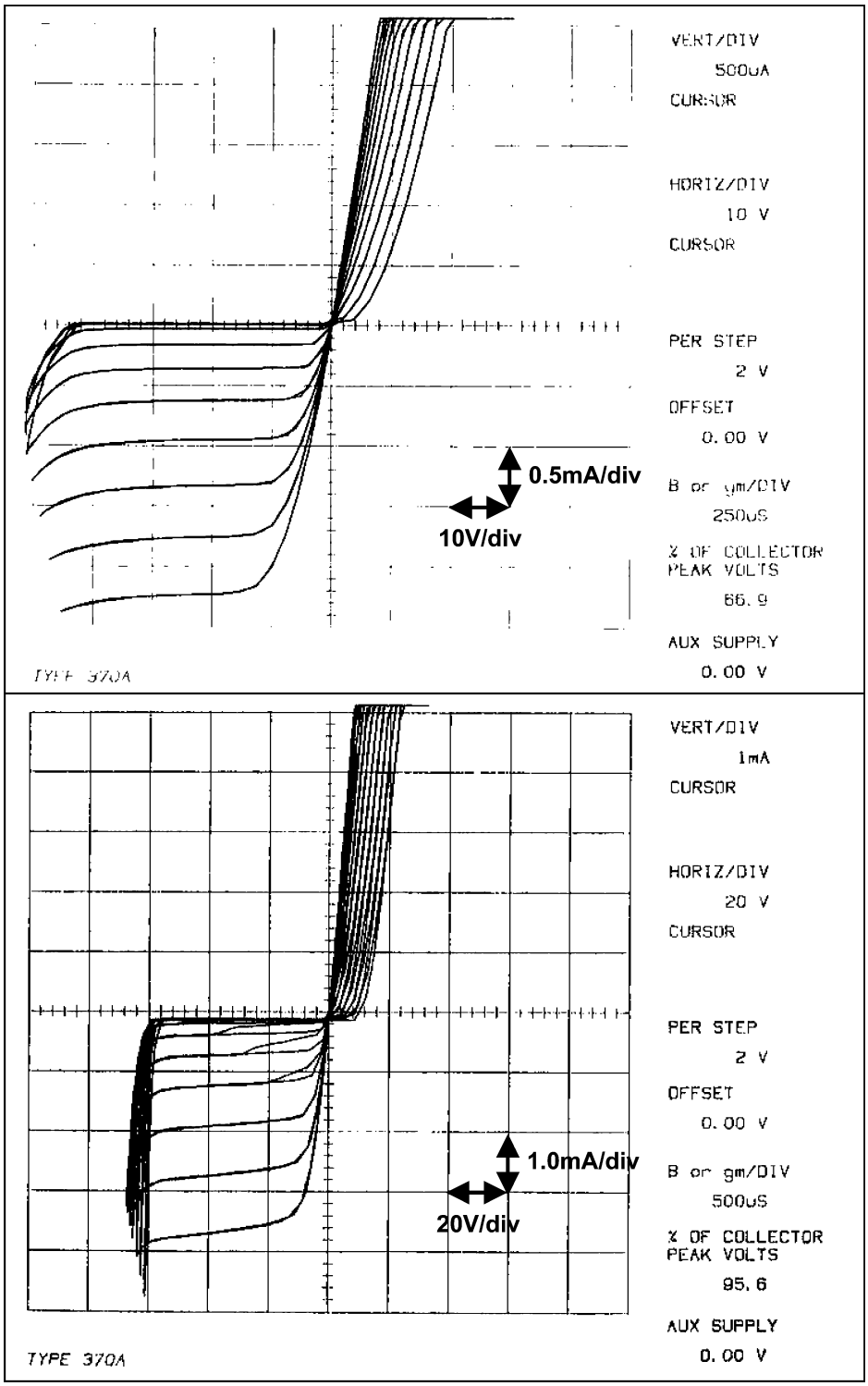

Fig. 10. I–V curves of a 40-μm-gate PMOS transistor before (top) and after (bottom) aluminum thermomigration. For the top I–V curves, the horizontal scale is 10 V/division, the vertical scale is 0.5 mA/division, and the step is 2 V. For the bottom I–V curves, the horizontal scale is 20 V/division, the vertical scale is 1 mA/division, and the step is 2 V.

with no voltage applied. In Fig. 9(b), the finger is shown moving at 1933 Hz (note the blurriness of the finger).

VI. Integrated Circuitry

The compatibility of the thermomigration process with integrated circuitry is also investigated. A silicon wafer with PMOS transistors of gate lengths ranging 40–90 μm is taken and the I–V characteristics of the devices are measured to record the transistor characteristics before the thermomigration process is performed [Fig. 10(a)]. The interconnect aluminum is removed using PAN etch since it melts and/or thermomigrates during the process. 1000 Å of chromium was evaporated to act as a mask for the etch that is needed after the thermomigration to remove the excess Al and heat damaged silicon. Windows are opened in

the Cr for the thermomigration regions. 5 μm of Al is then deposited on the wafer and patterned photolithographically. The PMOS wafer is then thermomigrated. After the thermomigration, the wafer was etched in $HF : HNO_3 : H_2O$ for 3 min to remove the excess Al and heat damaged Si. The Cr is then removed. 2500 Å of Al is redeposited on the wafer and repatterned to replace the previously removed Al interconnects between PMOS devices.

The I–V characteristics of the PMOS devices are remeasured [Fig. 10(b)]. The PMOS devices performed nearly identically after the thermomigration processing, demonstrating compatibility of the thermomigration process with integrated PMOS devices. It should be noted that the scales for the before and after I–V curves are different. The curve taken before thermomigration is 0.5 mA/unit in the y-direction and 10 V/unit in the x-direction, whereas the scale for the I–V curve taken after thermomigration is 1 mA/unit in the y-direction and 20 V/unit in the x-direction.

VII. Conclusion

The application of TGZM to the fabrication of npn junctions for junction isolation of bulk-micromachined SCS devices is demonstrated. The breakdown voltage and leakage current of the thermomigrated junction isolation are characterized. Breakdown voltage multiplication can be achieved by arranging multiple npn junctions in series. Practical demonstration of this technique is shown by fabricating an electrostatic rotary actuator. Compatibility of the TGZM process with PMOS devices is demonstrated.

Acknowledgment

The authors would like to thank the staff of Georgia Institute of Technology Microelectronics Research Center, Atlanta, GA. Prof. T. Kaiser of Montana State University contributed a great deal of advice and work to this research. Also, Millisensor Systems and Actuators (MSSA), Newton, MA, graciously lent their expertise on various aspects of this project. Finally, the authors would like to thank the Microsensor and Microactuator (MSMA) research group at the Georgia Institute of Technology, in particular R. Shafer for much of the work with filament evaporator.

References

[1] J. Bhardwaj and H. Ashraf, "Anisotropic dry silicon etching," presented at the Symp. Microstructures and Microfabricated Syst. Annu. Meeting Electrochem. Soc. Montreal, QC, Canada, May 4–9, 1997.

[2] Y. Gianchandani, K. Ma, and K. Najafi, "A CMOS dissolved wafer process for integrated p^{++} microelectromechanical systems," in *Proc. Tranducers '95*, Stockholm, Sweden, Jun. 25–29, 1995, pp. 79–82.

[3] L. Parameswaran, C. Hsu, and M. Schmidt, "A merged MEMS-CMOS process using silicon wafer bonding," in *Proc. Int. Electron Devices Meeting*, Washington, DC, Dec. 10–13, 1995, pp. 613–616.

[4] C. Gui, H. Jansen, M. de Boer, J. Berenschot, J. Gardeniers, and M. Elwenspoek, "High aspect ratio crystalline silicon microstructures fabricated with multi layer substrates," in *Proc. Tranducers '97*, Chicago, IL, Jun. 16–19, 1997, pp. 633–636.

[5] T. Brosnihan, J. Bustillo, A. Pisano, and R. Howe, "Embedded interconnect and electrical isolation for high-aspect-ratio, SOI inertial instruments," in *Proc. Transducers '97*, Chicago, IL, Jun. 16–19, 1997, pp. 637–640.

[6] K. A. Shaw, Z. L. Zhang, and N. C. MacDonald, "SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures," *Sens. Actuators A, Phys.*, vol. A40, no. 1, pp. 63–70, Jan. 1994.

[7] B. Streetman, *Solid State Electronic Devices*. Englewood Cliffs, NJ: Prentice-Hall, 1990.

[8] S. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[9] W. Pfann, *Zone Melting*. Huntington, NY: Krieger, 1978.

[10] T. R. Anthony and H. E. Cline, "Deep-Diode arrays," *J. Appl. Phys.*, vol. 47, no. 6, pp. 2550–2557, Jun. 1976.

[11] T. R. Anthony, J. K. Boah, M. F. Chang, and H. E. Cline, "Thermomigration processing of isolation grids in power structures," *IEEE Trans. Electron Devices*, vol. ED-23, no. 8, pp. 818–823, Aug. 1976.

[12] M. J. Little, R. D. Etchells, J. Grinberg, S. P. Laub, J. G. Nash, and M. W. Yung, "The 3-D computer," in *Proc. Int. Conf. Wafer Scale Integration*, 1989, pp. 55–64.

[13] P. Campbell, K. Jones, R. Huber, K. Horch, and R. Normann, "A silicon-based, three-dimensional neural interface: Manufacturing processes for an intracortical electrode array," *IEEE Trans. Biomed. Eng.*, vol. 38, no. 8, pp. 758–767, Aug. 1991.

[14] T. Johansson, M. Abbasi, R. J. Huber, and R. A. Normann, "A three-dimensional architecture for a parallel processing photosensing array," *IEEE Trans. Biomed. Eng.*, vol. 39, no. 12, pp. 1292–97, Dec. 1992.

[15] M. Abbasi, R. Johansson, and R. Normann, "Silicon-carbide-enhanced thermomigration," *J. Appl Phys.*, vol. 72, no. 5, pp. 1846–1851, Sep. 1992.

[16] D. Lischner, H. Basseches, and F. D'Altroy, "Observations of the temperature gradient zone melting process for isolating small devices," *J. Electrochem. Soc.*, vol. 132, no. 12, pp. 2997–3001, 1985.

[17] F. Laermer, A. Schilp, K. Funk, and M. Offenberg, "Bosch deep silicon etching: Improving uniformity and etch rate for advanced MEMS applications," in *Proc. IEEE Microelectromech. Syst.*, 1999, pp. 211–216.

Charles C. Chung received the B.A. degree in physics and environmental studies from the University of Pennsylvania, Philadelphia, in 1991, the M.A. degree in physics from Duke University, Durham, NC, in 1993, and the Ph.D. degree in electrical engineering from the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, in 2004. His Ph.D. field of study was the electrical isolation techniques for bulk micromachined MEMS devices and inertial navigation MEMS systems.

He is now at LV Sensors, a MEMS startup in the San Francisco bay area. His primary interests are in micro/nanosystems, particularly for high-volume applications and for space exploration.

Mark G. Allen (M'89–SM'04) received the B.A. degree in chemistry, the B.S.E. degree in chemical engineering, and the B.S.E. degree in electrical engineering from the University of Pennsylvania, Philadelphia, in 1984, 1984, and 1988, respectively, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, in 1989.

He joined the faculty of the Georgia Institute of Technology, Atlanta, in 1989, where he currently holds the rank of a Professor and the J. M. Pettit Professorship in Microelectronics. His research interests are in the areas of micromachining and MEMS, in particular the development and application of new fabrication technologies for micromachined devices and systems.

Prof. Allen was General Cochair of the 1996 IEEE MEMS Conference, and is North American Editor of the *Journal of Micromechanics and Microengineering*.