SILICON-EMBEDDED 3D TOROIDAL AIR-CORE INDUCTOR WITH THROUGH-WAFER INTERCONNECT FOR ON-CHIP INTEGRATION

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ABSTRACT

This paper presents a CMOS-compatible process for fabrication of 3D structures embedded in the volume of a silicon wafer, and capable of interconnection to circuitry on the wafer surface. The key challenge of embedding structures in the silicon substrate is processing inside deep silicon trenches. This difficulty is overcome by means of several key techniques: multilevel wafer etching; cavity shaping; fine proximity lithography at the bottom of trenches; and laminated dry-film lithography on complex 3D structures. As a technology demonstration, a topologically complex 3D toroidal inductor is fabricated in a deep silicon trench, and is coupled to the wafer surface with high-power, electroplated through-wafer interconnect. Inductors fabricated in these trenches achieved an overall inductance of 60 nH, dc resistance of 399 mΩ, and quality factor of 17.5 at 70 MHz.

INTRODUCTION

There has been continuing desire for increasing compactness and complexity in silicon systems, as well as integration of different components on a single wafer. Increased complexity has typically been achieved by means of advances in semiconductor manufacturing leading to larger and larger numbers of transistors on a single chip. As the semiconductor industry advances into the nanometer-scale regime, this approach is reaching its limit, necessitating advanced approaches such as through-silicon vias and chip stacking. However, the relatively large volume of the silicon wafer itself remains untapped. To take advantage of this unused volume, MEMS technology can be utilized to enable embedding of functional devices into the silicon bulk, and interconnects can be implemented to enable connection from these devices to the circuits on the wafer, as shown in Figure 1. For example, in applications such as power converters, the integration of magnetic components presents a major challenge for further system miniaturization. Embedding the inductors within the wafer volume and realizing high-power through-wafer interconnect is a promising technique for making ultra-compact DC-DC converters, in which digital control circuitry and power switches are located on the wafer surface, and suitable energy storage elements are located within the silicon substrate.

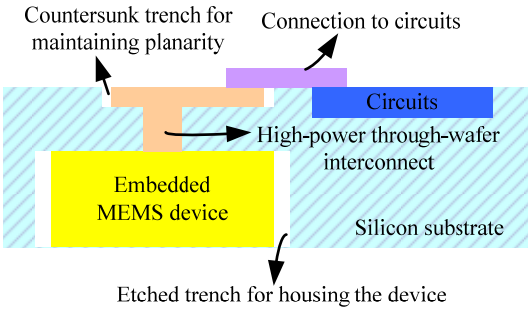


Figure 1: Schematic illustration of on-chip integration with embedded MEMS device.

In this paper, a CMOS-compatible process for fabrication of 3D structures embedded in the volume of a silicon wafer, and capable of interconnection to circuitry on the wafer surface, is demonstrated. A significant challenge in embedding the structure within the wafer volume is the difficulty of processing inside deep silicon trenches. This difficulty is overcome by means of several key techniques: multilevel wafer etching to form silicon trenches and vias; cavity shaping to facilitate uniform deposition of photoresist; fine proximity lithography to pattern at the bottom of trenches; and laminated dry-film lithography on complex 3D structures. As a technology demonstration, a topologically complex 3D toroidal inductor is fabricated in a deep silicon trench, and is coupled to the wafer surface with high-power, electroplated through-wafer interconnect, as shown in Figure 2.

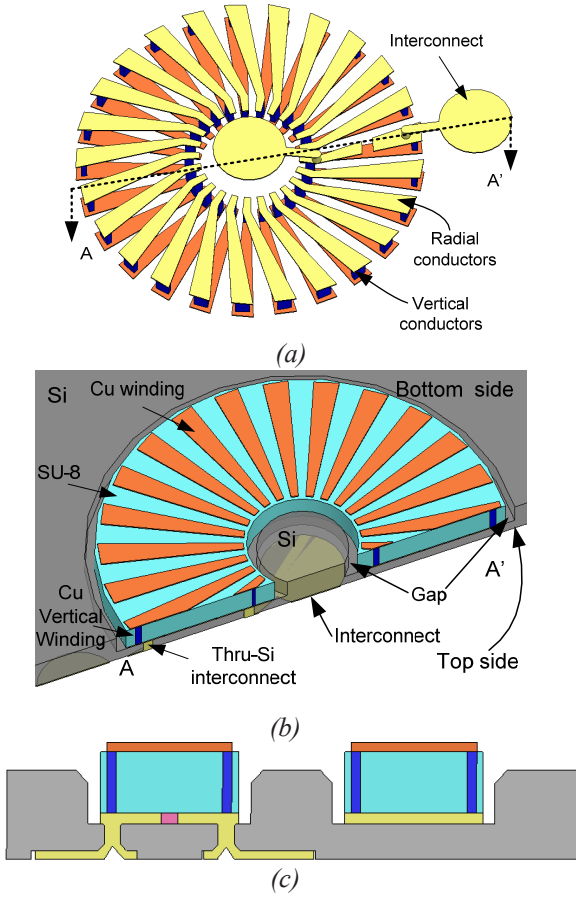


Figure 2: Schematic of the toroidal inductor design: (a) top-view with Si removed for illustration, (b) bottom-view with cross-sectional cut (Si substrate is drawn partially transparent in order to show the interconnect at the top side), and (c) cross-sectional view.

The silicon-embedding approach exploits the unused volume of the substrate to achieve further miniaturization. However, embedding inductors within conductive silicon may result in loss and/or resonance at high frequencies. A spiral inductor that was embedded in the silicon substrate with interconnect [1] exhibited only a limited quality factor due to substrate loss. Compared to spiral and solenoid inductors, toroidal inductors constrain the magnetic flux within a closed path, resulting in potential less loss in the substrate and less magnetic interference with other circuits.

Although surface-micromachined RF toroidal inductors that operate in the GHz range [2-4] have been successfully demonstrated, such structures do not take advantage of the silicon wafer volume. Furthermore, when considering next-generation power converter systems with operating frequency of 10-100 MHz, substantial conductor thicknesses in excess of those achievable by sputtering are beneficial. PCB-embedded or micromachined toroidal inductors shown in [5-6] have been demonstrated at lower operating frequencies, but have not been integrated into silicon. Previous efforts to embed toroidal inductors within the volume of silicon substrates [7-8] possess a shallow profile due to fabrication limitations and have a typical inductance of several nH. The toroidal air-core inductor fabricated here using the presented technology not only has densely-packed windings with deep profile to achieve high inductance within a small footprint, but also has conducting pathways for interconnection to circuitry.

FABRICATION

The detailed fabrication process is shown in Figure 3 with the images of fabricated devices shown in selected steps. For better illustration, the silicon wafer is drawn upside down throughout the entire process, and the top/bottom side of the wafer will be referred to as indicated in the figure.

Starting with a standard silicon wafer in step 1, a silicon trench of 300 µm depth is first etched from the bottom side of the wafer using a photoresist mask and the Bosch process in step 2. After stripping the photoresist, a double mask made of silicon dioxide and photoresist is then patterned for etching the through-silicon vias from the top side of the wafer in step 3. After removing the photoresist mask, countersunk silicon trenches for embedding the interconnect and testing pads are etched in step 4, with the entire structure completed after cleaning in step 5. Embedding the interconnect and pads helps to maintain a planar surface for trouble-free wafer handling, and rounded-off edges [9] are also formed through additional isotropic etching before and after the Bosch process to facilitate uniform coverage of spray-coated photoresist at the edges of the recesses.

After deposition of low-temperature PECVD oxide on both sides of the wafer, a blanket metal seed layer is sputtered into the deep silicon trenches and patterned at the trench bottom using a spray-coated photoresist mask in step 6. The spray-coating technique is essential in obtaining fine proximity lithography results at the bottom of the trenches as well as protecting the seed layer from being attacked at the rounded-off edges. In step 7, dry-film photoresist is first laminated and patterned on the top side of the wafer and seed layer is then sputtered to metalize the via sidewall as well as the interconnect trenches. By lifting off the dry film in acetone, a patterned seed layer for interconnect is obtained in step 8. This lift-off process guarantees a well-metalized via sidewall and compensates for any seed layer loss that was induced in the previous wet etching process due to imperfect photoresist coverage. Then with a spray-coated photoresist mold defined in step 9, the testing pads, through-wafer interconnects and the copper windings are formed simultaneously in a single electroplating step, and

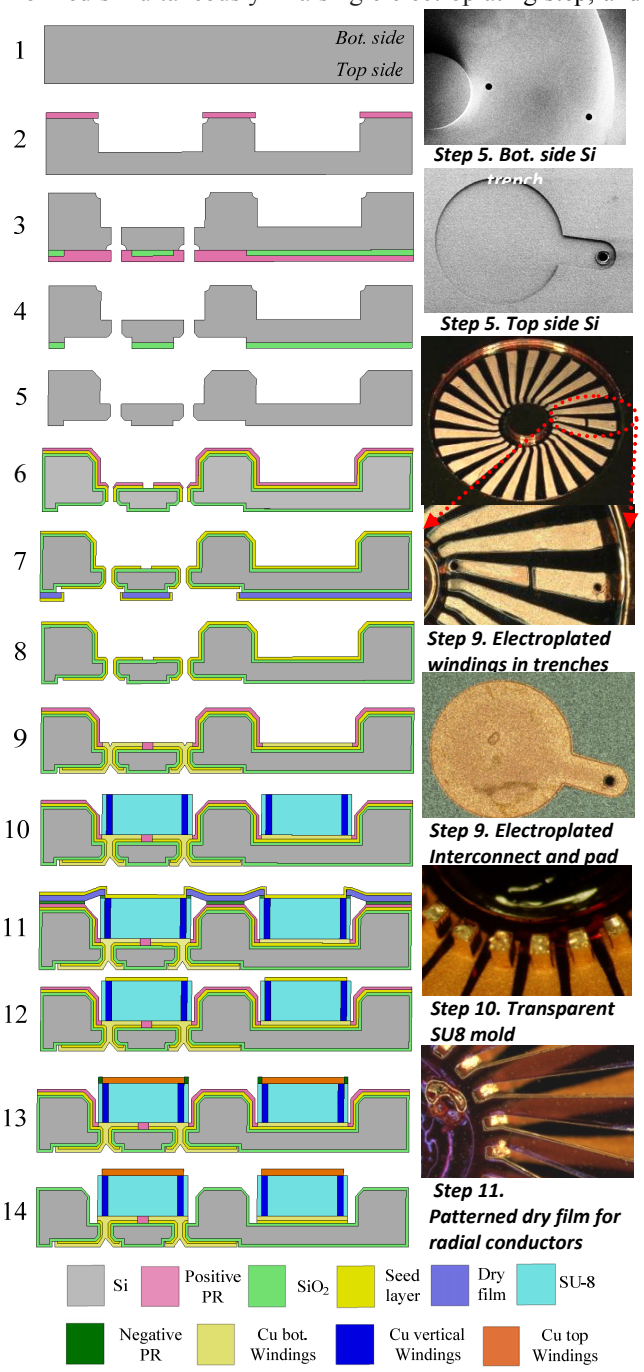


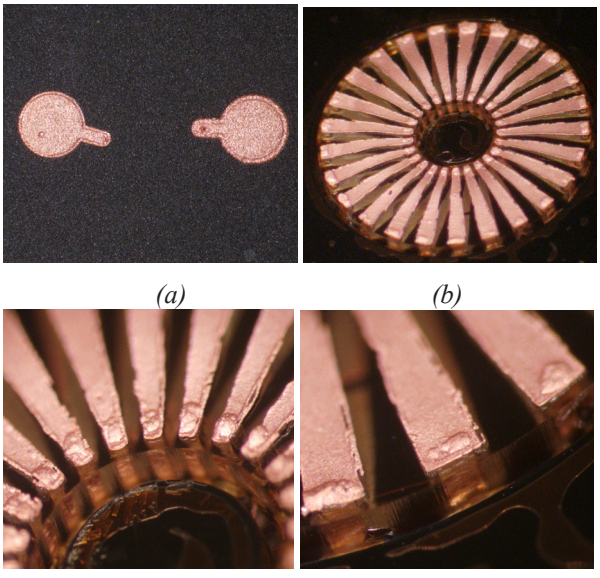
Figure 3: Fabrication process for 3D embedded toroidal inductor with SEM pictures and photomicrographs of the partially finished device in selective steps (substrate flipped upside down for illustration).

the photomicrographs of the electroplated structures on both sides of the wafer are shown.

After hard baking the photoresist layer, a layer of thick SU-8 is then cast and patterned in the deep silicon trenches in step 10. Electroplating follows to form the vertical conductors. To fabricate the radially-oriented conductors on top of the SU-8 mold, a laminated dry-film technique is employed to enable patterning of the seed layer on complex 3D surfaces in step 11. The dry film prevents the gap between the SU-8 mold and the silicon substrate, as shown in Figure 2(b), from being sputtered with metal layer, and the underlying photoresist layer is to facilitate a clean removal of the dry film during lift-off. The patterned seed layer is electrically connected through the vertical conductors to the bottom conductors, as shown in step 12, and the radial conductors are electroplated within a spray-coated photoresist mold in step 13, forming the conducting paths in the toroidal inductor. At the end, the device is isolated and completed after removing the photoresist left from step 9 using oxygen plasma and etching the seed layer in step 14. Images of a completed device are shown in Figure 4, with a birds-eye view from both sides of the wafer as well as the close-up view on some of the winding details.

TESTING RESULTS

Electrical characterization of the fabricated inductor is performed with an impedance analyzer (HP4194) by probing the interconnect pads shown in Figure 4(a), and the results are plotted in Figure 5. The toroidal inductor demonstrated a low-frequency inductance of 109 nH and a dc resistance of 1.3 Ω, proving the capability of thepresented technology for embedding functional devices in the silicon substrate with interconnects. However, the quality factor is limited at high frequency as shown in Figure 5(b), which is due to the sharply decreased inductance value above 10 MHz. To understand this, a preliminary estimation on the parasitic capacitance of the device is conducted.

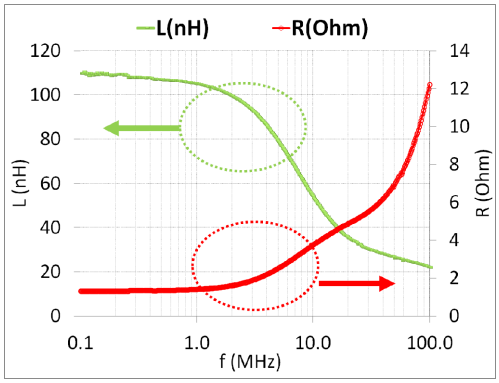


(a) *(b)* *(c)* *(d)*

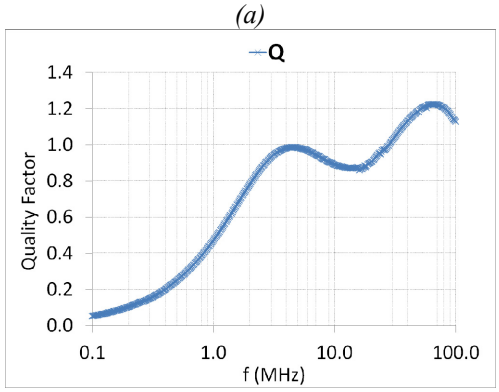
Figure 4: Fabricated 3D toroidal inductors embedded in the silicon substrate, with birds-eye view from wafer top side (a) and bottom side (b), and close-up view on the inner(c) and outer (d) copper windings.

The two major contributors to the parasitic capacitance are: the capacitance generated between the vertical conductors and the silicon substrate with mainly an air medium, and the capacitance coming from the radial conductors in contact with the silicon substrate with a layer of silicon dioxide in between. By estimating the area of the conductors, and the distance between conductors and the substrate, the parasitic capacitance generated from the two sources is calculated to be approximately 0.2 pF and 180 pF respectively. The summation of them leads to a resonant frequency of approximately 35 MHz with an inductance of 109 nH presented, which is in accordance with the decreasing trend observed in the inductance vs frequency curve shown in Figure 5(a).

To confirm the effect of the parasitic capacitance, embedded inductors without interconnect are also fabricated. A partial releasing of the inductor is then performed, such that the inductor is still within the silicon trench, but an air gap is introduced between the bottom radial windings and the silicon substrate, thus reducing the main contributor to parasitic capacitance. From the results shown in Figure 6, the partially released inductor within the trench achieves a quality factor of 17.5 at 70 MHz with an overall inductance of 60 nH, and a dc resistance of 399 mΩ, while the unreleased inductor only has a maximal quality factor of 4 at 10 MHz. This

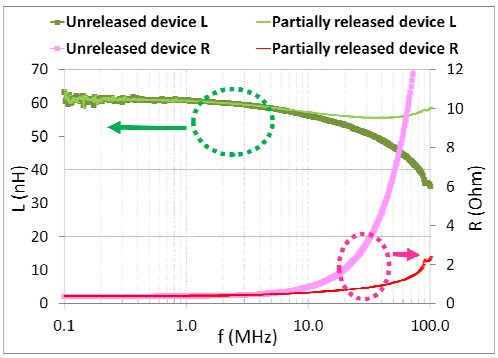


(a)

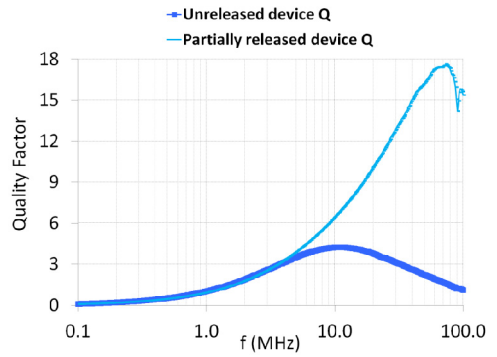


(b)

Figure 5: Measured inductance and resistance (a), and quality factor (b), of the fabricated inductor with through-wafer interconnect. The inductor possess a height of 420 µm, an outer diameter of 8 mm, an inner diameter of 4 mm, a conductor thickness of 20 µm and 50 turns.



(a)



(b)

Figure 6: Measured inductance and resistance (a), and quality factor (b), of fabricated inductors, illustrating the effect of partial release. The inductors possess a height of 400 µm, outer diameter of 6 mm, inner diameter of 1.5 mm, conductor thickness of 20 µm, and 25 turns.

suggests a way to improve the quality factor of the integrated inductor by reducing the parasitic capacitance, either through implementing this partial release into the process, or by increasing the thickness of the dielectric layer that isolates the bottom radial windings from the silicon substrate.

CONCLUSIONS

A CMOS-compatible process for embedding 3D structures in deep silicon trenches is presented and through-wafer interconnect is realized for connecting the device to the potential circuits that sit on the wafer surface. Toroidal inductors with interconnects are fabricated as a technology demonstration, which favors the ultimate on-chip integration of power converter systems. Further optimization on the fabrication process, such as increasing the insulation layer thickness, or partially releasing the devices within the cavity, can be conducted to improve the inductor performance.

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