Silicon-Embedding Approaches to 3-D Toroidal Inductor Fabrication

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***Abstract*—This paper presents complementary-metal–oxide–semiconductor-compatible silicon-embedding techniques for on-chip integration of microelectromechanical-system devices with 3-D complex structures. By taking advantage of the "dead volume" within the bulk of the silicon wafer, functional devices with large profile can be embedded into the substrate without consuming valuable die area on the wafer surface or increasing the packaging complexity. Furthermore, through-wafer interconnects can be implemented to connect the device to the circuitry on the wafer surface. The key challenge of embedding structures within the wafer volume is processing inside deep trenches. To achieve this goal in an area-efficient manner, straight-sidewall trenches are desired, adding additional difficulty to the embedding process. Two approaches to achieve this goal are presented in this paper, i.e., a lithography-based process and a shadow-mask-based process. The lithography-based process utilizes a spray-coating technique and proximity lithography in combination with thick epoxy processing and laminated dry-film lithography. The shadow-mask-based process employs a specially designed 3-D silicon shadow mask to enable simultaneous metal patterning on both the vertical sidewall and the bottom surface of the trench during deposition, eliminating multiple lithography steps and reducing the process time. Both techniques have been demonstrated through the embedding of the topologically complex 3-D toroidal inductors into the silicon substrate for power supply on-chip (PwrSoC) applications. Embedded 3-D inductors that possess 25 turns and a diameter of 6 mm in a silicon trench of 300-μm depth achieve overall inductances of 45–60 nH, dc resistances of 290–400 mΩ, and quality factors of 16–17.5 at 40–70 MHz. [2012-0187]**

***Index Terms*—Deep-trench patterning, silicon-embedding, spray coating, toroidal inductor, 3-D shadow mask.**

I. Introduction

As semiconductor scaling begins to approach ultimate limits, advanced approaches such as chip stacking and system-in-package/system-on-package [1]–[4] have been developed to enable integration of multiple chips or components into a single package for continued system multifunctionality and miniaturization. In many of these approaches, the relatively large volume of the silicon bulk compared with the active volume of the circuitry, even in thinned wafers, remains untapped. To take advantage of this "dead volume" in the wafer, silicon-embedding approaches can be utilized to enable fabrication of functional devices into the silicon bulk, and through-wafer interconnects can be implemented to enable connection from the embedded device to the circuitry on the wafer surface, achieving the ultimate chip-scale integration, as shown in Fig. 1. This silicon-embedding approach, as compared with other integration schemes of 3-D structures such as surface micromachining of the devices on or beside the circuits [5]–[9], offers additional system miniaturization, which is particularly beneficial when the system profile is a major concern.

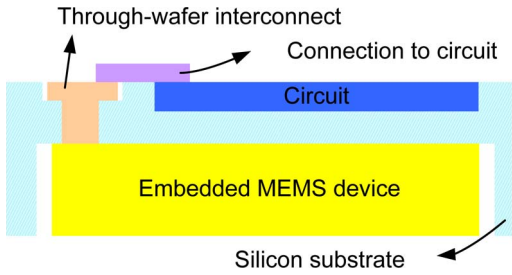

Fig. 1. Illustration of a chip-scale integration scheme with a MEMS device embedded in the wafer volume and connected to the circuitry on the wafer front surface using through-wafer interconnects.

The silicon-embedding approach has found application in integrating many microelectromechanical-system (MEMS) devices and structures such as accelerometers [5], permanent-magnet microgenerators [10], interconnects and copper circuitry [11], [12], magnetic components for power applications [13]–[17], hall sensor [18], and microfluidic devices [19]. In [10], the authors proposed a manual drop-in method to embed prefabricated stator windings into a preetched silicon trench with preelectroplated interconnects folded and threaded through silicon trenches for realization of a silicon-embedded microgenerator. Although this technique avoided the difficulty of processing inside silicon trenches with complex silicon features, the drop-in approach is a manual serial process. The creation of devices directly inside the silicon trenches with batch-fabrication-compatible technology, although challenging, needs to be addressed. To date, most of the published research has focused in embedding 2-D structures into the silicon substrate due to their less complex geometry and ease in fabrication process [11], [12], [16], [17]. Significant challenges remain in embedding complex 3-D structures with deep profile into the silicon. An additional challenge is introduced

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when the constraint of vertical, rather than sloped, trench walls is imposed to maximize the area efficiency of the embedding process.

Generally, two techniques have been demonstrated for patterning on or within 3-D recessed surfaces, i.e., a spray-coating technique with proximity lithography and a shadow-mask method. The spray coating of photoresist has been well studied and reported to generate well-patterned features, for example, in KOH/TMAH etched trenches [14], [22]. The trenches are formed with slanted sidewalls to enable pattern definition on the sidewall, which could lead to a trench opening as much as seven times the size of the bottom of the trench [14], increasing the footprint of the device. With vertical sidewalls, patterning typically requires tilting of the structures when using this method due to the strong vertical directionality of the ultraviolet light.

Shadow masking can be also used for patterning in trenches. Traditional shadow masks are usually 2-D planar structures that are aligned and attached to the device wafers to define metal patterns during evaporation [12], [18]. This approach is challenging for deeply recessed surfaces because of the pattern blurring introduced due to the gap that exists between the planar shadow mask and the recess. Recently, 3-D silicon shadow masks that possess self-aligning mechanical structures have been demonstrated to enable fine feature patterning in deep recessed surfaces [19]–[21]. However, the margins between the drop-in mask and the trench sidewalls do not favor the use of conformal deposition methods such as sputtering. The directional evaporation method required multiple sample tilts during deposition as well when the vertical trench walls needed to be coated [20].

As an example of a technology that could greatly benefit from embedded 3-D structures, consider dc–dc power converters designed for ultracompactness, resulting in an integrated power supply on chip (PwrSoC) [7]. These converters, comprising digital control logic, power electronic switchers, and magnetic storage elements, can be utilized not only as small standalone chargers for portable electronics but also as indispensible components of compact electronic systems requiring multiple voltage levels. The requirements of such devices, in addition to compactness, include reasonably large power handling capability, as well as shielding of stray magnetic fields that might influence other portions of the converter or system. In accordance with Fig. 1, such a PwrSoC could be realized by forming the switches and the control logic on the wafer front surface while forming the 3-D magnetic energy storage element and high power interconnect within the wafer volume.

In this paper, two approaches for embedding complex 3-D structures into deep silicon trenches with vertical sidewalls are pursued based on the development of the aforementioned lithography-based technique and 3-D shadow-mask technique, respectively. These processes allow for conformal metal deposition, as well as patterning along vertical sidewalls. A process for incorporating through-wafer interconnects is also presented to enable connection from the device to the circuitry on the wafer surface.

As a technology demonstration, topologically complex 3-D toroidal inductors are fabricated and embedded in the silicon substrate using both approaches, with through-wafer interconnects also demonstrated. Since toroidal inductors constrain the magnetic flux within a closed path in contrast to the substrate-penetrating magnetic field that spiral inductors generate, potentially less magnetic interference will be imposed on other circuits, and complex shielding techniques can be bypassed. The flux containment offered by toroidal inductors may be particularly important in ultracompact converters, in which the physical separation of components is minimized.

PCB-embedded toroidal inductors for megahertz operation [23], [24] and surface-micromachined toroidal inductors that operate in the gigahertz range [25] have been successfully demonstrated, yet such structures do not take advantage of the silicon wafer volume. Previous efforts to embed toroidal inductors within the volume of the silicon wafer [13], [14] possessed a shallow profile due to fabrication limitations and achieved low inductance values that are more suitable for RF application. When considering next-generation integrated power converter systems with an operating frequency of 10–100 MHz, high inductance and conductor thickness in excess of those achievable by RF inductors are required. In this paper, the toroidal inductors fabricated by the presented technologies not only have densely packed electroplated windings but also a deep profile embedded in silicon to achieve high inductances and low resistances.

II. Inductor Fabrication

A. Lithography-Based Silicon Embedding

The lithography-based process combines a spray-coating technique with thick epoxy processing and dry-film lithography on nonplanar surfaces to enable creation of complex 3-D structures in deep silicon trenches. A schematic of the embedded inductor design is shown in Fig. 2. Structures are defined in the etched trench using spray coating and fine proximity lithography. Patterning on the vertical sidewalls is avoided by processing thick SU-8 to form a mold for housing the vertical conductors. An air gap must be maintained between the SU-8 mold and the sidewall to facilitate seed layer removal, which isolates the windings at the end of the fabrication process. The complete process flow for realizing the embedded inductor is shown in Fig. 3 [15] with scanning electron microscopy (SEM) images and optical photomicrographs of the partially fabricated devices also presented for selected steps. The interconnect scheme is temporarily ignored here as it will be introduced later. For better illustration, the silicon wafer is drawn upside down throughout the entire process, and the front and back sides of the wafer will be referred to as indicated in Fig. 3.

Referring to Fig. 3, fabrication begins with a standard 4-in silicon wafer in step 1, whose thickness is 500 μm and resistivity is in the range of 1–10 Ω cm. A silicon trench of 300-μm depth and 2-mm width is first etched into the back side of the wafer through the Bosch inductively coupled plasma process as shown in step 2. A cavity-shaping technique is utilized to form rounded-off edges during the etching to facilitate the uniform coverage of spray-coated photoresist on the vertical sidewalls [11]. After deposition of 6-μm-thick plasma-enhanced chemical vapor deposition (PECVD) oxide as insulation layer and metal sputtering, spray coating of photoresist, proximity

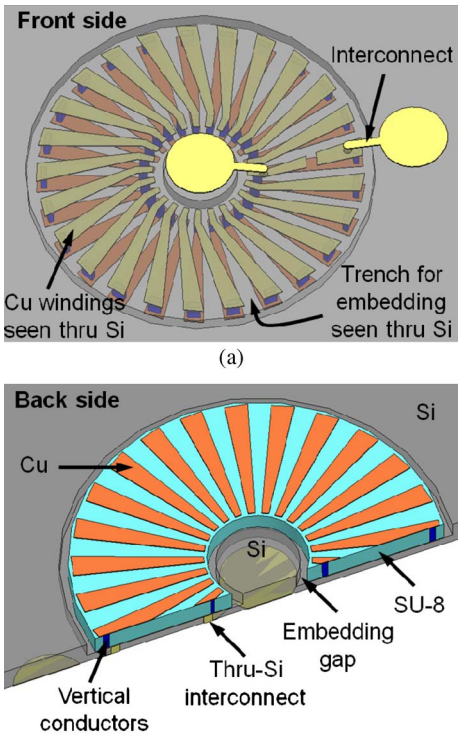

Fig. 2. Schematic of the embedded 3-D toroidal inductor using lithography-based approach. (a) Wafer front side with silicon substrate drawn partially transparent and SU-8 epoxy removed to illustrate the embedded structures; and (b) wafer back side with cross-sectional cut.

lithography, and wet etching are performed to obtain a patterned seed layer for radial windings on the recessed bottom surface of the trench in steps 3 and 4. With a spray-coated photoresist mold defined again in step 5 to protect the metallized trench sidewalls and wafer surface, 20-μm-thick radial copper conductors are electroplated. After hard baking the photoresist, thick SU-8 is then cast and patterned in the trench, followed by electroplating to form the vertical conductors in step 6. To fabricate the radial conductors on top of the SU-8 mold, a laminated dry-film technique is employed to generate a patterned seed layer through a liftoff process on the complex 3-D surface, as shown in steps 7 and 8. The dry film prevents the gap between the SU-8 mold and the silicon substrate from being sputter coated, which would be otherwise challenging to remove due to the narrow gap. An additional patterned photoresist layer under the dry film facilitates the clean removal of the dry film in acetone, as shown in step 7. The top radial conductors are then formed by electroplating in step 9, and the device is completed after removing the protection photoresist layer using oxygen plasma and etching away the underlying seed layer in step 10.

Photomicrographs of a fabricated inductor with 25 turns are shown in Fig. 4 with electrical testing pads located on one radial conductor that is intentionally separated into two pieces. The minimum gap between two adjacent copper conductors in the inner diameter of the inductor is approximately 120 μm, and the vertical conductors buried in SU-8 at the inner diameter are 125 μm by 160 μm in area. The inductor embedded in the trench is approximately 100 μm higher than the silicon surface due to the fact that SU-8 has to be cast thicker to enable reflowing and planarization across the substrate during baking.

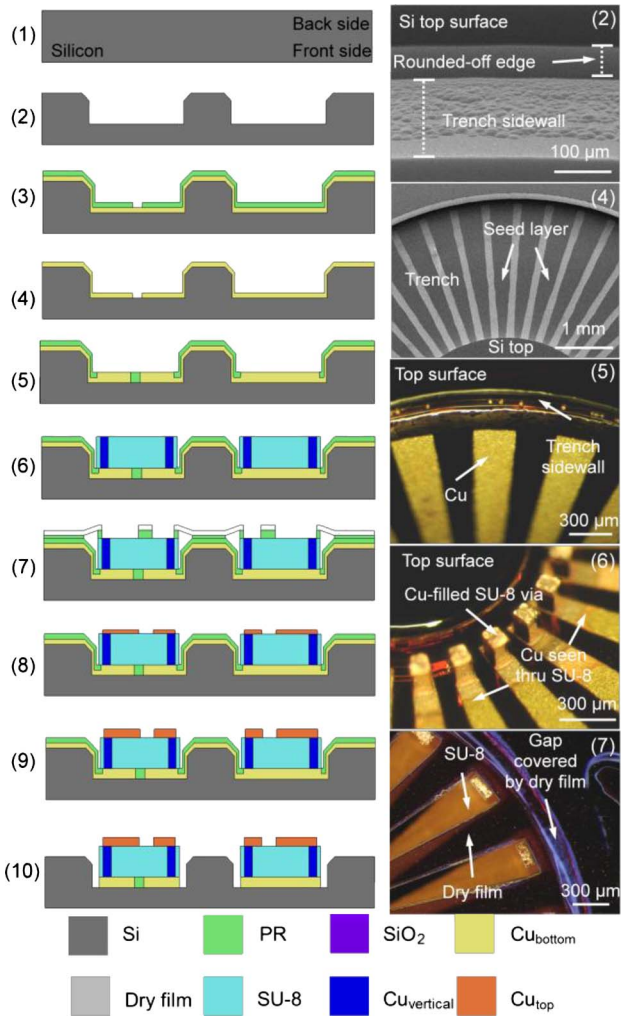

Fig. 3. Fabrication process of the toroidal inductor using the lithography-based silicon-embedding approach with results of partially completed devices also shown in critical steps. Steps 1 and 2: Silicon etching; 3: proximity lithography; 4: seed layer patterning; 5: bottom radial conductor fabrication; 6: vertical conductor fabrication; 7: dry-film patterning; 8: seed layer liftoff; 9: top radial conductor fabrication; 10: seed layer etching and device completion. Features are not drawn to scale.

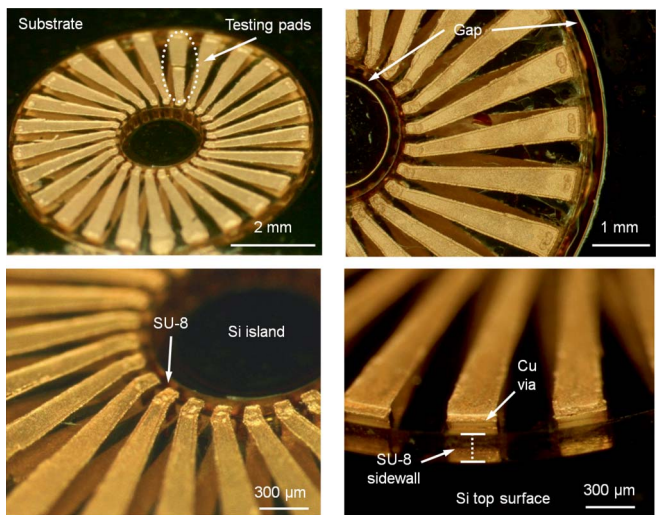

Fig. 4. Fabricated inductor embedded in silicon using the lithography-based approach.

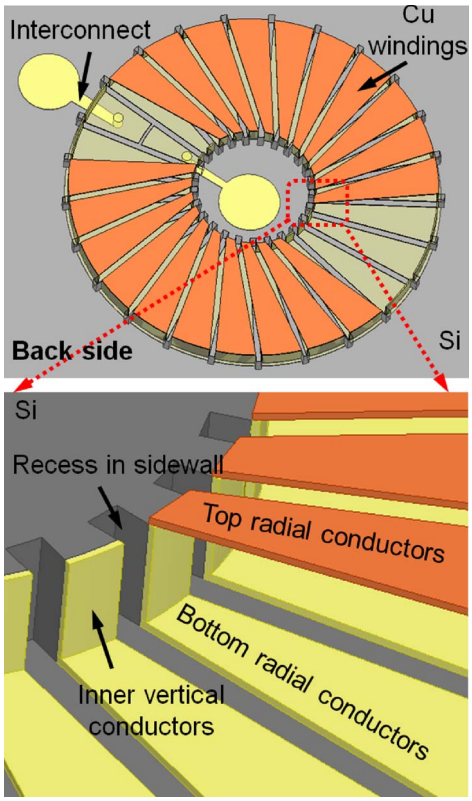

Fig. 5. Schematic of the embedded 3-D toroidal inductor using the 3-D shadow-mask-based approach. Bottom view of wafer back side. Some radial conductors are removed for illustration, and silicon substrate is drawn partially transparent to show the through-wafer interconnects on the front surface of the wafer.

B. Shadow-Mask-Based Silicon Embedding

The shadow-mask process utilizes a specially designed 3-D silicon shadow mask that is formed through multilevel wafer etching to realize the direct patterning of the metal layer on both the vertical sidewall and the bottom surface of the deep trench. Moldless electroplating can then follow to form the 20-μm-thick copper conductors as required. The benefit of this approach is that plating can occur along the entire vertical sidewall, as well as the bottom surface of the trench simultaneously. The process time of the shadow-mask method is significantly reduced compared with the lithography-based approach due to the elimination of several lithography steps, thick epoxy processing steps, and use of moldless electroplating. The inductor resulting from this approach possesses a slightly different embedding geometry compared with the lithography-based approach, as shown in Fig. 5. The vertical conductors sit directly on the passivated sidewalls of the silicon trench with no air gap introduced between them and are isolated from each other automatically by the recesses etched into the vertical trench sidewalls. Using this approach, the upper surface of the fabricated inductor can be maintained coplanar with the back side of the wafer.

In the shadow-mask approach, conformal metal deposition (sputtering) is utilized in order to obtain a uniform and thick seed layer on all exposed areas (bottom and side) of the deep trench. However, sputtering could introduce severe pattern

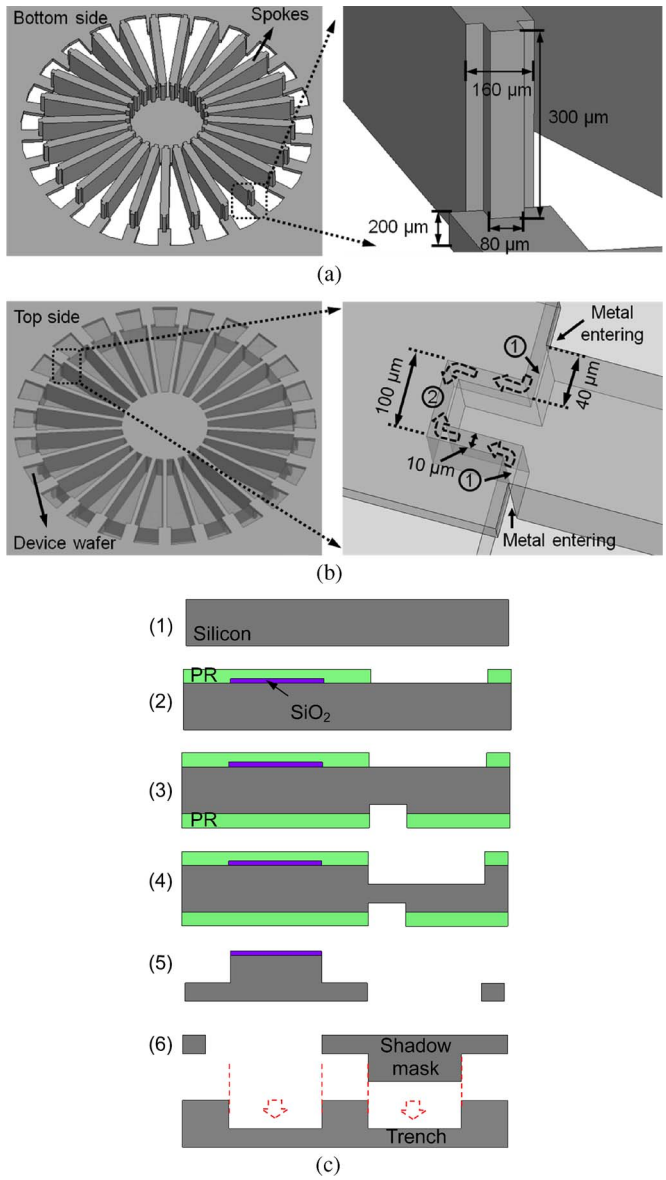

Fig. 6. Schematic of the designed 3-D shadow mask: (a) Bottom view of the mask with details of the 3-D spoke structure, (b) top view of the mask after insertion into the device wafer with magnified view of the registration scheme, and (c) fabrication process. The portion of the shadow mask that covers regions 1 and 2 in the magnified view of (b) is drawn partially transparent for illustration.

blurring due to the nondirectional characteristic of the sputtered metals and the intrinsic margins that exist for registering and inserting the shadow mask into the device wafer. Thus, special features on the shadow masks and device wafers are designed to ensure clean pattern definition after seed layer sputtering.

The fabrication process of the shadow-mask-based approach proceeds in two parts. First, the shadow mask is designed and fabricated; then, the shadow mask is applied to the inductor fabrication. It should be noted that the shadow mask, once fabricated, can be reused.

The design and registration schematic of the shadow mask, as well as its fabrication process, is presented in Fig. 6. The multiple spokelike structures, when looking from the bottom side of the shadow mask, as shown in Fig. 6(a), are designed to fit into

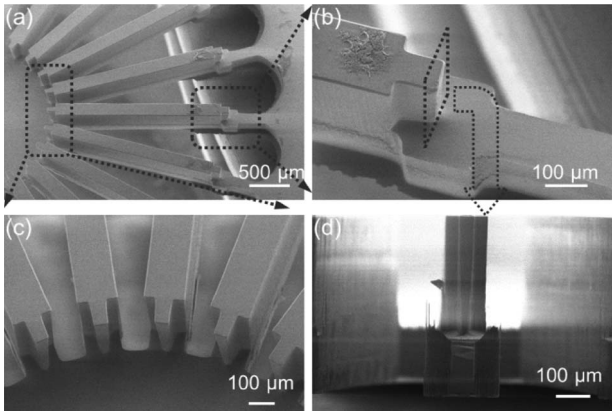

Fig. 7. SEM images of the fabricated 3-D silicon shadow mask. (a)–(c) Tilted view and (d) side view of the spoke structure.

the trench and define the isolation gaps between adjacent copper conductors. The protruding ends on the spokes, as shown in the magnified views, are designed to match the recesses etched into the vertical sidewalls of the trench. The underlying mechanism, as shown in Fig. 6(b), is that the tortuous path between regions 1 and 2 prevents the sputtered metals from entering the recess, keeping region 2 free of any metal deposition, and thus ensures isolation between the to-be-formed vertical conductors on the trench walls. In addition, the protruding ends on the spokes also act as alignment marks during registration and insertion of the shadow mask into the device wafer.

The detailed process for fabricating the 3-D silicon shadow mask is as follows [see Fig. 6(c)]. Starting with a standard 4-in wafer that is 500 μm thick in step 1, a double-layer mask consisting of oxide and photoresist are first formed through wet etching and photolithography in step 2. The photoresist acts as a mask for etching 200-μm silicon into the wafer, as shown in step 4, which defines the thickness of the connection framework in the shadow mask, and the oxide mask is used to etch 300-μm silicon to form the spokes, as well as the open area in the mask that allows metals to be deposited through, as shown in step 5. A shallow Bosch etching step is conducted in step 3 to compensate for the lower etch rate [due to deep reactive-ion etching (DRIE) lag] of the small patterns at the inner diameter of the inductor. This is critical as nonuniformity-based overetching of the spokes and the framework may result in overly fragile structures. After stripping the oxide in step 6, the silicon shadow mask is ready for use. SEM images of the fabricated 3-D silicon shadow mask are shown in Fig. 7.

Once the shadow mask has been completed, inductor fabrication can commence. The complete process flow for fabricating the embedded inductors using the premanufactured shadow mask is illustrated in Fig. 8 with micrographs of partially completed devices also shown in selected steps. Starting with a standard 4-in wafer that has a thickness of 500 μm and a resistivity in the range of 1–10 $\Omega \cdot$ cm in step 1, a silicon trench with vertical sidewalls and recesses in the sidewalls is first formed using the Bosch process as shown in step 2. After deposition of a passivation layer such as PECVD silicon dioxide, the prefabricated 3-D shadow mask is then aligned with and inserted into the trench using a flip-chip bonder (Finetech

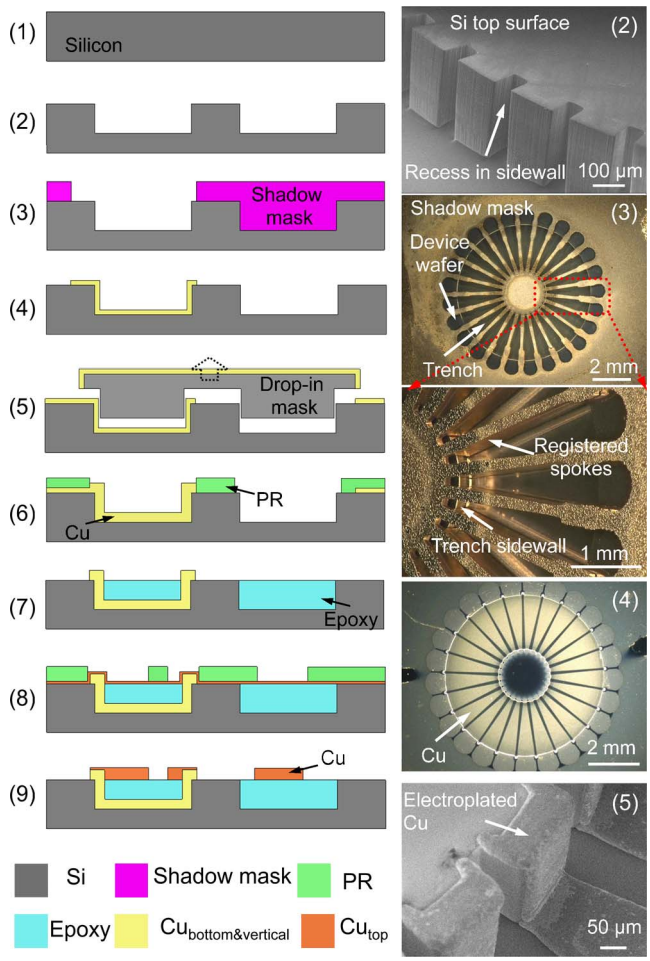

Fig. 8. Fabrication process of the embedded toroidal inductors using the 3-D shadow-mask-based approach with results of partially completed devices also shown in critical steps. Features are not drawn to scale. Steps 1 and 2: Silicon etching; 3: shadow-mask registration; 4 and 5: seed layer patterning; 6: bottom radial and vertical conductor formation; 7: epoxy filling; 8: photoresist mold for electroplating; 9: top conductor formation.

Fineplacer Lambda) in step 3. The shadow mask is placed on the bonder stage while the device wafer is positioned on the bonder arm. The wafer is aligned with the shadow mask and brought into contact with the mask using a force of 3 N. This force was found to allow complete insertion during successful alignment but not to cause device or mask damage even in the case of misalignment and insertion failure. Tape-based adhesive is temporarily applied after mask insertion to maintain the contact between the mask and the device wafer and is removed once the metal deposition is completed. The alignment accuracy of the bonder is 0.5 μm, and the registration margins between the shadow mask and the device features are designed to be 10 μm, well within the aligner tolerances. To guarantee a well-defined metal pattern, the height of the spokes in the shadow masks must match with that of the trench within a maximum error of 70 μm, which is achievable since the depth of the Bosch etching can be accurately controlled. A thick layer of Ti/Cu (1 μm) is sputtered into the trench, and the subsequent physical removal of the shadow mask results in this layer being patterned, as shown in step 4. To electrically connect the seed layer patterned in individual trenches for subsequent electroplating, a second

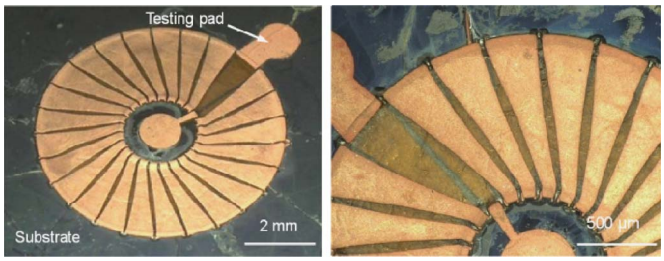

Fig. 9. Fabricated inductor embedded in silicon substrate using the 3-D shadow-mask-based approach.

thin metal deposition (3000 Å) is conducted by dropping in individual silicon donut structures to mask the trench area in step 5. In step 6, spray-coated photoresist is then defined to protect the wafer surface, and electroplating is performed to obtain the 20-μm-thick copper conductors in the trench, from sidewalls to the bottom surface. After photoresist stripping and seed layer removal in step 7, premolded solid epoxy donuts are dropped into the silicon trench and melted at a temperature of 120 °C to prepare a planarized surface for top conductor fabrication. After evaporation of a seed layer and photoresist patterning in step 8, electroplating follows to form the top radial conductors. The fabrication process concludes by stripping the photoresist and etching away the seed layer in step 9.

Since there is no gap between the vertical copper conductors and the trench walls in the embedding design, no complex dry-film technology is needed for the fabrication of the top radial conductors as used in the lithography-based process. In addition, the uncrosslinked epoxy in the trench can be easily removed if required [26], resulting in a true air-core inductor. Photomicrographs of the fabricated inductors are shown in Fig. 9 with two circular pads of 500 μm in diameter designed for probing and electrical testing. The gap between the top radial conductors gradually widens from the inner and outer edges of the trench to the middle to facilitate timely and uniform etching of the seed layer after electroplating. Well-patterned radial conductors with a constant gap of 100 μm at the bottom surface of the silicon trench can be clearly observed through the transparent epoxy.

C. Process Discussion

By using well-established conventional techniques, the lithography-based approach enables batch fabrication and offers great design and fabrication flexibility. In this approach, there are no techniques that are specific to the inductor device. Therefore, the same set of techniques can be potentially applied to fabricate other devices with device-oriented adjustments. Furthermore, devices with different embedding depths can be also realized from batch to batch without changing the masks.

However, due to the processing of thick SU-8 epoxy that is needed in forming a mold for the vertical copper conductors, the lithography-based approach is more time-consuming. In addition, tens of hours are required to fill such a thick mold using bottom–up electroplating.

In the shadow-mask approach, the vertical conductors are simultaneously formed with the bottom radial conductors during one metal deposition and one 20-μm-thick copper electroplating step, eliminating multiple lithography steps, the thick SU-8 patterning process, and the bottom-to-top filling of the SU-8 vias. Although the fabrication of the shadow mask does take time, the shadow mask can be reused to produce many device wafers. Therefore, the overall processing time of the shadow-mask approach is greatly reduced compared with that of the lithography-based approach. The fact that this process is less complex may also lead to a higher yield of devices under nonideal fabrication conditions and less performance degradation due to fabrication limitations.

While the shadow-mask approach offers great benefit in reducing the process time, care has to be taken to ensure high processing quality in forming the shadow masks. Any dirt or residues that are not removed from the wafer surface during processing steps prior to DRIE will act as masks in the etching and generate defects that prevent the shadow mask from being in intimate contact with the device wafer. In addition, the number of the devices that can be put in one shadow-mask wafer is also limited by the fragility of the wafer. Since the thickness of the silicon framework connecting individual shadow masks is determined by the wafer thickness and the height of the spokes, the deeper the silicon trench, which is desirable for higher inductance, the taller the spokes, and thus, the thinner the silicon framework (the framework is 200 μm thick in this paper). Therefore, the shadow-mask wafer can become increasingly fragile with an increasing number of devices incorporated. To address this problem, a reinforcing outer frame can be designed to help strengthen the shadow-mask wafer. For demonstration in this paper, six shadow masks are fabricated in a 100-mm-diameter wafer with a reinforcing outer frame that has the original substrate thickness. The robustness of the outer frame greatly facilitates mask handling, insertion, and removal. Fabricated shadow-mask wafers have been reused over 30 times without failure. Furthermore, it should be emphasized that this process is batch-fabrication compatible, as six devices are simultaneously fabricated with a single mask insertion. Denser packing, smaller devices, or larger area substrates would lead to greater batch sizes.

III. Interconnect Integration

In order to electrically connect the embedded toroidal inductors to circuitry on the front side of the wafer for a PwrSoC application, through-wafer interconnects can be implemented. The interconnect technique proposed here is compatible with both silicon-embedding approaches and can be integrated into the inductor fabrication process as shown in Fig. 10.

The steps from the original inductor process are labeled with the same numbers as before, and the added steps for fabricating the through-wafer interconnects are leveled in alphabetical order. After silicon trenches are formed in step 2, through-silicon vias and countersunk trenches for embedding the interconnects on the front side of the wafer can be then etched using a patterned photoresist mask and an oxide mask, respectively, as shown in steps (a)–(c). After forming the patterned seed layer in the trench in step 3, the metallization of the interconnect trenches is completed through sputtering and liftoff of dry-film

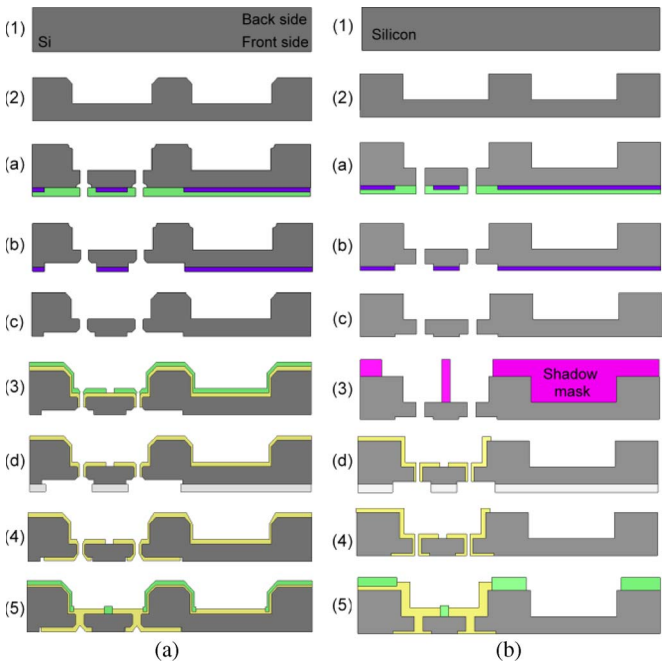

Fig. 10. Process integration of through-wafer interconnects with (a) lithography-based approach and (b) shadow-mask-based approach. Added steps for fabricating the interconnects are labeled in letters with the original steps labeled in numbers as previously shown.

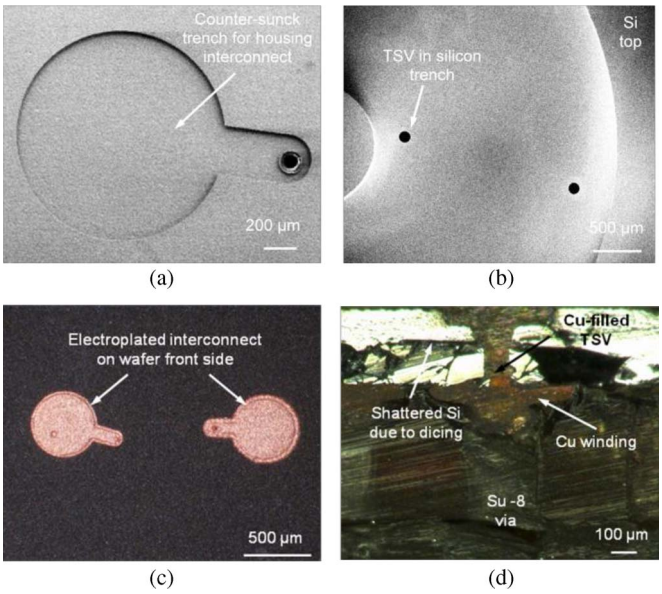

Fig. 11. Through-wafer interconnects. (a) Front and (b) back sides of the structured silicon prior to electroplating. (c) Front side and (d) cross section of the completed through-wafer interconnects with a partially completed embedded inductor.

photoresist as shown in step (d). With a patterned seed layer obtained in step 4, through-wafer interconnects and testing pads are simultaneously formed with the radial copper conductors as shown in step 5. The remaining steps for fabricating the inductors are the same as discussed before and will not be repeated here. Results of the fabricated interconnects are shown in Fig. 11 with SEM images of the etched through-silicon vias and microphotographs of the completed interconnects.

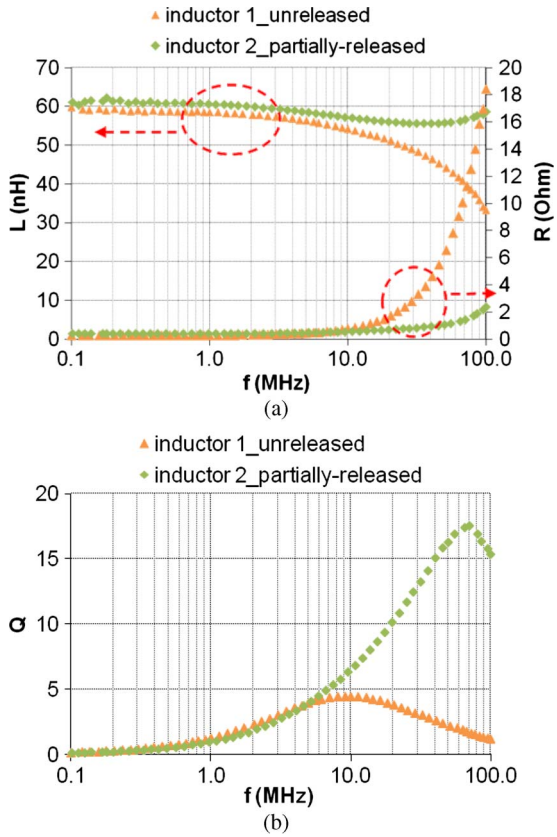

Fig. 12. Measured L, R, and Q of the embedded toroidal inductors from the lithography-based approach. The inductors have 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 400 μm, and a 6-μm-thick oxide insulation layer.

IV. Characterization Results

The electrical characterization of the embedded inductors is performed with an impedance analyzer (HP4194) in the frequency range of 100 kHz to 100 MHz. Results of the fabricated inductors from the lithography-based approach are shown in Fig. 12 and compared with an inductor that is partially released in the trench in order to reduce the capacitive coupling between the device and the substrate. The partial releasing is achieved through an abrupt heating and cooling cycle such that the inductor is still embedded in the silicon trench, yet an air gap is introduced between some of the bottom radial windings and the silicon substrate. An inductance of 60 nH, a dc resistance of 400 mΩ, and a quality factor of 4.5 at 10 MHz is measured for a completed inductor with 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 400 μm, and a 6-μm-thick oxide insulation layer, as shown in Fig. 12. By suppressing the capacitive coupling effect using partial release, the inductor quality factor improves from 4.5 at approximately 10 MHz to 17.5 at approximately 70 MHz.

Upon verifying the significant effect of parasitic capacitance, inductors with a 12-μm-thick oxide insulation layer are fabricated using the shadow-mask-based approach. The inductor had a height of 300 μm, and other geometric parameters were maintained the same as for the lithography-based inductors. The characterization results, as shown in Fig. 13, demonstrate an overall inductance of 45 nH, a dc resistance of 290 mΩ,

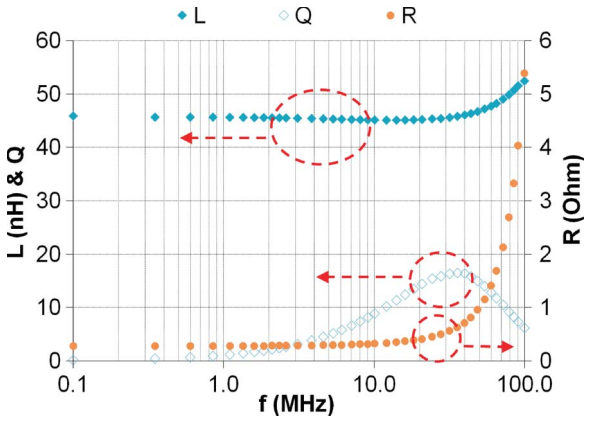

Fig. 13. Measured L, R, and Q of the embedded toroidal inductor from the shadow-mask approach. The inductor has 25 turns, an inner diameter of 2 mm, an outer diameter of 6 mm, a height of 300 μm, and a 12-μm-thick oxide insulation layer.

TABLE I
COMPARISON OF THE MEASURED INDUCTANCE AND QUALITY FACTOR OF VARIOUS SILICON-EMBEDDED INDUCTORS

Reported work	Type	L(nH)	Q_{max}@freq
This work	Toroid	45-60	16-17.5@40-70 MHz
Liang[13]	Solenoid	3.3	17.8@4.5 GHz
Gu[14]	Toroid	9.06	17.8@3.3 GHz
Yu[15]	Toroid	60	4@10 MHz
Wu[16]	Planar	15.8	5.5@16 MHz
Pan[17]	Planar	2000	60@30 MHz

and a quality factor of 16 at 40 MHz. The improved quality factor, compared with 4.5 of the unreleased inductor with thin insulation layer, further demonstrates the importance of parasitics minimization. The inductor from the lithography-based process exhibits a higher inductance because of the taller profile that was fabricated. Table I compares the measured inductance and quality factor of the fabricated inductors in this paper with the results of silicon-embedded inductors from literature. Both flux-confined (e.g., toroidal) and nonflux-confined (e.g., solenoidal and planar) geometries are shown.

The integration of through-wafer interconnects with embedded inductors is also demonstrated using the lithography-based approach as an example. The fabricated device had an inductance of 110 nH and a dc resistance of 1.3 Ω for an inductor with 50 turns and a diameter of 8 mm [15].

V. CONCLUSION

Complementary-metal–oxide–semiconductor-compatible processes for embedding 3-D complex structures in deep silicon trenches with vertical walls has been presented, and through-wafer interconnect has been realized to demonstrate the potential to electrically connect the device to circuitry on the wafer surface. Two approaches have been developed for the silicon-embedding process, i.e., a lithography-based approach that combines spray coating technique and thick epoxy processing with dry-film technique, and a shadow-mask-based approach that employs a 3-D silicon shadow mask to enable direct metal patterning on the vertical sidewalls of the trench. The successful fabrication of embedded 3-D toroidal inductors has been demonstrated with the characterization results that have been presented. Although these fabrication approaches have been demonstrated with the application goal of embedding inductors for ultracompact PwrSoC, these concepts can be extended to integrating other MEMS devices into the substrate as well, such as resonators, sensors, RF filters, and microfluidic devices.

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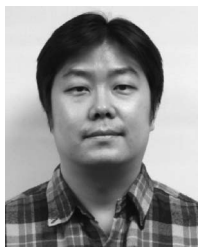

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