SILICA HERMETIC PACKAGES BASED ON LASER PATTERNING AND LOCALIZED FUSION BONDING

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ABSTRACT

We develop a hermetic package process based on laser machining that simultaneously achieves dicing and localized fusion bonding of stacked, patterned bulk silica wafers; this process enables rapid hermetic encapsulation of foundry CMOS/MEMS. Because of the extremely low thermal diffusivity of fused silica, as well as the localized and controllable nature of the laser spot illumination, the interwafer molten bond line penetrates less than 200 microns laterally into the device, sparing the CMOS chip the extreme heat of fusion bonding. Metallic feedthroughs can be incorporated without compromising the hermeticity of the package. Furthermore, excimer laser patterning of fused silica prior to bonding had 100x shorter processing time than patterned wet etching. Such fused silica hermetic packages have many favorable attributes; for example, the excellent chemical inertness enables biocompatibility, and the transparency at radio and optical frequencies enables wireless transmission through the package.

INTRODUCTION

Hermetic packaging of electronic circuitry for signal processing and transmission of biocompatible sensors and actuators is extremely challenging. The packaging should attain long-term hermeticity to provide the electronic circuitry with protection from the harsh environment of the human body. Simultaneously, the package material should be biocompatible so that human body is compatible with the package [1]. The packaging approach should optionally support feedthroughs to provide connection between the circuits and the sensors without compromising the hermeticity of the package. Finally, transparency to energy such as optical or RF signals are beneficial for energy harvesting and data transmission.

In order to achieve long-term hermeticity, packages made from glass, ceramic or metal are preferred [2]. Fused silica, which is transparent to light and RF signals, largely chemically inert, and biocompatible, is an attractive choice. Further, the availability of this material in wafer form facilitates its use in standard micromachining processes such as lithography, wafer bonding, and laser machining.

Bonding of multiple patterned wafers is a potential approach to encapsulation of functional electronic systems such as MEMS and CMOS. Common silica wafer bonding methods include anodic, glass frit, eutectic, reactive and fusion bonding [3,4]. Although fusion bonding is considered the most robust, its overall high temperature requirements may induce thermal issues, such as potentially damaging the enclosed systems. Adhesion bonding with polymer or solder materials may be utilized, at the expense of long term hermeticity [5]. The process presented here achieves localized fusion bonding of fused silica wafers without damaging encapsulated devices.

Metal feedthroughs on glass have been implemented using glass frit to immobilize metal wires extending through a glass shell; this approach was widely used in vacuum tubes. Temperatures above 400 °C are typically required even with low melting point glass. To maintain compatibility with batch fabrication techniques, this work explores the use of electrodeposited feedthroughs and their influence on the hermeticity of the package.

Multiple approaches to hermeticity assessment have been employed, including helium fine leak testing; gross bubble testing; radio-isotope testing; Raman spectroscopy; and Fourier transform infrared spectroscopy [6]. Many of these approached require relatively complex instrumentation; further, as packages shrink, hermeticity testing becomes more challenging.

A simpler testing method is to obtain the pressure or moisture information inside the package by encapsulating a pressure or humidity sensor. Water vapor, in particular, is of great concern as it can cause corrosion and ultimately device failure. Previous researchers encapsulated a humidity sensor into the package and wirelessly transmitted the sensor data for hermeticity test [4, 7]. In our design, a digital humidity sensor is encapsulated and data is obtained directly from the sensor by wire connection with feedthroughs, allowing a simultaneous test of the bonded package and the metallic feedthroughs.

PACKAGING METHOD

Overall Design

Figure 1 illustrates the packaging approach, comprising: 1) a fused silica base substrate (6×6×0.7mm) with a cavity and providing multiple feedthroughs and connection pads underneath; 2) a humidity sensor connected with the feedthroughs of the base substrate; 3) a cover fused silica (6×6×0.7mm) wafer with a cavity and bonded with the base substrate. The overall dimension of the package is 6×6×1.4mm.

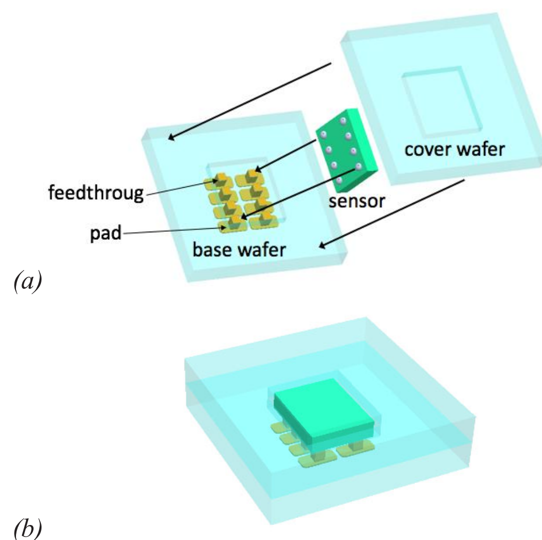

Figure 1: Schematic of package (a) package structure, (b) ensemble view.

The silica wafers are patterned using excimer laser patterning and the pads are defined by optical lithography. These wafers are stacked, cavities within the layers are optionally populated with CMOS chips, and the stack is Van der Waals bonded. Laser dicing of individual devices from the stacked wafers results in localized wafer-to-wafer fusion bonding at the edges of the device.

Excimer Laser Patterning on Fused Silica

An excimer laser (IPG IX-255, wavelength 193 nm) is utilized to ablate cavities in the fused silica; since the frequency of the excimer UV transmission is sufficiently energetic to break the chemical bonds of the material, thermal effects are minimized [8]. To pattern a 350 μm deep cavity in a package of this lateral extent, this excimer laser requires 3 minutes – 100x faster than the deep etching using concentrated HF at rate of 1.1 μm/min [9]. In addition, laser processing is maskless and results in a more anisotropic wall profile.

Localized Fusion Bonding with CO_2 Laser

Direct bonding of fused silica can be achieved by contacting a pair of the cleaned wafer surfaces at room temperature without external pressure, since hydrogen bonds form between Si-OH groups present on each of the hydrophilic surface. Thermal anneals would further increase the bonding strength by converting Si-OH groups into Si-O-Si bonds [10].

Localized thermal treatment can be realized with a carbon dioxide (CO_2) laser (PLS4.75, wavelength 10.6 μm). This laser is able to cut fused silica very well due to high photon absorption at this frequency. The high power density of the CO_2 laser results in rapid heating, melting and partial or complete vaporization of the material [11]. By proper balance of the laser power and cutting speed, localized fusion bonding and contour definition can be accomplished simultaneously. Localized fusion bonding of the cover wafer and base wafer at temperatures exceeding 1000 °C results in strong bonding at the interface [12].

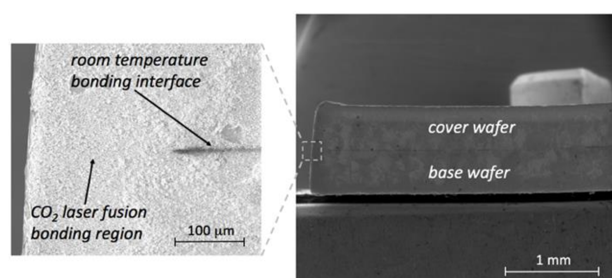

Figure 2: Cross sectional views of two fused silica wafers which were Van der Waals bonded and subsequently laser diced. Note that the interface between wafers disappears in the vicinity of the laser diced edge.

Figure 2 illustrates this process by means of bonding two fused silica wafers, each of 500 μm thickness. Initially the wafers are Van der Waals bonded at room temperature, and possess a distinct bond line. Dicing using the CO_2 laser is then performed. Complete fusion bonding with no distinguishable bond line is observed in the vicinity of the laser diced edge. Further from the diced edge, the original bond line is still present, suggesting a significant falloff in temperature as distance from the dicing line increases. This temperature falloff, due in part to the very low thermal diffusivity of fused silica, could be exploited to encapsulate thermally sensitive parts sufficiently far from the localized fusion bond.

Thermal Simulations

To determine the temperature distribution of the fused silica during the laser dicing and fusion process, as well as identify regions within the package that remain sufficiently cool to allow damage-free encapsulation, a COMSOL multiphysics simulation is performed. Size parameters of the package are selected so as to identify minimum sized packages in which temperatures do not exceed CMOS compatibility limits during fusion bonding. The overall thickness of the package depends in part on the device to be encapsulated; to ensure robustness, a design rule is adopted such that a minimum silica thickness of 300 μm is utilized for all areas of the package. (For example, if a 400 μm deep cavity is machined into a silica wafer, a total silica wafer thickness of 700 μm is required.) This thickness in turn informs laser cutting parameters and therefore the minimum distance from the edge of package to the encapsulated device.

In Figure 2, it is shown that using laser parameters of 100 % power and 3 % speed of this particular CO_2 laser, dicing of the wafer stack in a single pass with a laterally fused extent of 180 μm is achieved. Taking the diced edge as x=0, this experimental result suggests that the silica temperature was maintained at its melting point during the laser dicing between x=0 and x=180 μm, and fell below this temperature for x>180 μm. These parameters were used as input to the simulation. The dimensions of the fused silica were 6×6×1.4mm. Other material properties and parameters used in the simulation: thermal conductivity: 1.2 W/m·K, density: 2.65×10^3 kg/m^3, heat capacity: 755 J/kg·K and beam duration (calculated from lateral cutting speed and spot size): 0.03s. A thermal diffusion simulation shows the temperature of the fused silica falls to 500 K at a distance from the edge x=670 μm, as shown in Figure 3.

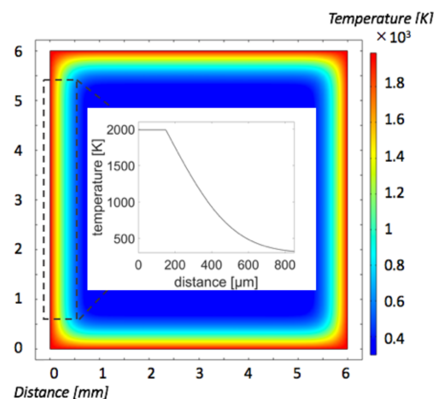

Figure 3: Heat diffusion over the package resulting from laser dicing. At the edge is a 180 μm wide molten region and the temperature deceases further into the center. The low thermal conductivity of fused silica slows heat propagation; at a distance of 670 μm from the edge, the temperature has fallen to less than 500 K.

FABRICATION PROCESS

The fabrication process is based on the combination of standard lithography and fused silica laser patterning and dicing. The process is comprised of four steps: (1) electrodeposition of copper as the pad for wire connection; (2) fabrication of cavity and blind vias with excimer laser and filling the feedthrough with copper electroplating; (3) fixation and soldering of the sensor to be encapsulated within the silica package; and (4) localized laser-based fusion bonding and dicing of the cover and base wafers.

Fabrication begins with deposition of a 30 nm titanium and 200 nm copper seed layer on the bottom of the base wafer. Lithographically patterned negative photoresist KMPR1050 is utilized as the mold for the electroplating of a 40 μm thick copper pad (Figure 4(a), (b)). The pattern of the copper pad is defined by the pads layout of the target digital sensor (HDC1008, TI, 2.04×1.59×0.675mm) which has eight solder-ball-terminated leads. Each pad is 900 μm × 400 μm with spacing of 100 μm. To facilitate subsequent soldering, seven extension pads of 1 mm × 200 μm are designed since one of the leads is not necessary for testing, as shown in Figure 5(b).

Excimer laser patterning in high fluence mode follows to form a partial chip encapsulation cavity (2.3×1.9×0.35 mm). Subsequently, feedthroughs of 250×250 μm are etched by excimer laser through the cavity until reaching the copper pad. The laser patterning induces a bump at the edge due to the redeposition of material during the ablation. This redeposition effect can be reduced by applying a thin film of ProtectoLED film prior to laser ablation; post-ablation removal of the film also removes any redeposited material. After film removal, the post-ablation bump is approximately 0.5 μm, and can optionally be removed completely by a 10 minute fluorine-based dry etch. The bottom of the base wafer is then covered with photoresist and copper electroplating is used to selectively fill the feedthroughs to a thickness of 350 μm (Figure 4(c), (d)).

To connect and stabilize the encapsulated sensor, solder paste is applied on top of the electroplated copper of feedthrough inside the base wafer. The sensor is placed into the cavity and the base wafer is heated to 220 °C on a hot plate in order to melt the solder paste and connect the sensor and the feedthrough (Figure 4(e)).

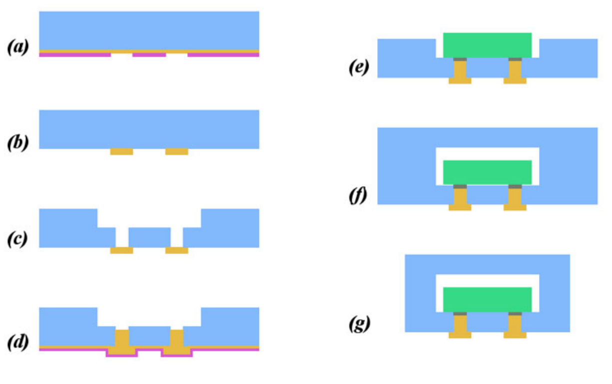

Figure 4: Fabrication process of hermetic package

A cover wafer is fabricated using similar processes to form a recess (2.3×1.9×0.35 mm) partially through its thickness to accommodate the sensor to be encapsulated. The cover wafer and the base wafer are then Van der Waals bonded at room temperature. (Figure 4(f)). Finally, the CO_2 laser is utilized to simultaneously dice the package and locally fuse the multilayer stack at the edges (Figure 4(g)).

Figure 5 shows the silica-encapsulated humidity sensor chip with feedthroughs. The smallest rectangle in the middle is the sensor under the cover wafer and the copper pads on the bottom can also be seen from the top view since the silica is transparent (Figure 5(a)). From the bottom view, there are eight pads with seven extended areas for later soldering and connection. On the extension areas, there are holes to prevent the delamination during fusion bonding due to the difference of the thermal expansion coefficient between copper and fused silica (Figure 5(b)). Cross section views demonstrate that the two wafers are molten at the interface and fused, as shown in Figure 5(c). Figure 5(d) shows the feedthroughs are completely filled with copper, with feedthrough spacing of 500 μm.

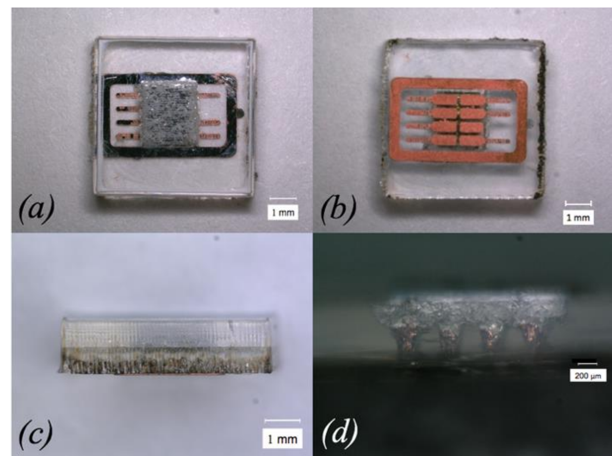

Figure 5: (a) Top view, (b) bottom view: 8 pads and 7 extended pads are fabricated, (c) cross view: two 700 μm thick wafers are stacked and the total thickness is 1.4 mm, (d) feedthrough detail: four feedthroughs are shown with 500 μm spacing.

HERMETICITY TESTING

In order to demonstrate sensor functionality and package hermeticity post-fusion, wires are soldered to the external package pads. A microcontroller MSP430F149 and peripheral circuit is applied to provide a clock and data signal for the IIC interface with the encapsulated digital sensor, and an oscilloscope is utilized to detect the output signal. In this way, the humidity change inside the package can be read directly from the sensor.

The package is held in an 85% humidity and 24 °C environment, and the humidity monitored as a function of time. Figure 6 shows the humidity information inside the package versus time over 78 days. A linear regression suggests the average humidity increase rate is under these conditions is 0.070 %/day, equivalent to a water vapor leakage rate of 6.40×10^{-14} atm·cc/sec. Given the accuracy of the humidity sensor is ± 4%, longer time testing will give a more accurate result.

The initial relative humidity inside the package is approximately 55% since the packaging process was

performed in open air. Several methods could be employed to reduce this initial humidity, including performing the initial bonding in vacuum or controlled environment, or utilizing getters to remove initial moisture further reduce the effects of any water vapor ingression.

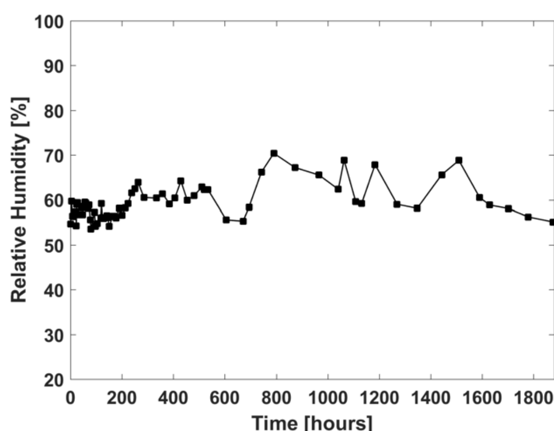

Figure 6: Hermeticity testing.

CONCLUSIONS

We hermetically packaged a commercial humidity sensor (HDC1008, TI) with eight electrical feedthroughs of 250×250 μm, spacing 500 μm, inside a locally fusion bonded, fused silica micromachined package. The encapsulated sensor and feedthroughs are functional after the localized fusion bonding. To determine the minimum safe distance between the fusion edge and CMOS, calculation and COMSOL simulation are performed. A minimum fusion edge to chip edge distance of 670 μm is required to maintain a CMOS-compatible temperature at the chip; this distance could be further reduced by, e.g., optimizing the package size and thickness, as well as considering multiple pass dicing at reduced power levels. Hermeticity testing was performed at 1atm, 85 % relative humidity, 24 °C. Given the small package volume, and the resolution of the humidity sensor, the water vapor leak rate could not have exceeded 6.40×10^{-14} atm·cc/sec, a promising indicator of hermeticity.

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