

Polymer-Core Conductor Approaches for RF MEMS

Yong-Kyu Yoon, *Member, IEEE*, Jin-Woo Park, and Mark G. Allen, *Senior Member, IEEE*

Abstract—In many radio frequency (RF) microelectromechanical systems (MEMS) applications, currents are confined to the outermost portions of conductors due to the skin effect. Conductors consisting of polymer cores coated with metal, the so-called *polymer-core conductor*, are appropriate to consider for these applications, and in many instances are easier to fabricate than their solid-metal-core counterparts. Implementation of polymer-core conductors using an SU-8 epoxy patterning and subsequent metal electrodeposition is reported. The SU-8 core approach allows for relatively simple formation of extremely high-aspect-ratio columns for inductor sidewalls. In addition, an SU-8 bridge fabrication technique has been realized using a double exposure and single develop scheme. The bridge thickness has been characterized as a function of the optical dose and the post bake time in an oven. Three-dimensional, high-aspect-ratio, high Q-factor, solenoid-type RF inductors are fabricated and tested to demonstrate the feasibility of the polymer-core conductor approach for RF applications. A single, vialess metallization over SU-8 back-bone structure provides the complete conducting paths of the inductor. A single turn inductor that is 900 μm in height and 600 μm in lateral extension shows a maximum Q-factor of 84 and an inductance of 1.17 nH at 2.6 GHz. [1382]

Index Terms—Double-exposure-single-development, epoxy-core conductor, high-aspect-ratio solenoid inductor, polymer-core conductor, radio frequency (RF) microelectromechanical systems (MEMS), SU-8 bridge fabrication.

I. INTRODUCTION

IT IS KNOWN that as frequency increases, an electromagnetic wave propagating through a good conductor attenuates quickly in the depth direction of the conductor and the resultant electric current flows through the outermost portion of the conductor. The distance where the electromagnetic wave reduces in amplitude by a factor of $1/e$ is called the skin depth δ defined in (1).

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \quad (1)$$

where ω (rad/sec) is the angular frequency of the electromagnetic wave, μ (H/m) is the permeability of the conductor, and σ (S/m) is the electrical conductivity. Thick radio frequency (RF) transmission lines or RF conductors have little benefit for electrical resistance reduction with thickness greater than several skin depths. For example, a hollow conductor whose conductor thickness is greater than a few skin depths (usually five skin depths) is considered electrically equivalent to the solid conductor where outer diameters of both conductors are the same as shown in Fig. 1. Thus, as long as the metal coating

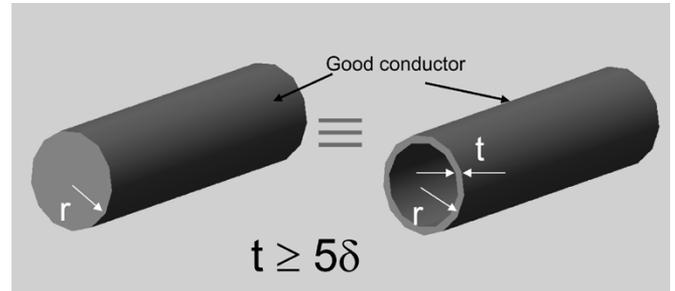


Fig. 1. Solid conductor (left) and electrically equivalent hollow conductor (right) in the high frequency regime.

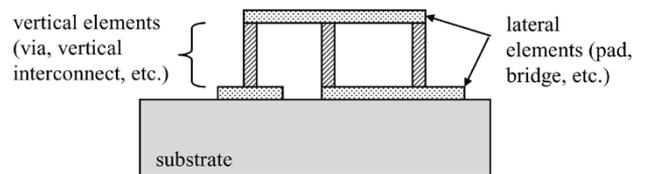


Fig. 2. Two conductor elements in RF components: vertical elements (via or vertical interconnect) and lateral elements (lateral pad on the substrate or lateral bridge).

is large in thickness compared with the skin depth at the operating frequencies of interest, no degradation of conductivity is expected in polymer-core (or epoxy-core) structures compared with all-metal structures. Due to ease of fabrication, such conductors are potentially of interest for many RF microelectromechanical systems (MEMS) applications, such as inductors, transformers, fixed and variable capacitors, switches, and antennas.

Typical RF MEMS components consist of two basic elements as shown in Fig. 2: a vertical element such as a via, a vertical interconnect, or a wall; and a lateral element such as a lateral pad or electrode on the substrate, or a laterally extended bridge. In many cases, conventional vertical and lateral elements have been implemented using via mold formation and subsequent metal electrodeposition through the mold [1], [2], such that a solid metal structure is formed. Often this approach possesses fabrication challenges such as difficulty in formation of the tall and high-aspect-ratio via molds, and difficulty in subsequent plating through the narrow and deep molds leading to seams or voids, and finally lengthy process time which increases with the via height.

Alternatively, the conductor elements can be implemented using a polymer back-bone structure patterned in desired shapes followed by subsequent metal overcoat. This approach takes advantage of advanced MEMS polymer processes for relatively easy fabrication of complicated three-dimensional (3-D) structures, while maintaining good electrical RF conductor performance by ensuring the metal overcoat is several skin depths in

Manuscript received July 19, 2004; revised February 11, 2005. Subject Editor K. Najafi.

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: yky7434@ece.gatech.edu).

Digital Object Identifier 10.1109/JMEMS.2005.851804

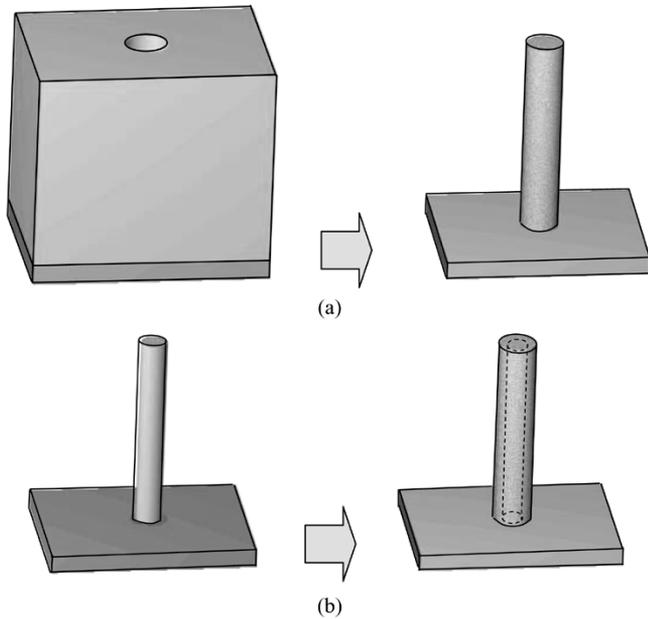


Fig. 3. Two approaches for vertical interconnects. (a) Solid conductor. (b) Polymer-core conductor.

thickness [3]. SU-8 (Microchem, Inc.), a negative-tone photodefinable epoxy, is considered as a good candidate for a back-bone polymer material since it allows thick and high-aspect-ratio 3-D structures to be fabricated relatively easily [4], [5] and complex 3-D structures fabricated using SU-8 have been reported by many researchers [6]–[11].

This paper consists of three sections. In the first section, fabrication processes for high-aspect-ratio vertical RF conductors using SU-8 column patterning and subsequent electrodeposition over the column are introduced. Second, a fabrication process for lateral SU-8 bridge formation using double-exposure-single-development is introduced and the bridge thickness is characterized as a function of the UV dose and the post exposure bake time. Third, with combination of the vertical and lateral epoxy back-bone patterning and a subsequent single electrodeposition step, a 3-D, high-aspect-ratio, high Q-factor, solenoid-type RF inductor is fabricated and tested to demonstrate the process feasibility for RF applications.

II. POLYMER-CORE APPROACHES FOR VERTICAL RF CONDUCTORS

In this section, fabrication processes for high-aspect-ratio RF conductors are detailed using SU-8 column patterning and subsequent electrodeposition over the column. The concept of the polymer-core conductor (or in this case epoxy-core conductor) combining epoxy back-bone patterning with subsequent metallization provides a methodology for obtaining complex 3-D shapes of various RF components with relative ease by taking advantage of advanced 3-D epoxy fabrication technologies. The developed polymer-core conductor technique can be applied to fabricate RF passive components such as inductors, capacitors, and millimeter wave radiating components.

Two fabrication approaches for a high-aspect-ratio vertical interconnect are shown in Fig. 3. One approach is to make a

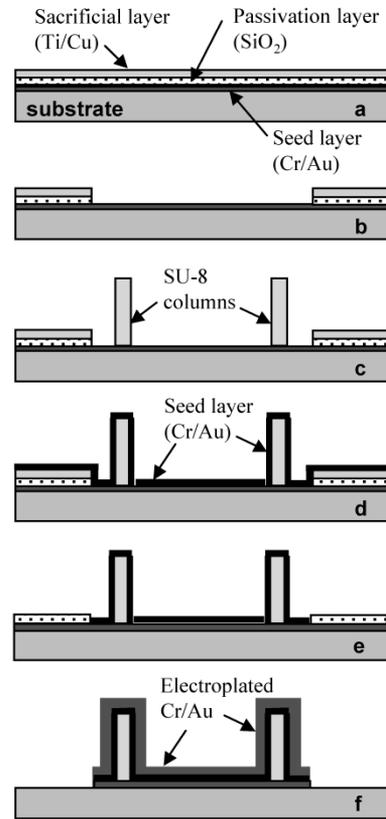


Fig. 4. Fabrication process using a prepatterned seed layer scheme for column metallization.

concave via mold and fill it solidly with plated metal, which will be called a *solid conductor* process in Fig. 3(a). The other is to make a high-aspect-ratio polymer column and cover it with plated metal, which will be called a *polymer-core conductor* process in Fig. 3(b).

A fabrication process for vertical polymer-core RF conductors is detailed in Fig. 4. It utilizes a prepatterned seed layer scheme. First, the following three layers (each with a different ultimate function as will be seen below) are deposited in sequence: a seed layer (Cr/Au; 20 nm/150 nm), a passivation layer (SiO₂; 1 μm or thin SU-8; 2 μm), and a sacrificial layer (Ti/Cu; 20 nm/1 μm) (a). Patterning for the bottom conductors is performed using copper and titanium etching followed by oxide or SU-8 etching (b). A tall SU-8 column is patterned (c), and another seed layer (Cr/Au, 20 nm/150 nm) is conformally deposited using a dc sputterer (d). The sacrificial copper layer is etched using cupric sulfate saturated ammonium hydroxide solution. In this step, Cr/Au on top of copper is also lifted off. Titanium is etched using diluted hydrofluoric acid (HF) etchant (e). Copper and gold are plated up to thicknesses of 15 and 1 μm, respectively, over the columns and the bottom electrode area simultaneously. The top gold is used for a protection layer during subsequent seed layer etching and as an anti-erosion final layer for the RF components. The remaining passivation layer and the seed layer are removed to complete the process (f).

Fig. 5 shows a pair of epoxy core conductors simultaneously fabricated with a bottom conductor using a prepatterned seed

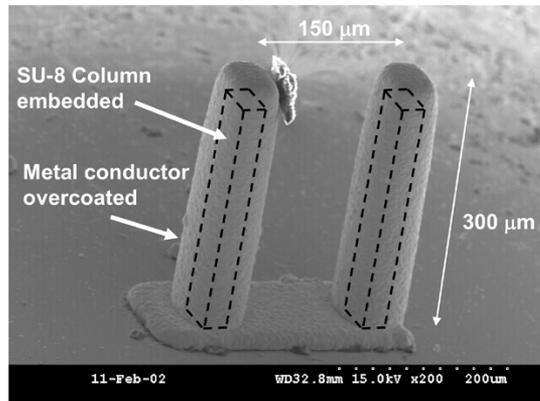


Fig. 5. Epoxy-Core conductor fabricated using a prepatterned seed layer scheme for column metallization.

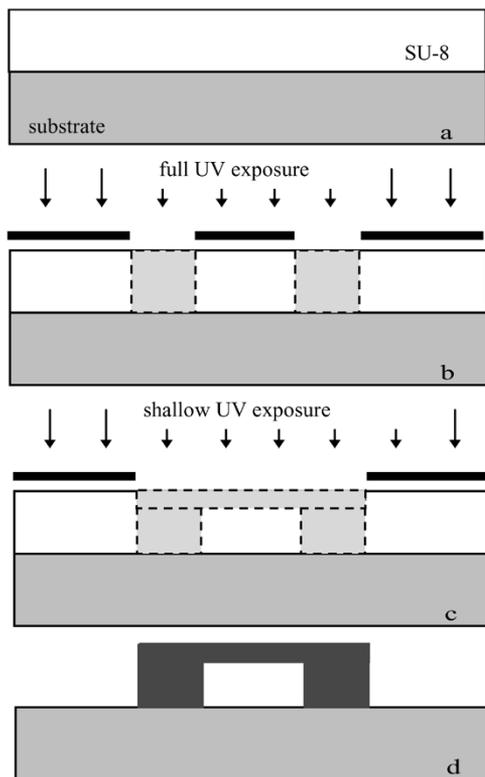


Fig. 6. Fabrication process for a bridge or a channel structure using a double-exposure-single-development technique.

layer scheme. Since the vertical conductors and the horizontal conductor are monolithically fabricated by a single electroplating step, they do not have an intermediate layer between each part, resulting in potentially improved mechanical and electrical properties compared with a conventional fabrication scheme, which uses two separate seed layer and electroplating steps [1]. In addition, closely placed vertical conductors (pitch between columns: $150\ \mu\text{m}$, column height: $300\ \mu\text{m}$) are successfully fabricated using this process.

A comparison of the vertical solid conductor process and the vertical polymer-core conductor process is summarized in

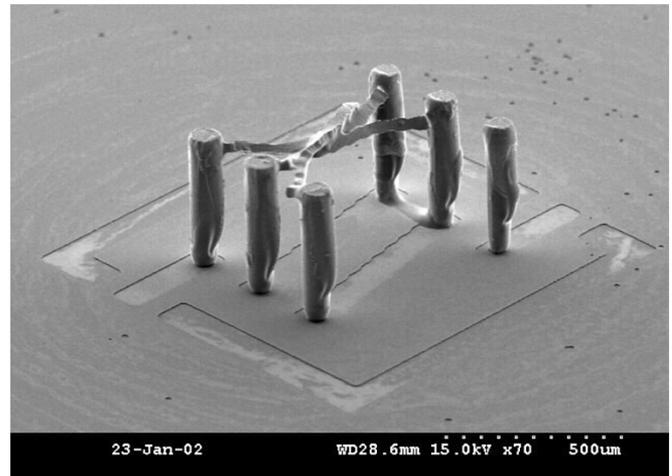


Fig. 7. Distorted bridges during the development due to poorly polymerized top portion of SU-8 in the case of using a hotplate for the second postexposure bake.

TABLE I
PROCESS COMPARISON OF VERTICAL SOLID CONDUCTOR PROCESS AND
POLYMER-CORE CONDUCTOR PROCESS USING UV LITHOGRAPHY
AND PLATING

	Solid conductor process	Polymer-core conductor process
Conductor type	Solid	Hollow
Polymer structure	Via mold	Column
High-aspect-ratio patterning material	SU-8(moderate-difficult), Other photoresists	SU-8(moderate)
Reasonably achievable aspect ratio	~5	~10
Metallization	Via filling plating (difficult) -stirring -vacuuming -additives	Column coating plating (easy) -mild stirring
Plating time	Long~ medium	Short
Mold removal	Solvent or dry ashing	Not required
Photolithography	Via mold patterning	Column patterning and Selective metallization (proximity UV lithography, pre-patterning, or electroless plating)
Preferred applications	Conductors for Power MEMS applications	RF MEMS; 3-D inductors, capacitors, transformer, vertical coaxial interconnect, millimeter wave antennas

Table I. In addition to the selective metallization for the epoxy-core conductors discussed here, it is also possible to consider direct metallization of the epoxy column using electroless plating with use of a conductive epoxy as a back-bone or a surface modification of conventional SU-8 epoxy [12]. This could result in fabrication simplification, but it was not extensively researched here.

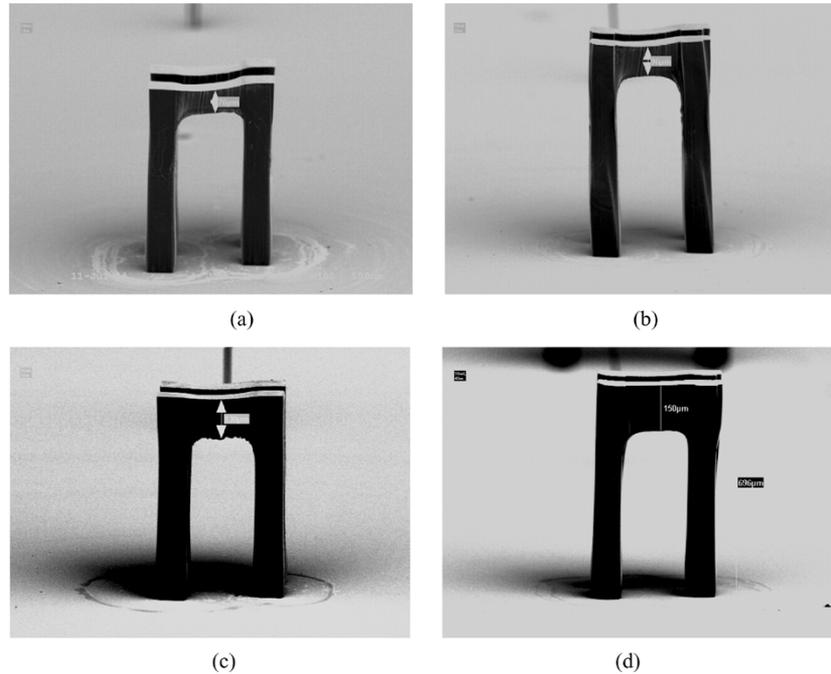


Fig. 8. Fabricated lateral SU-8 bridge structures with optical dose of 50 mJ/cm^2 and the various oven baking time of (a) 10, (b) 20, (c) 30, and (d) 40 min; the resultant bridge thickness is (a) 76, (b) 96, (c) 130, and (d) $150 \mu\text{m}$.

III. DOUBLE-EXPOSURE-SINGLE-DEVELOPMENT FOR LATERAL BRIDGE

Feely *et al.* at Rohm and Haas showed a 3-D-thick photoresist process using their dual-tone photoresist [13], [14], where they demonstrated that dual-tone resist chemistry combined with optical dose-controlled UV exposure could generate various patterns such as steps or overhangs. Multistep or continuous structures can be achieved by single exposure and single development with a grey-tone mask [15]; however, often the required high resolution mask is more expensive than its conventional counterparts. Alternatively, multiexposure processes with separate mask sets and controlled exposure time have been utilized for various applications, including RF inductors [16] and inkjet nozzles [17] both using a positive-tone photoresist and microchannels using SU-8 [11].

In this section, a double-exposure-single-development process used for high-aspect-ratio bridge fabrication is discussed. While the SU-8 multiexposure-single-develop technique described in [11] utilized antireflection coatings in order to control the thickness of the upper portion of the device, the technique described here relies on the control of the optical dose and the baking steps (baking method and baking duration) after the second exposure to achieve the final structure.

A. Fabrication

A fabrication process for a bridge or a channel structure using a double-exposure-single-development technique with SU-8 is detailed in Fig. 6. SU-8 (2025) with a thickness of $700 \mu\text{m}$ is coated on a substrate. The thickness is controlled by weighing the proper amount of SU-8 on a substrate and placing it on a hot plate. The reduced viscosity of SU-8 at high temperature makes the SU-8 uniformly spread over the substrate on the

well-leveled hot plate, resulting in self-planarization. The thick epoxy is then soft-baked for 22 h on the hot plate at 95°C (a). Full UV optical dose (I-line UV source; 365 nm , 3000 mJ/cm^2) is applied through a mask to create a latent image of the column or the channel wall (b). A postexposure bake is performed on the hot plate for 1 h at 95°C . Before it is developed, a shallow optical dose is applied to form the latent image of the top bridge or the channel cover layer (I-line UV source; 365 nm , $50\text{--}150 \text{ mJ/cm}^2$) (c). In order to efficiently crosslink the upper portion of the SU-8, the postexposure bake is performed in an oven ($10\text{--}40 \text{ min}$, 95°C) instead of on a hotplate. The structure is developed in SU-8 developer, propylene glycol monomethyl ether acetate (PGMEA), for 2 h to complete the process (d).

B. Characterization and Discussion

In the case of using a hotplate for the second postbake instead of an oven, the heat energy required for SU-8 polymerization is not effectively transferred from the substrate bottom to the top portion through the thick polymer layer. Polymerization of the top portion either does not occur, or results in very weak and loose bridge structures. After development, the bridges swing between posts and adhere to a neighboring bridge when drying the sample as shown in Fig. 7.

In the case of using an oven for the second postbake, the thickness of the bridge is controlled by the optical dose and the postexposure bake time. In order to characterize this double-exposure-single-development scheme, a set of bridge structures with a height of $700 \mu\text{m}$ are fabricated using SU-8 (2025) with various optical doses (50 mJ/cm^2 , 100 mJ/cm^2 , and 150 mJ/cm^2), and various bake times (10, 20, 30, and 40 min) in the oven at 95°C . After develop, rinse, and dry, the bridge thickness of the samples has been measured. Fig. 8 shows fabricated lateral bridge structures with an optical dose of 50 mJ/cm^2 and an

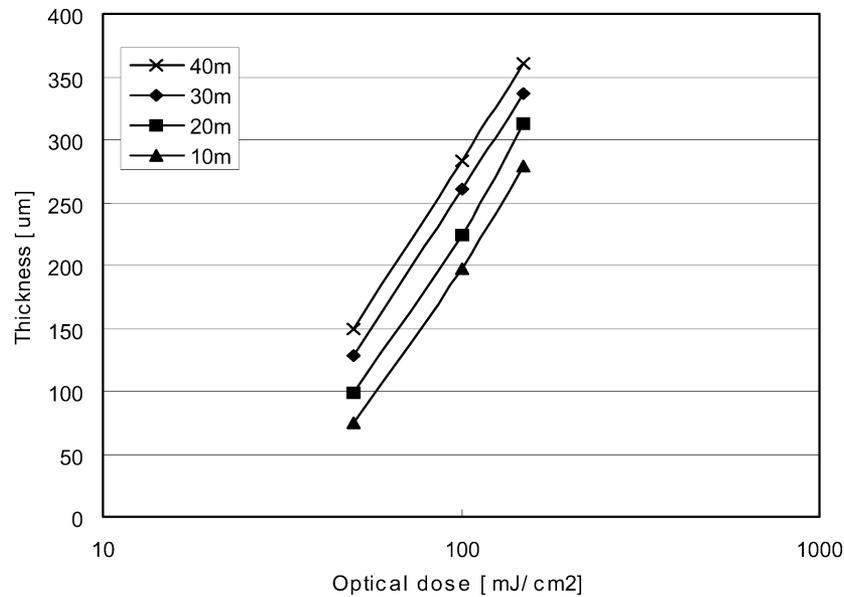
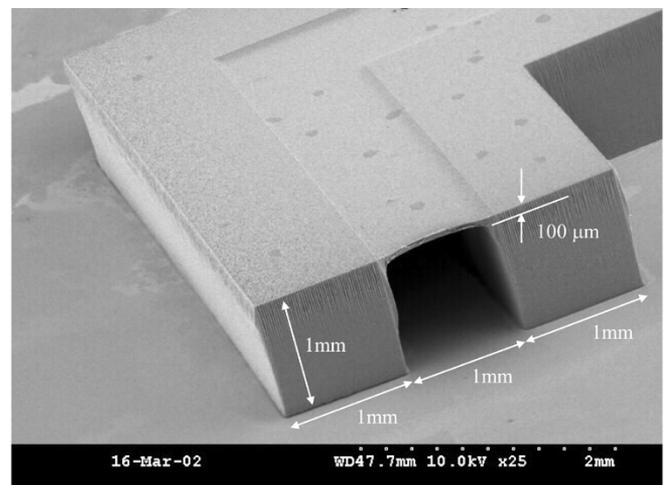


Fig. 9. Bridge thickness as a function of exposure dose (50, 100, and 150 mJ/cm^2) parameterized by postexposure bake time (10, 20, 30, and 40 min). A linear dependence of thickness on bake time, and a logarithmic dependence of thickness on exposure dose are observed.

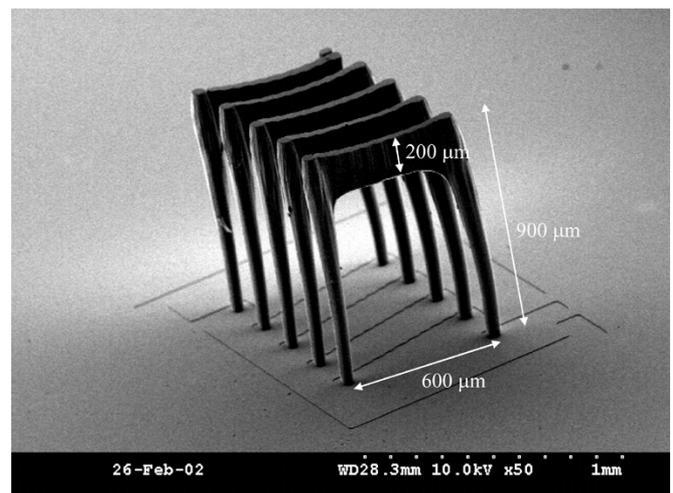
oven bake time of (a) 10, (b) 20, (c) 30, and (d) 40 min, resulting in a bridge thickness of (a) 76, (b) 96, (c) 130, and (d) 150 μm , respectively. Fig. 9 shows the resultant average bridge thickness as a function of the optical dose and the postexposure bake time. At least three different samples with the same fabrication condition are fabricated and the thickness is measured and averaged for each data collection. The mean values are within $\pm 2 \mu\text{m}$ for 50 mJ/cm^2 samples and $\pm 5 \mu\text{m}$ for 100 mJ/cm^2 and 150 mJ/cm^2 samples. The bridge thickness shows a linear dependency on the bake time between 10 and 40 min for all three optical doses, while the thickness shows a logarithmic relationship with the optical dose, as expected. To obtain a specific bridge thickness, multiple parameter sets of the optical dose and the postexposure bake time can be chosen in the graph. For example, a bridge thickness of 280 μm can be obtained with an optical dose of 150 mJ/cm^2 and a baking time of 10 min, with an optical dose of 100 mJ/cm^2 and a baking time of 40 min, or with other combinations of the dose and the bake time. No structural differences between two bridge structures obtained from two different fabrication conditions have been observed; quantitative chemical and mechanical properties of the bridge structure fabricated using different condition have not been characterized here. Note that the UV source used for this experiment is I-line (wavelength 365 nm); differing wavelength of UV sources yield different bridge formation results.

As examples of structures that can be produced from a well-characterized process, Fig. 10(a) and (b) show a microfluidic channel and a bridge structure with the top portion thickness controlled based on the previous data. The channel has a width of 1 mm, a height of 1 mm, and a cap thickness of 100 μm while the bridge has a lateral length of 600 μm , a height of 900 μm , and a bridge thickness of 200 μm . Also, various SU-8 structures for RF applications using this approach are shown in Fig. 11: a solenoid-type inductor, a transformer, a spiral-type inductor, and vertical coaxial interconnect.

The polymer-core approach has been applied for wafer level interconnect by Joung [18], where the reliability test has been



(a)



(b)

Fig. 10. Successfully fabricated structures. (a) Microfluidic channel. (b) Bridges connecting two columns.

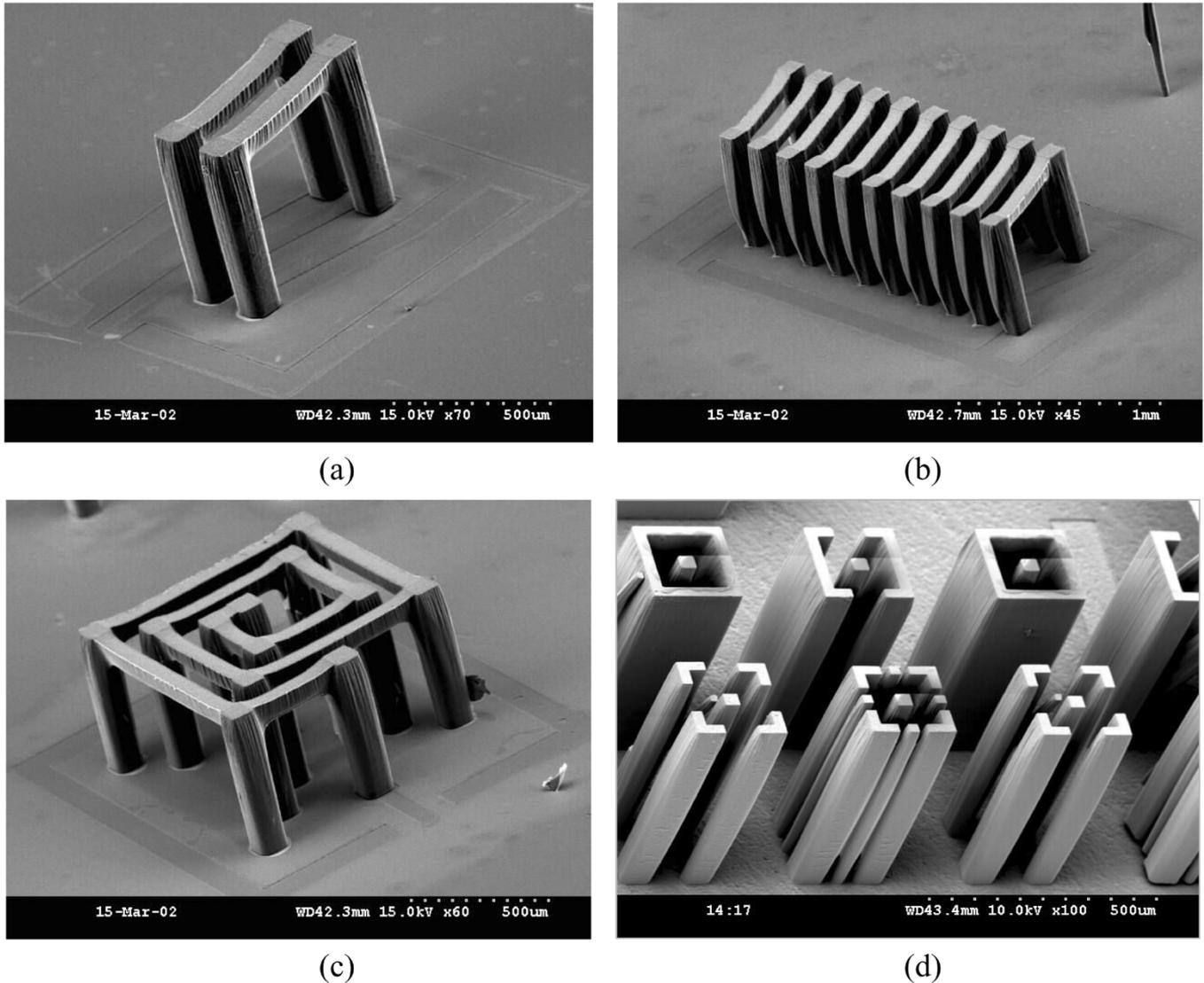


Fig. 11. SU-8 backbone structures for RF applications. (a) Solenoid-type inductor. (b) Transformer. (c) Spiral-type inductor. (d) Vertical coaxial interconnect.

performed between 40 °C and 147 °C. No failure during 5000 cycles with a period of 5 min has been reported. The conventional plastic chip packaging has its thickness of 3–4 mm, allowing tall structures with a height of up to 1 mm to be accommodated, while the flip chip technique requires a gap of 100 to 300 μm between chip and the substrate and highly extruding structure may not be placed.

IV. HIGH-ASPECT-RATIO INDUCTOR USING EPOXY-CORE CONDUCTOR

Integrated 3-D solenoid-type RF inductors with high Q-factor fabricated using MEMS technology have been pursued for several years [1], [19]–[22]. Recently, these devices have been integrated with CMOS circuits to form functional RF amplifiers [20]. These devices are typically fabricated by plating through photoresist molds. However, the ratio of coil height to turn-to-turn pitch in many of these devices is relatively low due to difficulties in forming and filling extremely small, high-aspect-ratio via holes. The low profile coil suffers from magnetic flux

leakage between relatively wide conductor line spaces, resulting in a reduction of the Q-factor. Increased core height, leading to a geometry closer to an ideal solenoid, should yield more ideal performance. In addition, the conventional integrated solenoid inductors consisted of at least three discrete layer processes: lower electrode, via, and upper electrode. This separate layer construction not only leads to an increased number of electrodeposition steps, but also has the potential for increased via resistance and/or mechanical weakness at each interface.

In this section, a high-aspect-ratio solenoid inductor is fabricated and tested to demonstrate the feasibility and the usefulness of the epoxy-core conductor technique for RF applications. The high-aspect-ratio (up to 10:1) columns and laterally extended bridge on top of the columns with a double-exposure-single-development technique are formed to provide a solenoid back-bone structure out of SU-8 epoxy. They are then selectively covered in a single electrodeposition step to provide the electrical path. With this geometry, a large inductance in the same number of turns is obtained, and the device is geometrically closer to an ideal solenoid inductor.

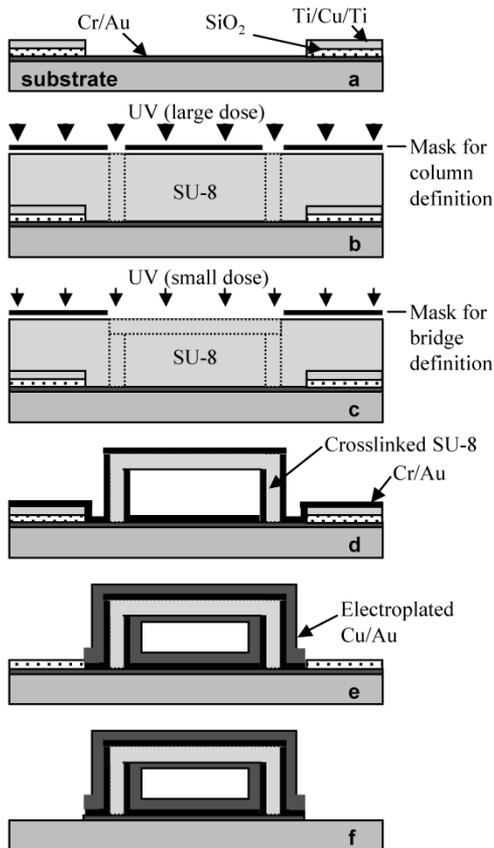
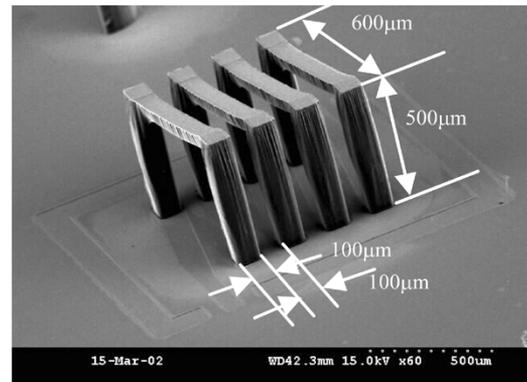


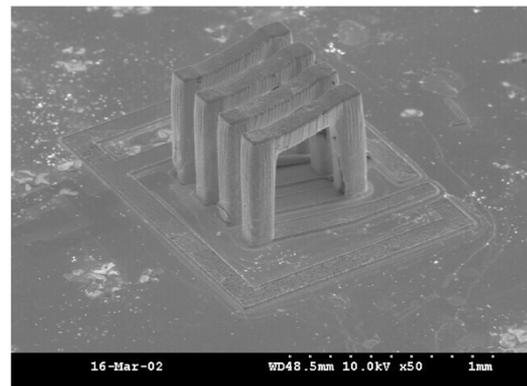
Fig. 12. Fabrication process of high-aspect-ratio inductor using epoxy-core conductor.

A. Fabrication

The fabrication process adopts a prepatterned seed layer scheme introduced in Section II for the selective SU-8 metallization and the details are depicted in Fig. 12. In order to selectively coat metal only on the SU-8 column, bridge, and bottom electrode definition area, three foundation layers are deposited on a glass substrate: a chromium/gold (Cr/Au, 20 nm/100 nm thick) electrical seed layer for electroplating; a silicon dioxide (SiO_2 , 1000 nm thick) passivation layer; and titanium/copper/titanium (Ti/Cu/Ti, 30 nm/1000 nm/30 nm) as a sacrificial layer for selective seed layer definition. The Ti/Cu/Ti and silicon dioxide layers are patterned for bottom electrode definition using photolithography and subsequent chemical etching (a). A single SU-8 layer is coated and soft baked, where the thickness of the SU-8 layer becomes height of the inductor. A large optical dose is applied through the column mask and postexposure baked at 95 °C on a hot plate (b). Prior to development, a small optical dose is applied through the lateral bridge mask, and the structure is postexposure baked at 95 °C in an oven. After these two-step exposures and bakes, the SU-8 has the desired bridge portion cross-linked at the top of the cross-linked columns (c). Developing the SU-8 leaves the column and bridge. After curing the released structure in a 100 °C oven for 3 h for removal of residual solvent in SU-8, Cr/Au (20 nm/150 nm) layers are coated using DC sputtering as the seed layer for subsequent electroplating (d). Removal of the previously deposited Cu/Ti layers leaves the Cr/Au



(a)



(b)

Fig. 13. Fabricated structure. (a) Fabricated SU-8 core structures prior to metal deposition. (b) After metal coating to form solenoid inductors. Note that the height of the inductors is approximately 500 μm .

TABLE II
SUMMARY OF REPORTED SOLENOID TYPE INDUCTORS

Reference	Inductance [nH]	Peak-Q	Peak-Q Frequency [GHz]	Year
Young [21]	4.8	30	1	1997
Kim [1]	1.7	56	7	1998
Yoon [19]	2.7	17	2.4	1999
Yoon [20]	2.6	21	4.5	2001
Joung [22]	3.45	71	2.0	2002
This Work	1.17	84	2.6	

seed layers only on the surface of the SU-8 structure and the bottom electrode area predefined in step (a). Cu/Au layers are then electroplated in sequence over the column and the bridge as well as on the bottom electrode area simultaneously to a thickness of 10–15 microns (e). Note that the skin depth of copper at 1 GHz is approximately 2 μm ; a 10 μm thickness of plated copper is 5 skin depths. Removal of the passivation SiO_2 and initial Cr/Au layer in sequence isolates the structure to complete the process (f).

B. Experiment and Results

Test inductor structures are fabricated on a glass substrate. A fabricated SU-8 core structure prior to metal deposition and after metal coating to form solenoid inductors is shown in Fig. 13(a) and (b), respectively. The height of the inductor is approximately 500 μm and copper and gold are electrodeposited in sequence to thicknesses of 14 and 1 μm , respectively,

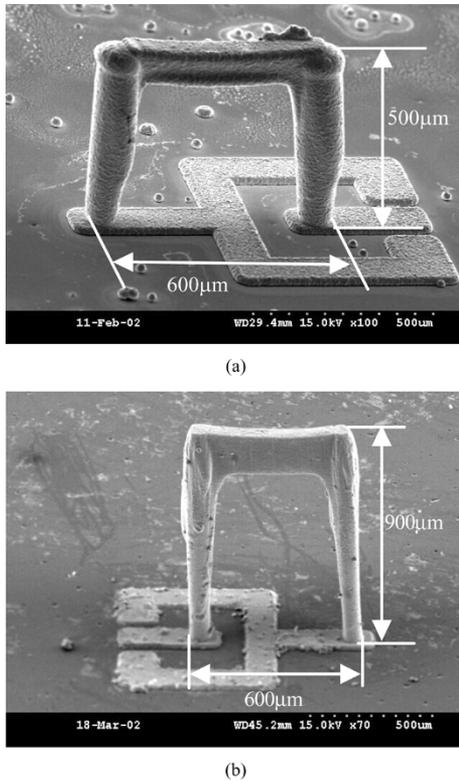


Fig. 14. Single-turn inductors. (a) 500 μm device. (b) 900 μm device.

in order to form electrical inductor path. Random metal bump growth through pin holes of the PECVD deposited oxide layer has been observed on the substrate during the electroplating. These undesired metal bumps can cause some structures to be shorted. The metal bumps have been removed through an extended substrate etch in dilute HF, resulting in the rough substrate surface in Fig. 13(b).

Two single-turn inductors, one 500- μm tall with a 600- μm core width, and the other 900- μm tall with a 600- μm core width, are shown in Fig. 14. S-parameter measurement is carried out in the frequency range of 100 MHz to 10 GHz using an HP8510C vector network analyzer with standard air coplanar G-S-G probe tips (150 μm pitch) from Cascade Microtech after a standard Short-Open-Load-Thru (SOLT) calibration. Inductance and Q-factor are extracted from the measured S-parameters. The obtained inductance and Q-factor as a function of frequency is shown in Fig. 15. The 900 μm device shows an inductance and a maximum Q-factor of 1.17 nH and 84 (at 2.6 GHz), respectively, while the 500- μm device shows an inductance and a maximum Q-factor of 0.77 nH and 85 (at 2.5 GHz), respectively. Inductance and Q-factor of the 900- μm device have been compared with those of solenoid-type inductors reported by other researchers in Table II. The relatively large Q-factors indicate that the RF performance of these devices is not degraded by conductors with epoxy-cores as compared with solid-cores.

V. CONCLUSION

A polymer-core conductor technology for RF application is introduced and implemented using SU-8 back-bone structure fabrication and subsequent selective metallization. The technology takes advantage of advanced micromachining polymer

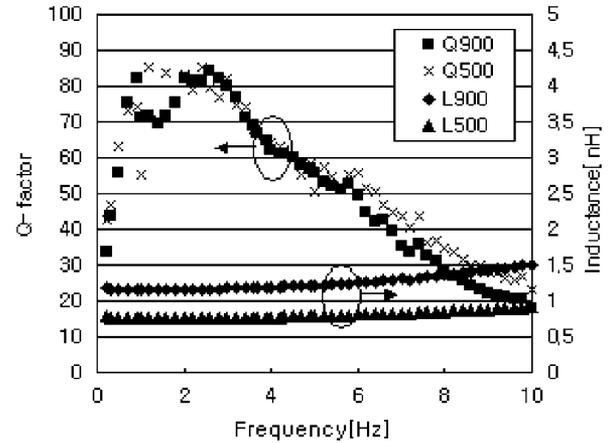


Fig. 15. Inductance and Q-factor for two single turn inductors.

process to build complex 3-D structures and overcoat them with metal for electrical component functionality to the thickness of several skin depths in the operating frequency of interest to maintain their electrical performance. This approach is quite appropriate for RF component applications with its process simplicity and potential for applications requiring complex 3-D structures. As an example, epoxy-core vertical interconnect formation and its selective metallization processes are demonstrated. The laterally extended polymer bridge fabrication using double-exposure-single-development is detailed and characterized with optical dose and postexposure bake time. The fabrication advantages of this approach have been utilized to create tall, 3-D solenoid inductors. As predicted by the skin effect phenomenon, high Q-factor is obtained even though the interior core of the devices is nonconducting. This approach may also be of interest for other RF MEMS applications, such as transformers, switches, and antennas.

ACKNOWLEDGMENT

The authors would like to thank Dr. S.-W. Yoon and Prof. J. Laskar of the Georgia Institute of Technology (Georgia Tech), Atlanta, for their assistance with device measurement and Dr. Y.-H. Joung and Dr. F. Cros, also of Georgia Tech, for helpful technical discussion.

REFERENCES

- [1] Y. J. Kim and M. G. Allen, "Surface micromachined solenoid inductors for high frequency applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, pt. C, vol. 21, no. 1, pp. 26–33, Jan. 1998.
- [2] J. Y. Park and M. G. Allen, "High Q spiral-type microinductors on silicon substrates," *IEEE Trans. Magn.*, vol. 135, pp. 3544–3546, 1999.
- [3] Y.-K. Yoon, J.-W. Park, and M. G. Allen, "RF MEMS based on epoxy-core conductors," in *Dig. Solid-State Sensor, Actuator, and Microsystems Workshop 2002*, Hilton Head Island, SC, 2002, pp. 374–375.
- [4] M. Despont, H. Lorenz, N. Fahrni, J. Brugger, P. Renaud, and P. Vettiger, "High-aspect-ratio, ultrathick, negative-tone near-UV photoresist for MEMS applications," *Proc. IEEE Microelectromech. Syst.*, pp. 518–522, 1997.
- [5] H. Lorenz, M. Despont, N. Fahrni, J. Brugger, P. Vettiger, and P. Renaud, "High-aspect-ratio, ultrathick, negative-tone near-UV photoresist and its applications for MEMS," *Sens. Actuators*, vol. A 64, pp. 33–39, 1998.
- [6] Y.-K. Yoon, J.-H. Park, F. Cros, and M. G. Allen, "Integrated vertical screen microfilter system using inclined SU-8 structures," in *Proc. IEEE Microelectromech. Syst. (MEMS)*, Kyoto, Japan, 2003, pp. 227–230.

- [7] H. Sato, T. Kakinuma, J. S. Go, and S. Shoji, "A novel fabrication of in-channel 3-D micromesh structure using maskless multi-angle exposure and its microfilter application," in *Proc. IEEE Microelectromech. Syst. (MEMS)*, Kyoto, Japan, 2003, pp. 223–226.
- [8] M. Han, W. Lee, S. K. Lee, and S. S. Lee, "Fabrication of 3D microstructures with inclined/rotated UV lithography," in *Proc. IEEE Microelectromech. Syst. (MEMS)*, 2003, pp. 554–557.
- [9] J.-H. Park, Y.-K. Yoon, M. R. Prausnitz, and M. G. Allen, "High-Aspect-Ratio tapered structure using an integrated lens technique," in *Proc. IEEE Microelectromech. Syst. (MEMS)*, Maastricht, The Netherlands, 2004, pp. 383–386.
- [10] Y. Choi, R. Powers, V. Vernekar, A. B. Frazier, M. LaPlaca, and M. G. Allen, "High aspect ratio SU-8 structures for 3-D culturing of neurons," in *Proc. ASME Int. Mech. Eng. Congress and Exposition*, Nov. 2003.
- [11] F. C. Tseng, Y. J. Chuang, and W. K. Lin, "A novel fabrication method of embedded micro channels employing simple UV dosage control and antireflection coating," in *Proc. IEEE Microelectromech. Syst. (MEMS)*, Las Vegas, NV, 2002, pp. 69–72.
- [12] A. O. Aggarwal, K. Naeli, P. M. Raj, F. Ayazi, S. Bhattacharya, and R. R. Tummala, "MEMS composite structures for tunable capacitors and IC-package nano interconnects," in *Proc. IEEE ECTC*, 2004.
- [13] W. E. Feely, J. C. Imhof, and C. M. Stein, "The role of the latent image in a new dual image, aqueous developable, thermally stable photoresist," *Polym. Eng. Sci.*, vol. 26, pp. 1101–1104, 1986.
- [14] W. E. Feely, "Micro-Structures," in *Tech. Dig. Solid State Sensor and Actuator Workshop*, Hilton Head Island, SC, 1988, pp. 13–15.
- [15] P. Six, "Phase masks and grey-tone masks," in *Semiconductor Fabtech*, 1995.
- [16] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, K. Lee, and C.-K. Kim, "High-Performance electroplated solenoid-type integrated inductor (S^2) for RF applications using simple 3D surface micromachining technology," in *Tech. Dig. IEEE Int. Electron Devices Meeting (IEDM '98)*, 1998, pp. 544–547.
- [17] J.-D. Lee, J.-B. Yoon, J.-K. Kim, H.-J. Chung, C.-S. Lee, H.-D. Lee, H.-J. Lee, C.-K. Kim, and C.-H. Han, "A thermal inkjet printhead with a monolithically fabricated nozzle plate and self-aligned ink feed hole," *IEEE J. Microelectromech. Syst.*, vol. 8, no. 3, pp. 229–236, 1999.
- [18] Y.-H. Joung, "Electroplating bonding technology for chip interconnect, wafer level packaging and interconnect layer structures," Ph.D., Georgia Inst. Technol., Atlanta, 2003.
- [19] J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, "Surface micromachined solenoid on-Si and on-glass inductors for RF applications," *IEEE Electron Dev. Lett.*, vol. 20, pp. 487–489, 1999.
- [20] Y.-K. Yoon, E. Chen, M. G. Allen, and J. Laskar, "Embedded solenoid inductors for RF CMOS power amplifier," in *Dig. 11th Int. Conf. Solid-State Sensors and Actuators, Transducers'01 Eurosensors XV*, vol. 2, 2001, pp. 1114–1117.
- [21] D. J. Young, V. Malba, J.-J. Ou, A. F. Bernhardt, and B. E. Boser, "Monolithic high-performance three-dimensional coil inductors for wireless communication applications," in *IEEE Electron Dev. Meeting Tech. Dig.*, Dec. 1997, pp. 67–70.
- [22] Y.-H. Joung, S. Nuttinck, S.-W. Yoon, M. G. Allen, and J. Laskar, "Integrated inductors in the chip-to-board interconnect layer fabricated using solderless electroplating bonding," in *IEEE Int. Microw. Symp. Dig.*, vol. 3, Jun. 2002, pp. 1409–1412.



Yong-Kyu Yoon (S'03–M'04) received the B.S. and M.S. degrees in electrical engineering in 1992 and 1994, respectively, from Seoul National University, Korea. He received the M.S.E.E. degree from the New Jersey Institute of Technology, Newark, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, in 1999 and 2004, respectively.

He is currently a Postdoctoral Fellow at the Microelectronics Research Center, Georgia Tech. He is engaged in the research of developing RF passive components and millimeter-wave antennas using 3-D MEMS technology, ferroelectric material study and its RF applications, and microfluidic system development for the lab-on-a-chip bio/chemical applications.



Jin-Woo Park received the B.S. degree in electrical engineering from Sung Kyun Kwan University, Seoul, Korea, in 1996, and the M.S. and Ph.D. degrees in electrical and computer engineering in 2000 and 2004, respectively, from the Georgia Institute of Technology (Georgia Tech), Atlanta.

He is currently working as a Postdoctoral Fellow at Georgia Tech. His research interests include design, fabrication, and characterization of micromachined magnetic components for power applications, and inductive heating of micromachined structures for transdermal drug delivery application.



Mark G. Allen (M'89–SM'04) received the B.A. degree in chemistry, the B.S.E. degree in chemical engineering, and the B.S.E. degree in electrical engineering from the University of Pennsylvania, Philadelphia, in 1984, and the S.M. and Ph.D. degrees in microelectronic materials from the Massachusetts Institute of Technology (MIT), Cambridge, in 1986 and 1989, respectively.

His research at MIT focused on micromachining techniques to create structures for the *in situ* measurement of mechanical properties and adhesion of thin films for use in microelectronic processing. He was also engaged in microactuators, microactuators, and in feedback-stabilized micromachined mirrors for laser applications. He joined the faculty of the Georgia Institute of Technology, Atlanta, after a Postdoctoral appointment at MIT. His current research interests are in the field of micromachining and in microsensor and microactuator fabrication that is compatible with the IC fabrication. Other interests are in micromachined pressure sensors and in acceleration sensors, micromotors, in integrated flow valves, in piezoelectric materials combined with semiconductor circuits and optical materials, in multichip packaging for integrated circuits and microstructures, in integration of organic piezoelectric materials with semiconductor circuits for sensing and actuation, and in materials and mechanical property issues in micromachining.