MICROMACHINED CAPACITORS BASED ON AUTOMATED MULTILAYER ELECTROPLATING

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ABSTRACT

A new type of capacitor, based on a high-aspect-ratio 3-dimensional micromachining process, is presented. Submicron layers of alternating metals are deposited by an automated robotic electroplating system. Selective etching of one of the two metals leaves a highly laminated structure with large surface area. To demonstrate the increased surface area, this structure is used as one electrode of a capacitor. A dielectric layer is added by atomic layer deposition (ALD) of alumina. A liquid electrolyte is added and vacuum-infiltrated to form the second electrode. 1.5 nF/mm^2 capacitance density is produced with a 10-layer structure.

INTRODUCTION

Power management passives continue to present an ever-growing challenge for electronics systems. A majority of modern components, from inertial sensors to pull-up resistors, have well-known, continually materializing paths to wafer- and package-level integration. However, capacitors, inductors, and transformers remain relatively unaccommodated, typically still being manufactured with bulk techniques such as wire winding or film stacking and rolling. [1] [2] Small-value components, such as those found in analog and radio-frequency circuitry, can in cases be built economically by normal IC fabrication flows. However, capacitors and magnetics of more substantial size, such as those used in power management, require more potent fabrication options.

Multilayer electrodeposition combined with sacrificial etching has been used to build magnetic cores with micron-scale laminations [3]. This approach, and the structures it yields, with their extremely high surface area, have potential for application to a number of important device types beyond magnetics. This paper details the augmentation of this automated multilayer approach through custom equipment [4], shown in Figure 2, and its extension to produce high-density filter capacitors.

The resulting capacitor fabrication flow is compatible with IC backend processing, using only batch-oriented microfabrication processes, including just one vacuum processing step, and operating within a thermal budget of 250 C. Further, it maintains ideal volume utilization over a wide device design space, spanning without penalty tradeoffs between capacitance density, operating voltage, and series parasitics.

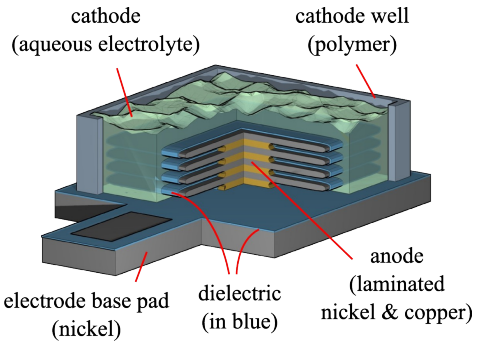

Figure 1: Device schematic

ELECTROPLATED MULTILAYERS

The basic process flow for achieving high surface area with sequential electroplating and sacrificial etching is shown in Figure 3. The first step is the formation of the plating mold, generally through thick-resist photolithography. Next, an arbitrary number of layers are electrodeposited, alternating between the two metals, termed sacrificial and structural metals. The thickness of each layer is set by the plating current and time. Finally, the mold is removed and the multilayer structure is placed in an etchant that will remove the sacrificial metal but not the structural metal. In this

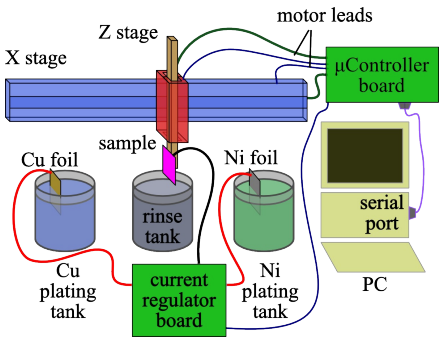

Figure 2: Robotic multilayer electroplating system

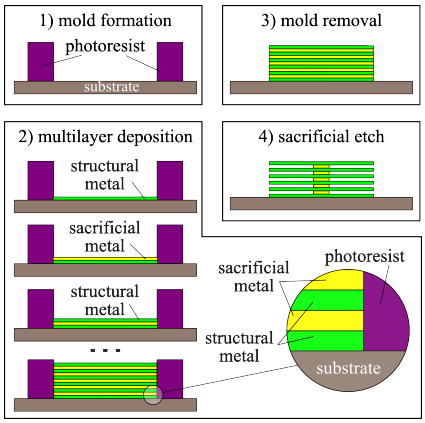

Figure 3: Generic process for laminated structures with multilayer deposition and sacrificial etch

step, the sacrificial layers are partially removed, but some amount of sacrificial material is allowed to remain, providing both mechanical support and electrical continuity between the structural layers. This leaves the structure shown in step 4 of Figure 3. The voids created by removal of the sacrificial material constitute horizontally oriented trenches in the sidewalls of the structure. It is these trenches that contribute the bulk of the structure's surface area.

The key requirements for this process are 1) two metals that readily electrodeposit onto each other and 2) an etchant that is selective to the sacrificial metal. These are not trivial challenges to solve, but once achieved, they allow an extremely wide range of structures to be built. Most importantly, they allow the creation of extremely high aspect ratios. Whereas the vertical dimension of the horizontal trenches can easily be submicron, the horizontal extent of the trenches is limited only by patterned area. Traditionally emphasized capabilities of the mold's photolithography process, such as maximum aspect ratio or sidewall angle, have very little bearing on the gains produced by this process. Figure 4 shows a structure consisting of 110 layers, each with a thickness of 600 nm and a gap of 600 nm between layers.

This process, with its high surface area yield, is of clear relevance in capacitor fabrication, but it can also deliver impact to any class of devices in which surface area is highly valued. These might include sensors, batteries, heat exchangers, and chemical reactors. As well, this process, with its conservative footprint, promises compatibility with a number of other techniques. As applied to capacitors, this process is fully compatible with both materials-based approaches, such as those based on high-*k* dielectrics, and multi-layering

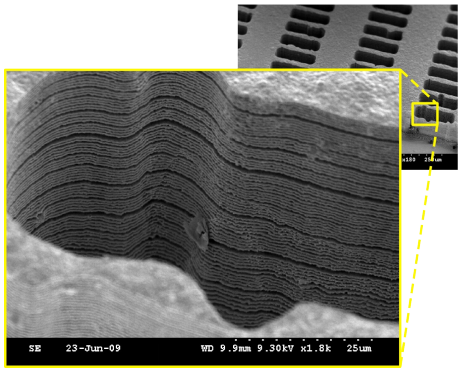

Figure 4: SEM images of anode structure having 110 600 nm thick layers, produced by automated multilayer deposition

approaches, such as those based on sequential metal-insulator deposition.

CAPACITOR FABRICATION

Figure 5 shows the fabrication process used to build the capacitors, consisting of four major steps.

The first step is to deposit the base pad for the first electrode. Approximately 5 µm of nickel is deposited through a 6 µm photoresist (NR9-8000, Futurrex) mold. This pad supports the subsequent multilayer structure, and also provides a terminal for device characterization.

The second step is the formation of the high-surface-area anode structure. This is accomplished by automated multilayer deposition followed by sacrificial etching. Nickel is the structural metal, and copper is the sacrificial metal, and both are plated from sulfate baths. A 120 µm photoresist layer (Futurrex NR2-20000) is used as the electrodeposition mold. For the characterized 10-layer devices, both structural and sacrificial layers were 4 µm thick. A solution of ammonium hydroxide (NH_4OH) saturated with copper sulfate (Cu_2SO_4) is used to selectively remove copper. Figure 6 details one of the completed 10-layer anodes.

Atomic layer deposition (ALD) is used to add the

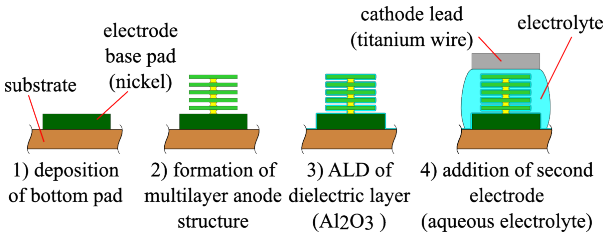

Figure 5: Capacitor fabrication flow

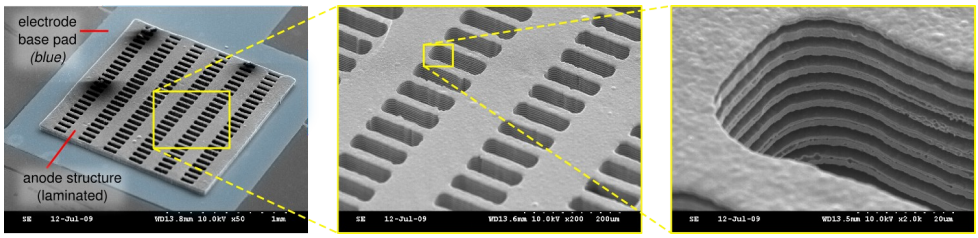

Figure 6: Anode (first electrode) structures

dielectric layer. ALD was selected primarily for its ability to deposit uniformly onto high aspect ratio topologies. Additionally, ALD gives precise control over deposit thickness, and access to a large set of materials. A 100 nm-thick aluminum oxide (Al_2O_3) layer, deposited by 600 cycles of alternating trimethylaluminum ($Al_2(CH_3)_6$) and water precursors at 250 C, encapsulates the anode and forms the capacitor's dielectric.

The Al_2O_3 layer showed excellent durability, except along the outer faces of the laminations. This was most likely due to the sharp edges present along those faces. As a remedy, a 250 nm parylene coating is performed immediately after the ALD step. Parylene's excellent sealing properties were sufficient to mask the breaches in the Al_2O_3 layer, giving functional capacitors.

An aqueous solution of nickel sulfate, boric acid, and saccharin is used for the second electrode. Vacuum is applied to extract air from the horizontal trenches, inducing the liquid to fully infiltrate. A polymer well is added just before the liquid, both to facilitate processing, and to retain maximal infiltration after the vacuum is removed. Figure 7 shows a completed die, containing several devices.

CAPACITOR DESIGN

The surface area amplification achieved by the anode structures is largely vertical in nature, and thus gives performance that is almost entirely independent of lateral geometry. However, it was necessary to design a structure that would address the fragility of the thin anode layers after their release. Substantial deformation is liable to induce fracture in the surrounding dielectric, directly causing device failure.

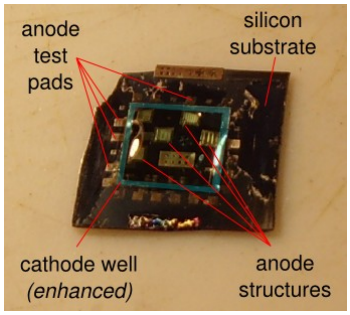

Figure 7: Photograph of completed capacitors

The chosen solution was to implement the capacitors as arrays of air bridges, or fully-released strips of material with mechanical support at both ends. The width of the air bridges was set to 15 µm, and their length was varied between 130 µm and 590 µm. The support regions were 100 µm wide. The air bridge arrays were approximately 1.5 mm x 1.5 mm overall. The minimum bridge width of 15 µm was due to the 1:7 aspect ratio limit of the photolithography process used. Its optimization would enable narrower bridges, shorter sacrificial etch times, and higher capacitance densities.

Figure 8a illustrates the combination of bridges and supports into a single structure, and Figure 8b illustrates the emergence of the bridge-support structure during the sacrificial etch.

The expected capacitance of the devices was calculated using a parallel-plate approximation over the surface of the anode. The anode surface area A_a is approximated as

$$A_a = \left[(2N_K - 1)A_{fK} - (2N_K - 2)A_{fC}\right] + \frac{h}{2N_K - 1}\left[N_K P_K + (N_K - 1)P_C\right] \quad (1)$$

The first addend in the expression accounts for horizontal surfaces, while the second addend accounts for vertical surfaces. N_K is the number of nickel layers, h is the total anode height, P_K and P_C are, respectively, the perimeter of the nickel and copper layers, and A_{fK} and A_{fC} are the flat (chip) area of, respectively, the nickel and copper layers. Uniform etching was assumed in determining the geometrical parameters A_{fC}, A_{fK}, P_C, and P_K. For the 110-layer anode shown in Figure 4, with a 100 nm Al_2O_3 dielectric layer, the capacitance density has a theoretical maximum of 45 nF/mm^2.

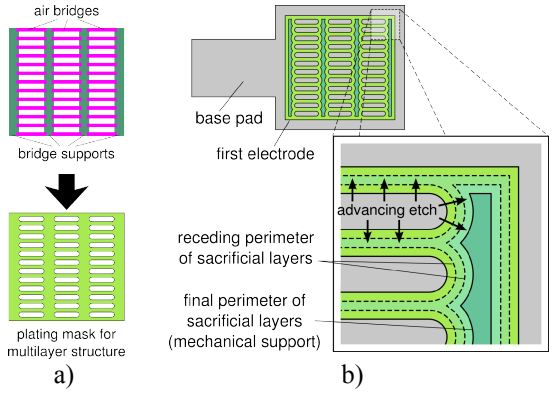

Figure 8: Air bridge-based electrode design. a) merging of bridges and supports into a single structure; b) selective release of air bridges during sacrificial etch

CAPACITOR CHARACTERIZATION

Figure 9a shows a schematic of the characterization experiment as well as the device model. A function generator produced a 1.5 V square wave. A current sense resistor, R_S, was used to observe the current flowing in the device. An oscilloscope was used to capture the resulting waveforms, from which the device model parameters could be extracted. Figure 9b shows typical results. This measurement approach allowed qualitative confirmation of the devices' functionality while also providing for quantitative measurement. Table 1 contains the results of the characterization.

The parallel leakage current G was measured with a sense resistor. Two sense resistors for R_S were used: R_{S1} and R_{S2} (380 and 760 Ω). From these two data points, the series resistance R_E and capacitance C were determined using the closed-form expressions

$$R_E = \frac{\tau_2}{\tau_1 - \tau_2} R_{S1} + \frac{\tau_1}{\tau_2 - \tau_1} R_{S2} \qquad (2)$$

$$C = \frac{\tau_1 - \tau_2}{R_{S2} - R_{S1}}$$

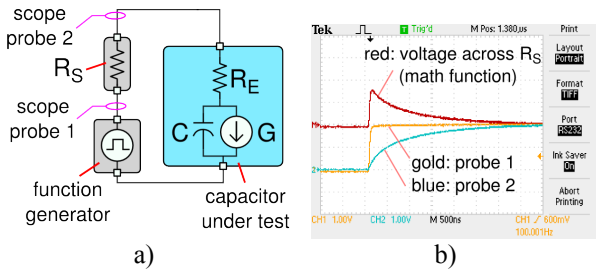

Figure 9: Device characterization: a) schematic and b) typical waveforms

Table 1: Characterization Results

Device	Expected capacitance	Measured device parameters			Capacitance density
		C	G	R_E	
1*	3.7 nF	1.09 nF	2.11 µA	83 Ω	0.50 nF/mm²
1	3.7 nF	3.53 nF	3.42 µA	195 Ω	1.61 nF/mm²
2	4.6 nF	3.33 nF	2.89 µA	435 Ω	1.52 nF/mm²

** measurement taken prior to vacuum infiltration of liquid cathode; all other data after cathode infiltration*

τ_1 and τ_2, the time constants associated with the two sense resistors, were extracted from the exponential regimes of the captured waveforms.

The capacitor values were well within range of their expected values, given the numerous sources of uncertainty in the devices' fabrication. The dramatic increase in capacitance seen with infiltration of the second electrode confirms the successful utilization of high aspect-ratio topology on the anode's surface. The leakage currents were much higher than would be expected due only to gigaohm-range resistivity of the Al_2O_3 layer. The leakage current was found to be insensitive to applied voltage, suggesting that it was due to electrochemical interaction between the anode and the electrolyte. This validated the assumed device model, but clearly indicates a severe obstacle to practical application of these devices. The series resistance values are also prohibitively high, but with improved second electrode materials, these figures should be readily decreased.

CONCLUSIONS

A new type of capacitor is presented, offering a density of 1.5 nF/mm² with a high degree of IC fabrication compatibility. The capacitors also demonstrate the utility of automated multilayer electroplating as a way to implement large amounts of surface area in a small amount of volume and chip area.

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