Micro-fabricated thin-film inductors for on-chip power conversion

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Abstract

This paper reports an optimized design and micro-fabrication approach for silicon-integrated elongated-spiral inductors for on-chip power conversion. The inductors are designed for high-power-density and high-efficiency DC-DC converters which transfer 25 W of power at frequencies between 5 and 30 MHz. The predicted power density of the inductors is close to 1 W/mm^2 with predicted overall converter efficiencies exceeding 90%. A Co-Zr-O multilayer thin-film magnetic material surrounds the planar copper windings of the inductor within etched silicon trenches. Materials and most processing steps have been experimentally verified. The miniaturization and integration of high-efficiency inductors on silicon can enable radical reductions in the size and cost of power converters for a myriad of applications.

1 Introduction

The integration and miniaturization of inductors has become a major focus of the power electronics community as the demand for high-performance low-volume converters has grown. Efficient power conversion circuits most often rely on magnetic components for energy storage; however, inductors and transformers are generally the largest and most lossy elements in these systems. Integrating inductors remains a primary challenge in achieving monolithic solutions for power conversion. Small and efficient magnetic components, and thereby converters, can increase the penetration of energy-saving technologies such as LED lighting by driving down system costs while increasing performance and efficiency [1].

Efforts to achieve chip-scale integration of inductors have taken advantage of thin-film materials to engineer magnetic cores [2, 3, 4, 5]. Thin-film magnetic materials operating at high frequencies can exhibit high saturation flux density and high resistivity [6]. These characteristics enable magnetic components to operate at higher power levels for a given footprint while minimizing hysteresis and eddy current losses. Further decreases in component size can be realized by increasing the switching frequency of the power converter [7]. The miniaturization of high-performance converters can thus be achieved by combining the benefits of thin-film magnetics materials with microfabrication techniques and high-frequency resonant converter topologies [8].

This paper describes the modeling, design, optimization, and fabrication of multi-turn inductors with multilayer nanogranular cores operating at high efficiencies. We investigate designs for high-performance thin-film power inductors fabricated on a silicon substrate using a Co-Zr-O nanogranular magnetic core material [9]. Previous work with this thin-film material has focused on single-turn V-groove inductors designed for low-voltage high-current power delivery applications [5, 10]. V-groove inductors can be embedded in thin-film packaging or integrated on the same die as silicon power devices, enabling the co-packaging of the entire power converter.

DC-DC converters designed for power delivery to LED lighting systems require larger inductances than can be practically fabricated using the V-groove technology. This requirement has driven the development of planar elongated-spiral inductors — multi-turn components with higher inductances than the V-groove inductors. This paper discusses the modeling and design of multi-turn racetrack inductors, illustrated in **Figure 1**, including a comprehensive model of the energy loss mechanisms in the inductor over a wide range of geometries. Additionally we describe the optimization of our inductor geometry to achieve high-performance operation in power converter circuits. Partially completed inductors are shown along with a fabrication plan for our components. Our racetrack inductors are predicted to achieve similar performance levels to our previous V-groove technology despite realizing significantly

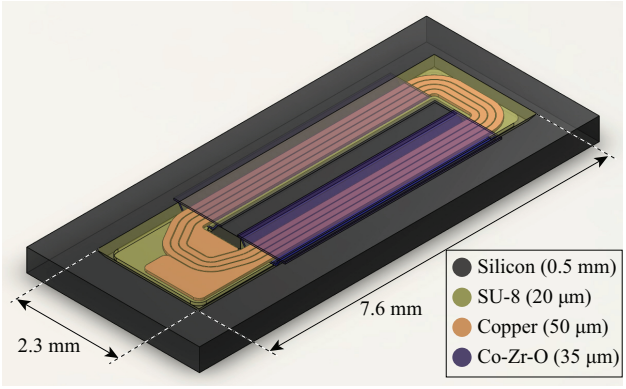


Figure 1 Illustration of an elongated-spiral inductor. Copper turns are surrounded by Co-Zr-O magnetic material within etched silicon trenches. The thickness of each material is shown above.

higher impedances. High-efficiency miniaturized inductors will support integrated DC-DC converters with applications in solid-state lighting and many other systems.

2 Modeling

A comprehensive model of the energy loss mechanisms in a racetrack inductor over a wide range of component dimensions was developed. The racetrack inductor uses the sloping sidewalls of an anisotropically-etched silicon channel to surround a copper winding with magnetic material (see **Figure 2**). The fabrication of these inductors will be described in Section 4.

Many of the loss mechanisms in multi-turn racetrack inductors are identical to those described in the models previously developed for V-groove inductors [11, 12, 13]. We have built a series of new models that account for eddy current and skin effects in both the copper windings and magnetic core layers. Finite-element simulations were used to validate the winding and core loses models for the racetrack inductor.

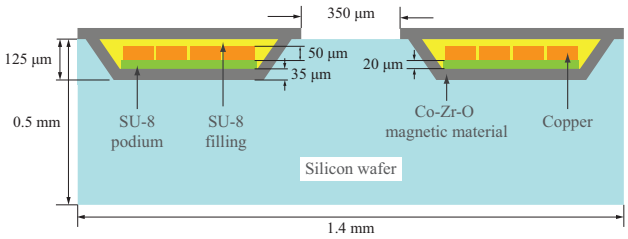


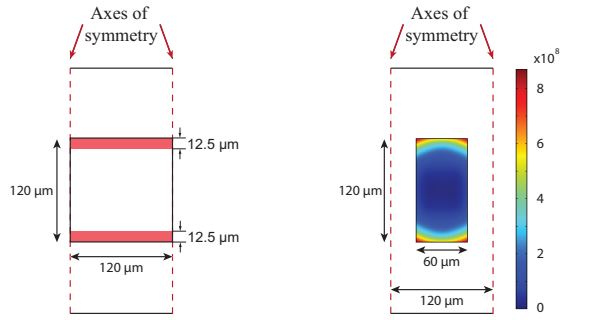
Figure 2 Illustration of racetrack inductor design.

2.1 Winding loss model

AC power losses in the conductive winding of a racetrack inductor are the result of skin effects, eddy currents, and an unequal balance of the magnetic field within certain regions of the winding. To understand how these factors impact winding losses, we first consider an inductor with an infinite number of turns where there is no gap between neighboring turns. At high frequencies, the current in such a winding, illustrated in **Figure 3(a)**, is confined to a layer of thickness $\delta = \sqrt{\rho/(\pi f \mu_0)}$, called the skin depth, along the top and bottom edges of a turn. In this expression, ρ is the conductor resistivity, f is the frequency of the current waveform, and μ_0 is the permeability of free space. The AC winding losses for such an idealized inductor are therefore quite predictable: the power loss (on a per meter basis) is simply

$$P_{loss} = \frac{\rho \cdot I_{ac,rms}^2}{2\delta \cdot w_{turn}} \tag{1}$$

where $I_{ac,rms}^2$ is the AC RMS current value and w_{turn} is the width of a turn. Such a winding design cannot be realized due to micro-fabrication constraints and the need for insulation between neighboring turns. When a gap is



(a) Idealized current distribution. **(b)** Simulated current distribution (A/m^2).

Figure 3 Current distribution at 30 MHz in an idealized winding with no gap between turns and a simulation result for a winding with a moderately-sized gap.

placed between turns, the magnetic flux lines incident upon the windings cause current to crowd in the outer corners of the windings, as seen in the simulation result in Figure 3(b). It is thus necessary to use finite-element simulations to determine the current distribution in the windings. 13,000 such simulations, normalized over frequency, were performed in COMSOL for winding geometries where the conductor thickness and width and the gap between turns was varied from $0.1{\cdot}\delta \leq X \leq 100{\cdot}\delta$. A look-up table was generated with the resulting AC resistance values over a wide range of geometries.

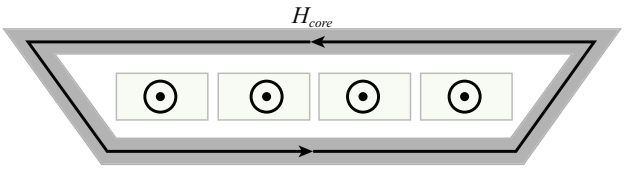
To create a model for an inductor with a finite number of turns, we must consider the magnetic field effects in the outer-most and inner-most regions of the winding window. Let us examine a winding with four turns, as shown in **Figure 4**. We assume a uniform magnetic flux throughout the core given by $\Phi = Ni/\mathscr{R}$, where N is the number of turns, i is the current through the winding, and $\mathscr{R}$ is the reluctance of the magnetic core. The magnetic material in the core is approximated as linear and gap reluctance is neglected. The magnetic field strength, H_{core}, is therefore uniform through the core. By Ampere's law, the field strength can be written as $H_{core} = Ni/l_{core}$, where l_{core} is the length of the loop through the center of the core that encircles the windings in Figure 4(a).

Since we have approximated H_{core} as constant through the core, the total MMF drop is evenly spread along the closed loop through the core.

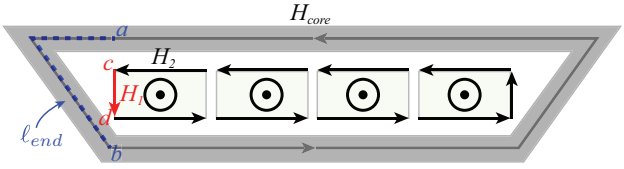
Conduction losses can be calculated analytically by approximating the tangential magnetic field strength along each edge of a winding as constants H_1 and H_3 (see Figure 4). The resulting power loss is

$$P = R_{dc}\zeta h_w^2 \left[\left(H_1^2 + H_3^2\right) \cdot G_1(\zeta) - 4H_1H_3 \cdot G_2(\zeta)\right] \tag{2}$$

where R_{dc} is the DC winding resistance, h_w is the height of the winding, $\zeta = w_{turn}/\delta$ [14, 15]. G_1 and G_2 are

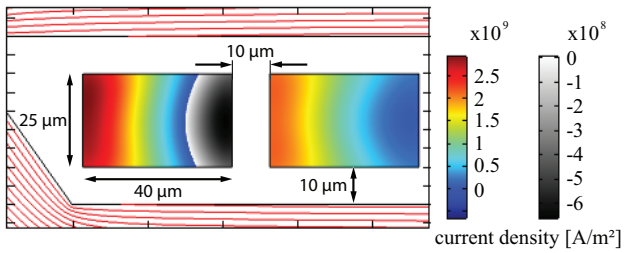


(a) Uniform magnetic field throughout core. Illustration not to scale.



(b) Magnetic field strength along edge of conductor.

(c) Negative current flows along inner edge of winding.



(d) Simulation at 30 MHz of current distribution in the winding. Positive current is shown in color, and negative current is shown in grayscale.

Figure 4 AC winding losses due to unbalanced MMF drop around the winding.

defined by

$$G_1(\zeta) = \frac{\sinh(2\zeta) + \sin(2\zeta)}{\cosh(2\zeta) - \cos(2\zeta)}$$
$$G_2(\zeta) = \frac{\sinh(\zeta)\cdot\cos(\zeta) + \cosh(\zeta)\cdot\sin(\zeta)}{\cosh(2\zeta) - \cos(2\zeta)}. \quad (3)$$

The magnetic field strength H_1 can be estimated by considering an Amperian loop surrounding the conductors along their edges. This closed path encircles the same amount of total current as the core, and the MMF dropped along segments of its length can be related to the MMF dropped within the core. The MMF dropped along the horizontal edges of each turn is assumed to be equal to the MMF dropped over a line segment of the same length in the core; this implies that $H_2 = H_{core}$. Integrating along the vertical edge of the outer turn in Figure 4(b),

$$\int_a^b \vec{H}_{core}\cdot\vec{dl} = \int_c^d \vec{H}_1\cdot\vec{dl}. \quad (4)$$

Simplifying this equation, we find $H_1 = \ell_{end}H_{core}/h_w$, where ℓ_{end} is the length of the path through the core labeled in Figure 4(b).

H_3 can be calculated by integrating around an Amperian loop surrounding an individual turn. The resulting value of H_3 is a negative number, meaning that current flows in a direction that opposes the main flow of current through the conductor, as shown in Figure 4(c). The net current through the conductor does not change; excess current flows through the outer and inner edges of the conductor resulting in higher AC winding losses. This effect propagates through all the turns in the winding but diminishes in the central turns, as seen in Figure 4(d).

The total AC winding loss in a racetrack inductor is the sum of the two loss effects described above: current crowding along the horizontal edges and an increased MMF drop along the vertical edges of the conductor. The net conduction losses in the winding were simulated (see Figure 4(d)) and agreed with the losses predicted by summing the two individual model results with less than 5% error. The AC conduction losses can be accurately estimated over a wide range of inductor geometries with an arbitrary number of turns in the winding.

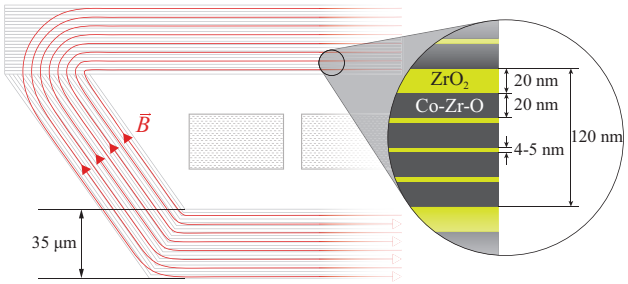
2.2 Core loss model

A detailed model of the high-frequency loss mechanisms in the magnetic core surrounding a racetrack inductor was developed. The magnetic core is constructed from a sputtered multi-layer thin-film Co-Zr-O material [9]. This material is an ideal choice for high-frequency integrated magnetics due to its high resistivity and high saturation flux density [16]. Our core loss model accounts for eddy current effects throughout the core — and specifically at the magnetic vias — in addition to hysteresis losses. Comprehensive models of eddy losses due to displacement currents and hysteresis losses in thin-film magnetic materials were previously completed and have been applied to this new inductor geometry [12, 13]. Material properties and modeling parameters for thin-film Co-Zr-O magnetic cores can be found in [13]. We have expanded on these models by analyzing the losses in the magnetic vias of silicon-integrated racetrack inductors.

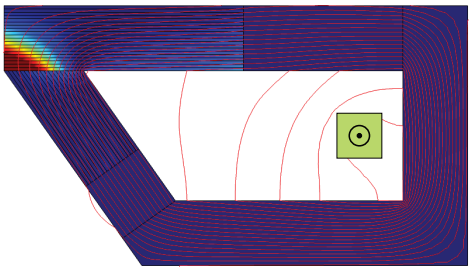
Multi-layer thin-film magnetic cores are designed to minimize eddy currents by separating magnetic layers with insulating material (ZrO_2 ceramic layers in **Figure 5(a)**). When flux lines travel parallel to the sputtered layers, as they do through the majority of the core, eddy currents are abated by the insulating layers and losses are minimized in the material. In our fabrication process, magnetic layers are sputtered along the base and sidewalls of the silicon channel simultaneously. In the final processing step, magnetic material is sputtered in horizontal layers to complete the magnetic path. This results in discontinuous magnetic layers at the via edges — shown in Figure 5(a).

Finite-element simulations were performed to quantify the eddy current losses in the magnetic vias. Simulations were run over a wide range of frequencies and the data were fit with a curve according to the equation

$$P_{eddy} = 4z_{core}\cdot k f^2 B_{max,ac}^2 \quad (5)$$



(a) Flux lines through magnetic vias. 4-5 μm ZrO_2 layers prevent columnar growth during sputtering process and 20 nm ZrO_2 layers block eddy current circulation [9].



(b) Simulated eddy losses in multi-layer core material.

Figure 5 Flux lines through the magnetic vias cross Co-Zr-O layers and induce eddy losses in the core.

where z_{core} is the length one core section into the page in Figure 5, k is a curve-fitting modeling constant, f is the frequency of the current waveform, and $B_{max,ac}$ is the peak AC flux density in the core. The factor of 4 accounts for the total losses across both core sections in the racetrack design. The value for the curve-fitting constant k was $k = 1.72 \times 10^{-12}$ W·sec^2·m^{-1}·T^{-2} calculated in the 5 to 30 MHz frequency range for a 35 μm-thick Co-Zr-O film with resistivity 550×10^{-8} Ω·m.

3 Optimization

We have outlined a comprehensive loss model for racetrack inductors which estimates power losses for any desired geometry. This model was coupled with a circuit loss model in a particle swarm optimization algorithm to determine the ideal geometric and circuit parameters to minimize the cost function $\mathcal{C}$,

$$\mathcal{C} = P_{loss} + \mathscr{Y} \cdot V_{ind} \tag{6}$$

where P_{loss} is the total power loss, $\mathscr{Y}$ is a weighting factor, and V_{ind} is the inductor volume. This cost function minimized the inductor footprint and power loss, with the priority between those two set by the weighting factor $\mathscr{Y}$. The parameters listed in **Table 1** defined the search space for designs which the constrained optimization algorithm could test.

Increasing switching frequency and using magnetic material reduces inductor volume and boosts power density; however, higher power handling per unit area can degrade efficiency [13]. It is therefore important to consider the tradeoff between power density (power per unit substrate area) and converter efficiency. Adjusting the weighting factor $\mathscr{Y}$ in Equation 6 between 0 and 1 allows optimal designs to be discovered at various points along a tradeoff curve (see **Figure 6**). The efficiency and power density of these inductors is similar to the results from our V-groove technology, despite achieving much larger impedances using this new racetrack design [17]. Our V-groove inductors have been compared to other integrated inductors published in the literature [17]. Capacitance values were determined using a simple parallel-plate model. A breakdown of the losses for the highlighted design in Figure 6 is shown in **Figure 7**. The numerical optimization method outlined above, which uses our comprehensive loss model, can determine optimal inductor geometries which maximize converter efficiency and power density.

Parameter	Low	High	Units
Switching frequency	3	30	MHz
Number of turns	2	12	
Insulator thickness	3	30	μm
Conductor thickness	20	100	μm
Gap aspect ratio	1	4	$\frac{h_{gap}}{w_{gap}}$
Max. flux density	0.1	1	T
Component capacitance	5	100	pF

Table 1 Optimization parameters.

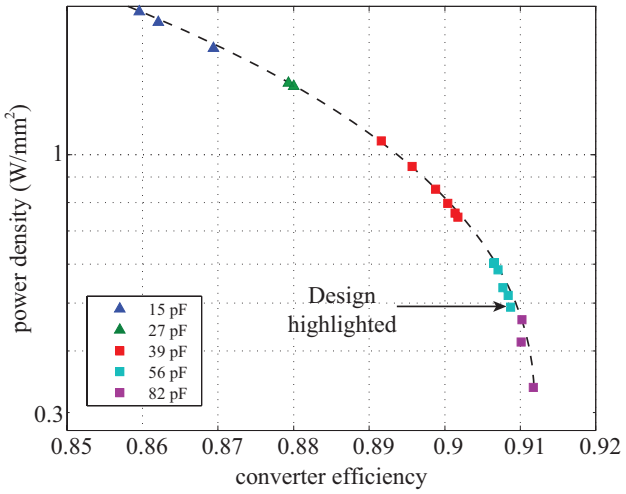


Figure 6 Optimized inductor designs which maximize the power density for a given converter efficiency. The capacitance at which this performance is achieved is listed for each point.

4 Fabrication

A micro-fabrication approach for elongated-spiral inductors integrated on silicon was developed and many steps have been tested. The primary steps involved in the fabrication of these components are illustrated in **Figure 8**.

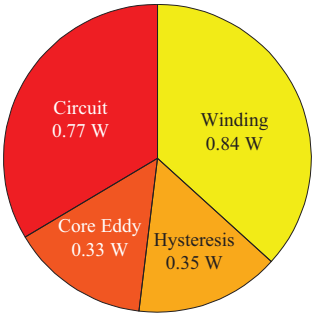


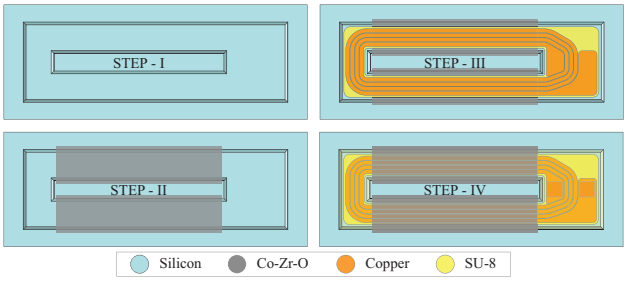
Figure 7 Predicted loss breakdown for an optimized inductor which achieves an efficiency of 91% and power density of 0.55 W/mm^2 for a 6-turn 1 μH design operating at a frequency of 6.4 MHz and a saturation flux density of 0.6 T.

We process silicon wafers with the <100> crystal plane exposed. A thick thermal oxide layer is grown on the surface of the wafers. The oxide is then patterned with the mask shown in **Figure 9(a)**. This mask incorporates corner compensation patterns to prevent undercutting in the silicon [18].

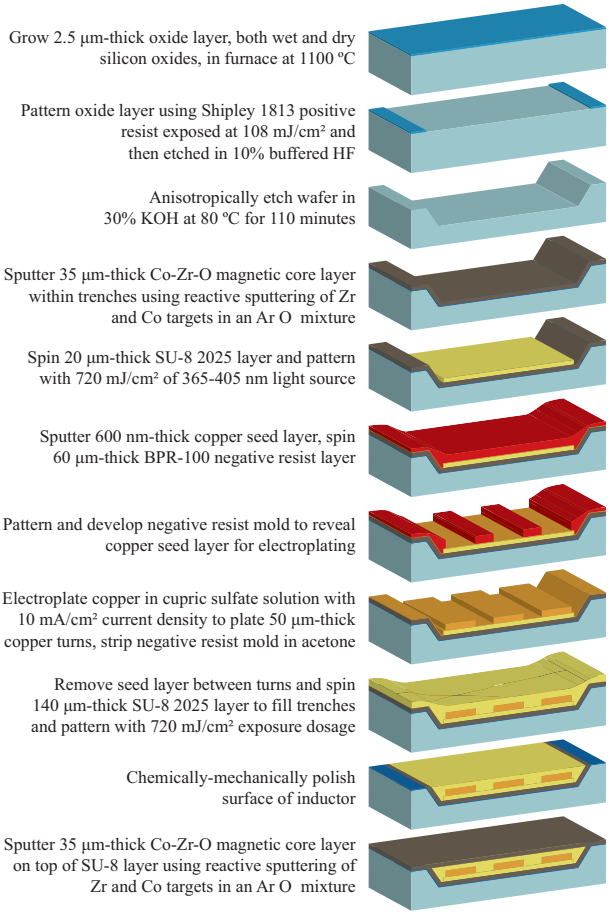
Wafers are anisotropically etched in a 40% weight concentration potassium hydroxide (KOH) solution to produce 140 μm-deep trenches with 54.7°sloping sidewalls [19], as shown in Figure 9(b). During the etching process, the wafers are agitated in an ultrasonic bath to improve the surface morphology at the bottom of the trenches [20].The directionality of the wafer in the solution was crucial in producing smooth surfaces in the etching process. Placing the wafers with the longer edge of the trenches normal to the base of the beaker produced smoother channels. 4 μm-tall remnants of the corner compensation pattern can be seen in the bottom of the trenches in Figure 9(b) — a result consistent with [18]. These remnants will be covered immediately by SU-8 in the completed inductor and will therefore not hinder device performance.

After anisotropic etching, an oxide layer is thermally grown to insulate the silicon wafer from the magnetic material. A 35 μm-thick Co-Zr-O core is reactively sputtered along the bottom and sidewalls of the trenches. A stainless steel shadow mask is positioned above the wafer to sputter two electrically-isolated magnetic cores. An inductor processed through this step is shown in Figure 9(c), although the core thickness in this example is only 10 μm.

A dielectric layer of SU-8 epoxy is then spun over the entire device to electrically insulate the coils from the core with a thickness based on the specification for the maximum tolerable capacitance. Copper turns are then electroplated through a negative resist mold. In the final fabrication steps, an SU-8 dielectric layer fills the remainder of the trench and the component is planarized. A 35 μm layer of magnetic material is sputtered to complete the magnetic path surrounding the windings. Preliminary testing has demonstrated good performance from our Co-Zr-O magnetic films up to 150 °C.



(a) Birds-eye view of the primary micro-fabrication steps.



(b) Detailed list of processing steps.

Figure 8 Outline of the primary processing steps for inductor fabrication. A silicon wafer is anisotropically etched **(I)**, a layer of magnetic material is sputtered **(II)**, the conductor is patterned **(III)**, and a final layer of magnetic material completes the inductor **(IV)**.

In addition to the magnetic material deposition shown in Figure 9(c), we have tested the molding and electroplating of the copper windings within silicon trenches. This result, for a component fabricated without magnetic material, is shown in **Figure 10**.

5 Conclusion

This paper describes the design, modeling, optimization, and fabrication of racetrack inductors integrated on sili-

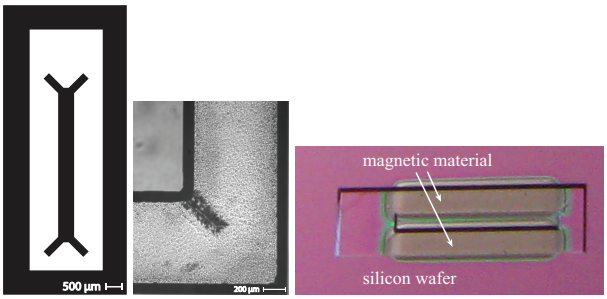


Figure 9 Anisotropic silicon etch mask with corner compensation **(a)**. Results for trenches etched to a depth of 140 μm **(b)**. Magnetic material deposited with a shadow mask **(c)** to produce two independent magnetic core sections.

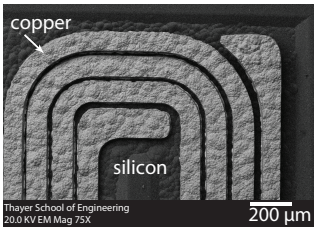


Figure 10 Partially-completed inductor. Roughness in the copper layer resulted from poor anisotropic etching of the silicon, an issue which has been resolved through ultrasonic agitation and wafer positioning during etching.

con substrates with Co-Zr-O magnetic cores. A detailed loss model for the inductors was presented along with an overview of the fabrication procedures used to build these components. Optimized inductor designs —determined through computational optimization — were shown over a range of power converter efficiencies and power densities. Designs exceeding efficiencies of 90% with power densities approaching 1 W/mm^2 are predicted from our models. Partially-completed inductors and fabrication results were presented. The remaining fabrication steps are currently being refined and tested. Completed inductors will be tested with small-signal methods and in a power converter circuit. Silicon-integrated racetrack inductors with thin-film magnetic cores can enable the miniaturization and proliferation of low-cost integrated DC-DC converters with a myriad of applications.

Acknowledgments

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