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Low-loss microelectrodes fabricated using reverse-side exposure for a tunable ferroelectric capacitor application

Yong-Kyu Yoon[1], J Stevenson Kenney[1], Andrew T Hunt[2] and Mark G Allen[1]

[1] Georgia Institute of Technology, School of Electrical and Computer Engineering, Atlanta, GA 30332, USA

[2] nGimat Co., 5315 Peachtree Industrial Boulevard, Atlanta, GA 30341, USA

E-mail: yongkyu.yoon@ece.gatech.edu

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Abstract
Narrowly spaced thick microelectrodes are fabricated using a self-aligned multiple reverse-side exposure scheme for an improved quality-factor tunable ferroelectric capacitor. The microelectrodes are fabricated on a functional substrate—a thin film ferroelectric (barium strontium titanate, BST; $Ba_xSr_{1-x}TiO_3$) coated sapphire substrate, which has an electric-field-dependent dielectric property providing tuning functionality, as well as UV transparency permitting an additional degree of freedom in photolithography steps. The microelectrode process has been applied to interdigitated capacitor fabrication, where a critical challenge is maintaining narrow gaps between electrodes for high tunability, while simultaneously forming thick electrodes to minimize conductor loss. A single mask, self-aligned reverse-side exposure through the transparent substrate achieves both these goals. A single-finger test capacitor with an electrode gap of 1.2 μm and an electrode thickness of 2.2 μm is fabricated and characterized. Tunability ($T = 100 \times (C_0 - C_{\text{bias}})/C_0$) of 33% at 10 V has been achieved at 100 kHz. The 2.2 μm thick structure shows improvement of Q-factor compared to that of a 0.1 μm thick structure. To demonstrate the scalability of this process, a 102-finger interdigitated capacitor is fabricated and characterized at 100 kHz and 1 GHz. The structure is embedded in a 25 μm thick epoxy resin SU-8 for passivation. A quality factor decrease of 15–25%, tunability decrease of 2–3% and capacitance increase of 6% are observed due to the expoxy resin after passivation. High frequency performance of the capacitor has been measured to be 15.9 pF of capacitance, 28.1% tunability at 10 V and a quality factor of 16 (at a 10 V dc bias) at 1 GHz.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Ferroelectric materials have been widely used for a variety of MEMS applications, which include micro sensors, actuators and transducers based on their piezoelectricity [1, 2], IR detectors based on their pyroelectricity [3, 4] and microwave components based on their favorable RF properties in the paraelectric phase [5, 6]. Barium strontium titanate (BST, $Ba_xSr_{1-x}TiO_3$) has been considered as one of the most attractive functional ferroelectric materials due to its high dielectric constant, large breakdown field intensity, low dielectric loss in a microwave regime and large electric-field dependency of permittivity. Examples of its usage include integrated memory devices [7, 8], decoupling components

[9, 10], capacitors for power electronics [11] and tunable RF components [12–19]. Its electrical properties vary to a large extent with the deposition method and environment, type of substrate and composition ratio of Ba and Sr, among other variables.

One approach to obtain high-quality BST thin film is to choose a well-matched substrate material and an epitaxial growth method for BST. As for substrates, magnesium oxide (MgO), lanthanum-doped aluminum oxide (LAO) or single crystalline aluminum oxide (Al_2O_3 or sapphire) is used for epitaxial growth of BST [20] while often sapphire or LAO is preferred to MgO in practical usage due to low cost. Those substrates also show high electrical isolation and low dielectric loss properties compared to a silicon substrate. There are many BST deposition methods currently in use such as RF sputtering, metal organic chemical vapor deposition (MOCVD), combustion chemical vapor deposition (CCVD), sol–gel or pulsed laser ablation (PLA), etc [21–24]. Among them, CCVD contains an additional advantage due to its open environment deposition without a need for a vacuum system [22].

The combination of an epitaxially grown thin BST layer by CCVD with a sapphire substrate allows a cost-effective functional smart substrate, which possesses the following features: a high dielectric constant, low-loss, large tuning power and UV transparency [25] which is useful for lithographic flexibility. The nominal dielectric constant of epitaxial BST on sapphire using CCVD is reported to be between 500 and 1000 with a tuning range ($\varepsilon_{r_max} : \varepsilon_{r_min}$) of 3:1–4:1 [15, 26].

The UV transparency of the substrate has been utilized here for the micromachining of thick microelectrodes by a self-aligned, reverse-side exposure technique. Usage of reverse-side exposure through the transparent substrate is reported in other fabrication processes as well, including thin film transistor (TFT) fabrication [27], field effect display (FED) fabrication [28] and SU-8 micro structures [29–33]. Since the reverse-side exposure takes advantage of a prepatterned opaque layer on the substrate in subsequent photolithography steps, the resultant self-alignment feature eases photolithography difficulties, minimizing alignment tolerance issues.

As an example, consider the interdigitated gap capacitor shown in figure 1. This capacitor comprises two microelectrodes in very close proximity and, in principle, requires only a single photomask. However, because the dielectric tunability of a ferroelectric capacitor depends on the electric field, small gaps between electrodes are necessary for high tunability for a given bias voltage. A thick electrode compared to the skin depth at the frequency of interest is also preferred for reducing conductor loss. A critical challenge in the fabrication of these same-surface interdigitated electrodes is maintaining narrow gaps for high tunability, while simultaneously forming thick electrodes to minimize conductor loss. In addition, some ceramic materials are too delicate for aggressive processing conditions such as acidic environment and therefore special care should be taken for electrode metallization and patterning on top of those materials. For example, BST is susceptible to acidic corrosion with most acids; often a lift-off process is used rather than metal deposition followed by acidic metal etching. While using a conventional lift-off process, it is difficult to fabricate tall and narrow gap electrodes due to the difficulty of forming high-aspect-ratio photoresist molds with the required pattern resolution; the self-aligned reverse-side exposure process alleviates its alignment efforts for the repeatable lift-off process for thick metallization. The utility of tunable capacitors includes phase shifters, tunable filters, voltage-controlled oscillators, frequency multipliers, mixers and phased array antennas [14, 15, 34, 35].

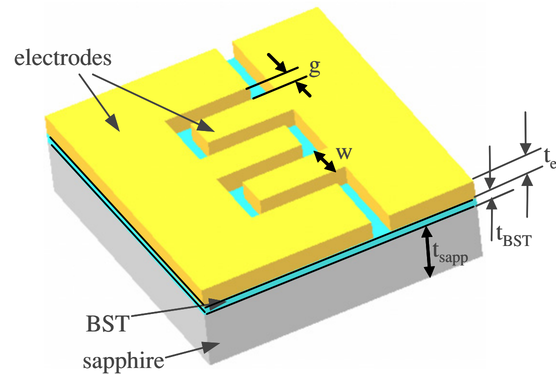


Figure 1. Structural schematic of an interdigitated gap capacitor on barium strontium titanate (BST) on a sapphire substrate.

In this paper, we first describe the fabrication of thick microelectrodes for a highly tunable capacitor based on epitaxially grown BST on a sapphire substrate. A single mask process and a repeatable self-alignment technique using reverse-side exposure through the transparent substrate combined with lift-off processes are employed to achieve both narrow gaps and thick electrode patterning. An additional benefit of the process is that the BST is passivated from aggressive processing conditions throughout the process, thereby maintaining its properties. Second, fabricated single digit BST gap capacitors are characterized and modeled with regard to capacitance as a function of bias voltage and gap. Lumped parameters for an equivalent circuit in the frequency range of 0.1–6 GHz are determined, giving a representative Q-factor for thin and thick electrode capacitors. Third, the scalability of the developed process is tested with multidigitated tunable capacitors. The fabricated multidigit capacitor is embedded in an epoxy resin for passivation, and additional polymer effects are characterized.

2. Fabrication

An R-plane sapphire (500 μm thick) with an epitaxially grown $Ba_{0.6}Sr_{0.4}TiO_3$ thin layer using CCVD has been chosen for a substrate, which is provided by nGmat Co. (Atlanta, GA). The CCVD technique allows epitaxial growth of BST in non-vacuum conditions. The epitaxial BST layer is approximately 500 nm thick. Copper (Cu) is used as the conductor material. The target value of electrode thickness t_e is 2 μm in figure 1, which is approximately one skin depth of copper at 1 GHz. For high tunability at a given bias voltage, the gap g should be small, and is targeted to be 1–2 μm in width. The fabrication process is shown in figure 2. This process is based on reverse-side exposure through a transparent substrate

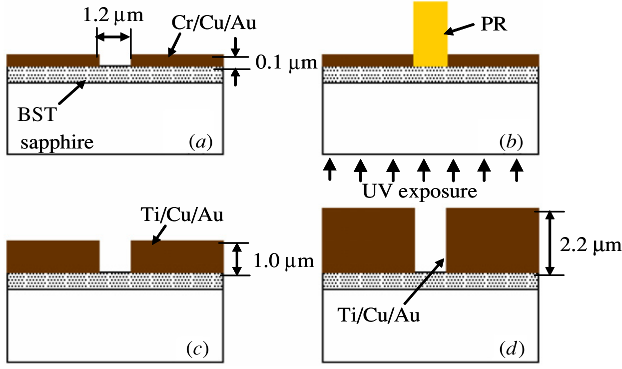


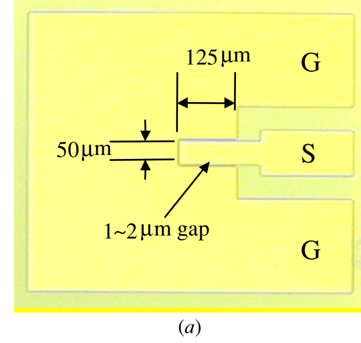
Figure 2. The fabrication process.

combined with repeated lift-off steps, and allows for the fabrication of thick metal electrodes while simultaneously maintaining small electrode gaps. Negative tone photoresist (NR9_1000PY, Futurrex, Inc.) is spin coated to a thickness of 1 μm on BST film and patterned. In a lift-off process, first metal layers (Cr/Cu/Au, 20 nm/100 nm/20 nm) are deposited and the photoresist removed (figure 2(*a*)). Chromium is used as an adhesion layer between the substrate and the subsequent copper layer, and the top gold layer is employed for oxidation protection. A second negative photoresist (NR9_1500, Futurrex, Inc.) is then spin coated to a thickness of 3 μm and baked. The photoresist is then exposed from the reverse side. Since the sapphire substrate and the BST thin layer are transparent, and the first metal layer is opaque, a self-aligned mold is opened in the negative photoresist over the first deposited metal layer (figure 2(*b*)). This mold can then be filled either using electroplating or subsequent lift-off steps to create thick, self-aligned electrodes. In this work, multiple lift-off processes are employed for isolated electrodes patterning since electroplating needs a conductor path while the electrical path for isolated electrodes requires an additional fabrication step. Ti/Cu/Au (20 nm/900 nm/30 nm) is deposited using a standard lift-off process followed by photoresist removal (figure 2(*c*)). A third metallization of Ti/Cu/Au (20 nm/1 μm/200 nm) and lift-off has been carried out to further increase metal thickness and the fabrication is complete (figure 2(*d*)). The reverse-side exposure approach can eliminate the need for repeated alignments, while simultaneously preserving the possibility for multilayer film deposition.

The fabricated narrowly spaced thick electrodes for a single digit gap capacitor have been shown in figure 3. The gap capacitor has a coupling length l of 300 μm as shown in figure 3(*a*). Figures 3(*b*) and (*c*) show a capacitor with a gap g of 1.2 μm and a thickness t_e of 0.1 μm after the first lift-off process and one with a gap g of 1.2 μm and a thickness t_e of 2.2 μm (1.8:1 gap aspect ratio) after the third lift-off process.

3. Characterization

The fabricated microelectrodes on the BST/sapphire substrate are not independently characterized but since their properties are merged with the capacitor characteristics,



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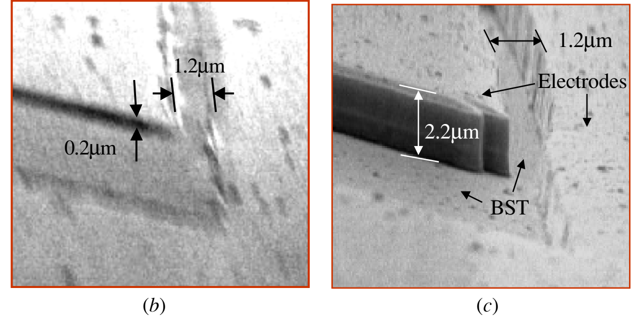


(*b*) (*c*)

Figure 3. A fabricated single digit gap capacitor: (*a*) 1.2 μm gap and 300 μm coupling length, (*b*) SEM picture of the gap area after the first lift-off (0.1 μm thick metal) and (*c*) after the third lift-off (2.2 μm thick metal).

the characterization of the fabricated tunable capacitor is performed instead. In this section, the substrate tuning, electrode gap effect and electrode thickness effect of the tunable ferroelectric gap capacitor are examined and its characteristics are described using literature-derived phenomenological equations.

A structural schematic of an interdigitated gap capacitor architecture is shown in figure 1. Two electrodes with thickness t_e and gap g are formed on top of high dielectric constant ferroelectric BST which has been epitaxially grown on a sapphire substrate.

3.1. Capacitance as a function of bias voltage

The dielectric permittivity of a ferroelectric material varies with the electric field. An analytical form of this dielectric permittivity dependence has been reported [36, 37], in which the permittivity dependence in a simplified form is ($\varepsilon^{-1} \propto 1 + kE^2$), where E is the electric field. When a gap capacitor is fabricated on a ferroelectric coated substrate, its bias voltage dependence follows this ε–E relationship while the total capacitance contains additional non-tunable contributions due to, e.g. the non-tunable substrate and air. For a certain temperature and geometry, a schematic capacitance versus bias voltage (C–V) curve is shown in figure 4. The resultant capacitance C and tunability T as a function of bias voltage can be expressed phenomenologically as in equations (1) and (2), respectively:

$$C(V) = C_{nt} + \frac{C_0 - C_{nt}}{1 + kV^2}, \qquad (1)$$

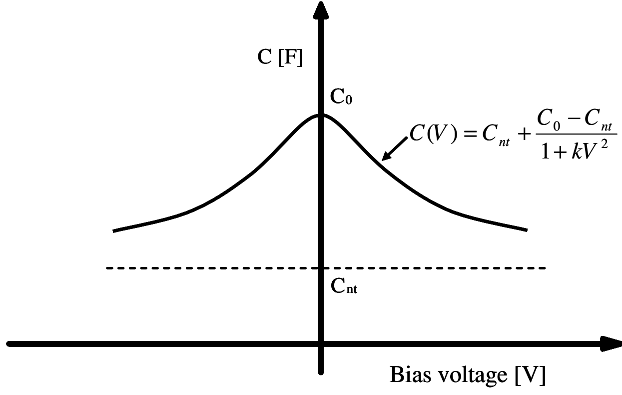


Figure 4. Schematic of capacitance as a function of bias voltage.

$$T(V) = \left|\frac{C(0) - C(V)}{C(0)}\right| \times 100$$
$$= \left|1 - \frac{C_{nt}}{C_0} - \frac{1 - C_{nt}/C_0}{1 + kV^2}\right| \times 100, \quad (2)$$

where C_{nt} is the non-tunable portion of the capacitance, C_0 is the zero bias capacitance and k is a material coefficient showing the extent of tuning. The coefficients (C_{nt}, C_0 and k) can be empirically determined.

3.2. *Capacitance as a function of gap*

The capacitance of a gap capacitor comprises three parts: one through the air, another through the substrate such as sapphire and the third through the ferroelectric layer such as BST. The total capacitance of these partial contributions has been previously described analytically using a conformal mapping approach [38–40]. Simplified forms of these capacitances are shown in equations (3)–(6) [39]:

$$C = C_{air} + C_{sapp} + C_{BST}, \quad (3)$$

$$C_{air} = \varepsilon_0 l \frac{2}{\pi} \ln\left(\frac{4(g + 2w)}{g}\right), \quad (4)$$

$$C_{sapp} = \varepsilon_0 l \frac{\varepsilon_{sapp} - 1}{\pi} \ln\left(\frac{16(t_{sapp} + t_{BST})}{\pi g}\right), \quad (5)$$

$$C_{BST} = \varepsilon_0 l \times \frac{\varepsilon_{BST} - \varepsilon_{sapp}}{g/t_{BST} + (4/\pi)(\ln 2)\sqrt{1 + 2\sqrt{2} \times 10^{-19}\varepsilon_{BST}/t_{BST}}}, \quad (6)$$

where C_{air}, C_{sapp} and C_{BST} represent the capacitance of the air, the sapphire substrate and the BST layer, respectively; ε_0, ε_{sapp} and ε_{BST} the permittivity of air, relative dielectric constant of sapphire and relative dielectric constant of BST, respectively; t_{sapp} and t_{BST} the thicknesses of sapphire and BST, respectively and l, g and w the coupling length, gap between electrodes and width of interdigital electrodes as shown in figure 1. When other material parameters are given, the capacitance as a function of gap can be calculated using these equations.

The capacitance can also be numerically calculated using finite element analysis. For example, the geometry used for two-dimensional (2D) electrostatic simulation (ANSYS 5.6) is shown in figure 5 with the following parameters.

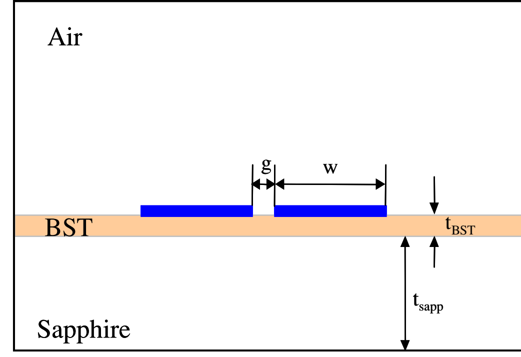
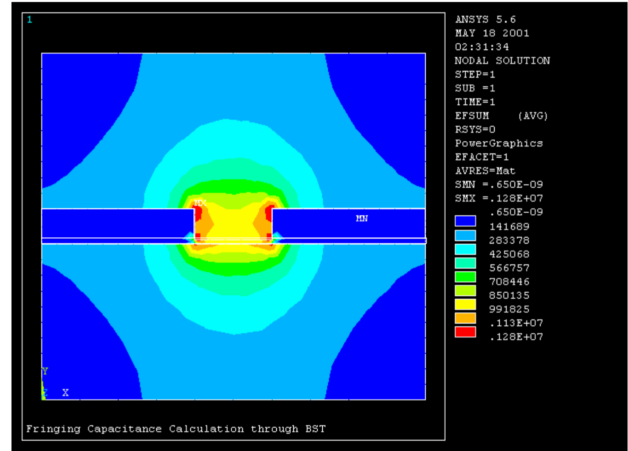
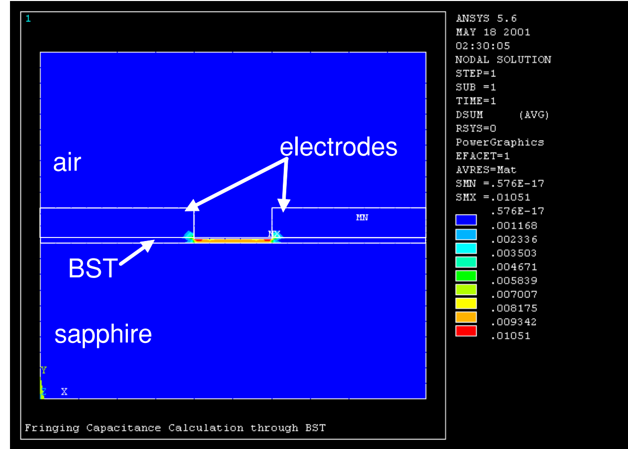


Figure 5. Capacitor geometry for 2D electric analysis.



(*a*)



(*b*)

Figure 6. Magnified view of the electric field and electric displacement distribution in the gap area with 5 μm gap: (*a*) electric field ($|\bar{E}|$) and (*b*) electric displacement ($\varepsilon|\bar{E}|$) (ANSYS 5.6).

- Relative permittivity of air ε_{air}: 1.
- Relative permittivity of sapphire ε_{sapp}: 10.
- Relative permittivity of BST ε_{BST}: 500–1000.
- Thickness of BST t_{BST}: 500 nm.
- Width of electrode w: 500 μm.
- Gap g: 0.5 μm–20 μm.

The electric field and electric displacement in the gap area are shown in figure 6. While a strong electric field is shown

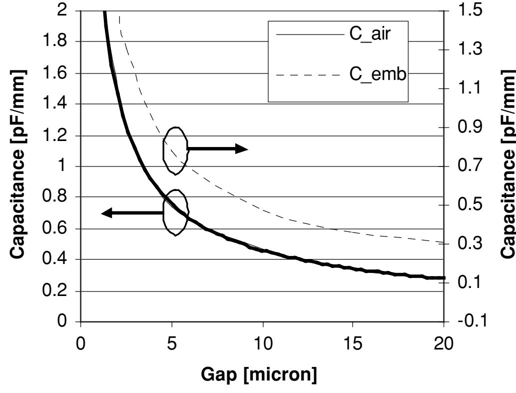


Figure 7. Capacitance as a function of gap; solid line shows without embedding and dashed line shows the effect of embedding in SU-8. Note each line uses a different *y*-axis in different scales, exaggerating capacitance difference.

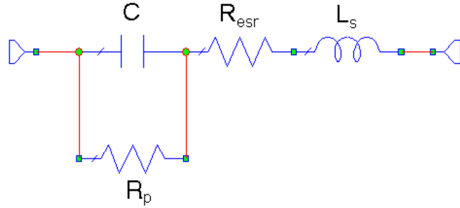


Figure 8. Equivalent circuit for gap capacitor.

in the gap area symmetrically between electrodes over the upper air region, the underlying ferroelectric BST region and the substrate region as shown in figure 6(*a*), strong electric displacement is concentrated only in the high dielectric BST layer of the gap area in figure 6(*b*). Based on the simulation, more than 80% of the total stored electric energy in the capacitor is attributed to the BST layer alone even though the thickness of BST is only 500 nm, when typical values of a relative permittivity of BST $\varepsilon_{\mathrm{BST}}$ of 800 and a gap g of 2 μm are used.

When the upper region is covered with a dielectric material (e.g. as might happen during passivation and subsequent packaging, resulting in an embedded capacitor), the capacitance increases due to the contribution of the embedding dielectric material. Figure 7 shows the capacitance as a function of gap in two cases: one without passivation (air ambient) and with passivation (SU-8 embedded, $\varepsilon_{\mathrm{SU\text{-}8}} \sim 3.5$). The capacitance with dielectric passivation shows a 2–10% increase over a 2–20 μm gap.

3.3. Quality factor

Practical passive components can be expressed by a combination of lumped circuit parameters (R, L and C). For example, a lumped circuit model of a practical capacitor includes the main capacitance C connected with a parallel resistance R_{p} representing a leakage loss, series parasitic inductance L_{s} and equivalent series resistance R_{esr} as shown in figure 8.

The total impedance is written as

$$Z = \mathrm{Re}(Z) + j\mathrm{Im}(Z), \tag{7}$$

where

$$\begin{aligned} \mathrm{Re}(Z) &= \frac{R_{\mathrm{p}} + R_{\mathrm{esr}} + \omega^2 C^2 R_{\mathrm{p}}^2 R_{\mathrm{esr}}}{1 + \omega^2 C^2 R_{\mathrm{p}}^2} \\ &= R_{\mathrm{esr}} + \frac{R_{\mathrm{p}}}{1 + (\omega C R_{\mathrm{p}})^2}, \\ \mathrm{Im}(Z) &= \frac{-\omega C R_{\mathrm{p}}^2 + \omega L_{\mathrm{s}} + \omega^3 L_{\mathrm{s}} C^2 R_{\mathrm{p}}^2}{1 + \omega^2 C^2 R_{\mathrm{p}}^2} \\ &= \omega L_{\mathrm{s}} - \frac{\omega C R_{\mathrm{p}}^2}{1 + (\omega C R_{\mathrm{p}})^2}. \end{aligned} \tag{8}$$

The quality factor Q is defined as the ratio of the energy stored in the device to energy dissipated per cycle. It is easily calculated for passive components in equation (9) if the complex impedances are known:

$$Q = \left| \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \right|. \tag{9}$$

In the high-frequency region, the real part of the impedance $\mathrm{Re}(Z)$ is dominated by R_{esr} while the imaginary part $\mathrm{Im}(Z)$ is approximated as $-1/\omega C$ as long as the operating frequency is below its resonant frequency and series inductance L_{s} is very small. Therefore, high Q-factor can be achieved by suppressing the equivalent series resistance R_{esr} existing in the frequency range of interest.

The equivalent series resistance R_{esr} in the RF range includes resistance for dielectric loss, dc resistance of electrodes, contact resistance and RF resistance of electrodes. Dielectric loss is a inherent property of dielectric materials and for a given material its extent is dependent on the deposition method and deposition condition of the dielectric. Epitaxially grown BST on a sapphire substrate is used in this work to ensure use of a high-quality material. DC resistance and metal contact resistance are considered independent of frequency while RF resistance is frequency dependent due to skin effect in the conductor; this portion of the total resistance can become significant at high frequency. It is desirable for the conductors of RF devices to be thick to minimize RF resistance; however, thicker conductors can result in increased fabrication complexity and provide diminishing benefit once the thickness greatly exceeds the skin depth at the operation frequency of interest. A conductor thickness corresponding to one skin depth at the frequency of interest has been chosen in this design.

3.4. Measurement and characterization of a single digit capacitor

The low frequency impedance of the fabricated gap capacitors is measured using a Keithley 3322 LCZ meter at 100 kHz. The capacitance and its tunability as a function of dc bias voltage for the capacitor of figure 3(*a*) (2.2 μm thickness) are plotted in figure 9. The coefficients (C_{nt}, C_0 and k) in equations (1) and (2) are empirically determined to best fit the measurement data and plotted in figure 9 as well. Modeling curves describe the measurement data well in the voltage range of 0 to 30 V. The coefficients used for the plot are summarized in table 1.

Several capacitors with various gaps (1.2 μm, 2.5 μm, 5 μm, 10 μm and 20 μm) have been fabricated and their impedance is measured at 0 and 30 V. Figure 10 shows the

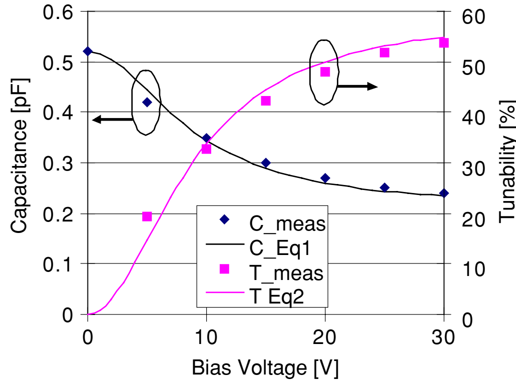


Figure 9. Capacitance and tunability of single digit gap capacitor (1.2 μm gap and 300 μm coupling length) structure.

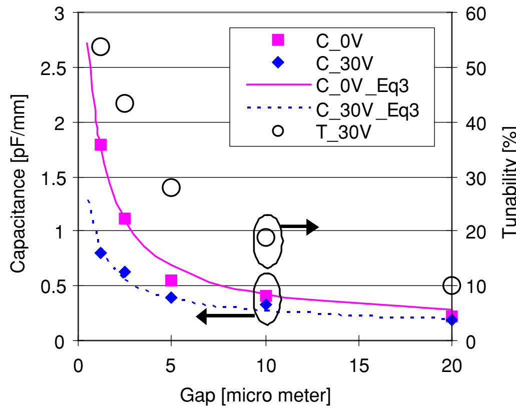


Figure 10. Capacitance and tunability as a function of gap; filled squares and diamonds show measured capacitance with 0 bias and 30 V, respectively, solid line and dashed line show simulated capacitance from equation (3) to equation (6) with 0 bias and 30 V, respectively, and empty circles show tunability at 30 V.

Table 1. Coefficients for capacitance and tunability curves of figure 9.

	C_{nt} (pF)	C_0 (pF)	k (V^{-2})
Capacitor in figure 3(*a*)	0.21	0.52	0.013

capacitance and tunability as a function of gap. A solid line, a dashed line, square marks and diamond marks show calculated capacitance with zero bias voltage, simulated capacitance with 30 V bias, measured capacitance with zero bias and measured capacitance with 30 V bias, respectively. Note that the capacitance of the fabricated samples is presented as a capacitance per unit length (pF mm^{-1}). The solid line in figure 10 is calculated using equations (3)–(6), where a dielectric constant of BST ε_{BST} of 700 and an electrode width w of 50 μm are used, while the dashed line is with a dielectric constant of BST ε_{BST} of 250. Capacitance and the percentage change of capacitance (tunability) of a narrower gap capacitor are higher than those of a wide gap capacitor as expected; namely, tunability benefits from a narrow gap.

The skin depth of copper at 1 GHz is approximately 2 μm and the thickness of the copper electrodes for the fabricated gap capacitors is 2.2 μm. To investigate the effect of electrode thickness on Q-factor, two gap capacitors

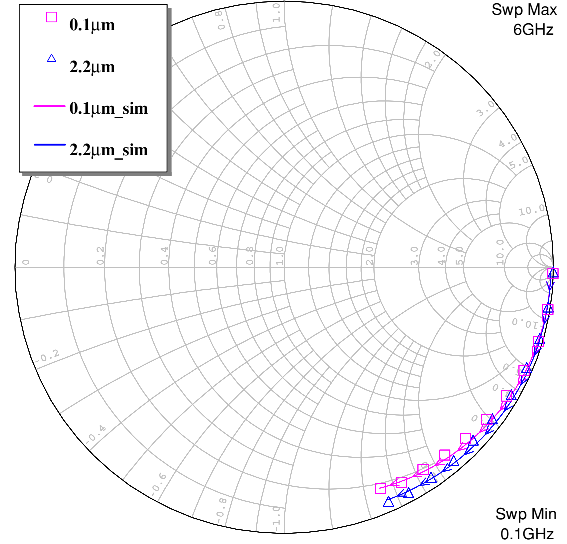
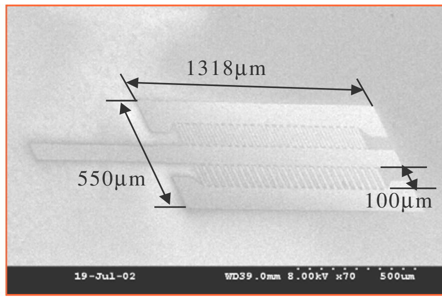


Figure 11. Smith chart of S-parameters for one-port gap capacitors with two different metal thicknesses; squares and triangles represent measured S-parameters for the 0.1 μm thick capacitor and 2.2 μm thick one, respectively. Solid lines show fitting curves between 100 MHz and 6 GHz.

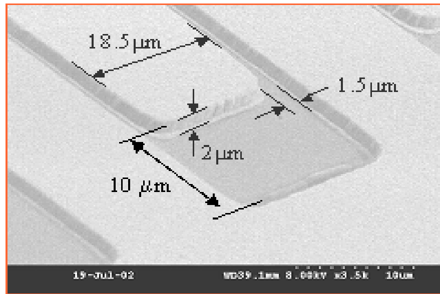
Table 2. Lumped parameters used for Q-factor calculation.

	C (pF)	R_p (Ω)	L_s (nH)	R_{esr} (Ω)	Q measured at 2.4 GHz
0.1 μm device	0.345	10^4	0.02	7.8	13.45
2.2 μm device	0.345	10^4	0.02	3.3	19.83

(one with 0.1 μm thick electrodes as shown in figure 3(*b*) and the other with 2.2 μm thick electrodes as shown in figure 3(*c*)) have been tested in the frequency range of 100 MHz–6 GHz. One-port scattering parameters are taken using an HP 8510 Vector Network Analyser and Cascade Microtech G-S-G probe systems after standard calibration. S-parameters are converted to Z-parameters and the Q-factors are calculated. The extracted capacitance includes both capacitance from BST of the gap area as well as parasitic capacitance from the pads or extended electrodes. More accurate capacitance measurement can be pursued using on-wafer de-embedding structures [41]. In this work, however, relative values of RF conductor loss due to different electrode thicknesses are of major concern, and this further de-embedding procedure has not been performed. The measured data and fitted data are plotted on the Smith chart in figure 11, where the square marks and the triangle marks represent the S-parameter plot of the 0.1 μm and 2.2 μm thick electrode capacitors, respectively. The structure with 2.2 μm thick electrodes shows low-loss performance. By fitting measurement data with the lumped circuit model of figure 8 numerically or using equations (8) and (9) in the frequency range of 0.1 GHz–6 GHz, the circuit parameters are determined and summarized in table 2. The equivalent series resistance R_{esr} for the 2.2 μm device is much smaller than that of the 0.1 μm device, resulting in Q-factor improvement.



(*a*)



(*b*)

Figure 12. SEM picture of a 102-finger interdigitated capacitor before embedding: (*a*) overall view and (*b*) magnified view.

4. Multi-interdigitated capacitor

Based on the initial test structures above, a 102-finger interdigitated capacitor has been fabricated to demonstrate the scalability of the proposed process to large capacitance. This structure is embedded in epoxy resin (a photopatternable epoxy, SU-8; Microchem Inc.) for passivation and characterized at low and high frequencies.

Since the thick conductor process uses a self-alignment technique, fabrication of multiple interdigitated structures does not increase process complexity since no fine alignment is required. The gap capacitor is a coplanar waveguide type having 51-finger electrodes in each side with a finger length of 110 μm, a finger width of 18.5 μm, a gap between fingers of 1.5 μm, a gap between fingers and pads of 10 μm and an electrode thickness of 2 μm. Figure 12 shows a SEM picture of the capacitor prior to embedding in SU-8. The overall dimension of the capacitor is 1318 μm $\times$ 550 μm.

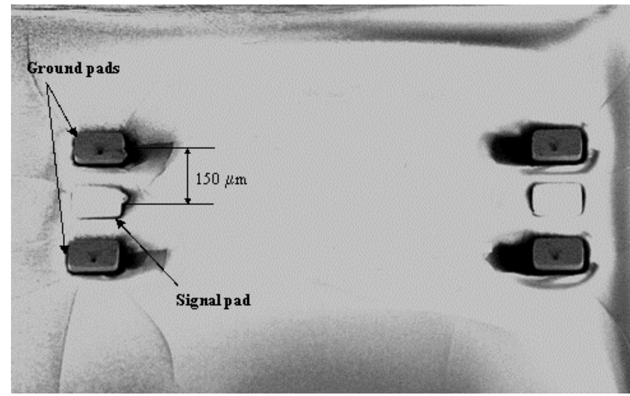


Figure 14. SEM image of an embedded capacitor in SU-8 with only probe pads visible.

Device passivation and the fabrication process for probe pads of the embedded ferroelectric tunable capacitors are shown in figure 13 [42]. First, the previously fabricated gap capacitor is spin coated with SU-8 as thick as 25 μm for passivation. Via holes are photo patterned through the embedded SU-8 (figure 13(*a*)). After seed layers of Ti/Cu (30 nm/300 nm) are conformally coated using dc sputtering, a negative-tone photoresist (NR9-8000, Futurrex, Inc.) is spin coated and photo patterned to form via and probe pad molds (figure 13(*b*)). Conductor layers of Cu/Au (5 μm/300 nm) are electrodeposited through the molds (figure 13(*c*)). Top photoresist and seed layers are removed sequentially to complete the process (figure 13(*d*)). A SEM image of the fabricated embedded capacitor is shown in figure 14, where only probe pads (signal pads and ground pads) are visible over the passivation layer.

Capacitance, tunability and Q-factor as a function of bias voltage are shown in figures 15(*a*)–(*c*), respectively. Before

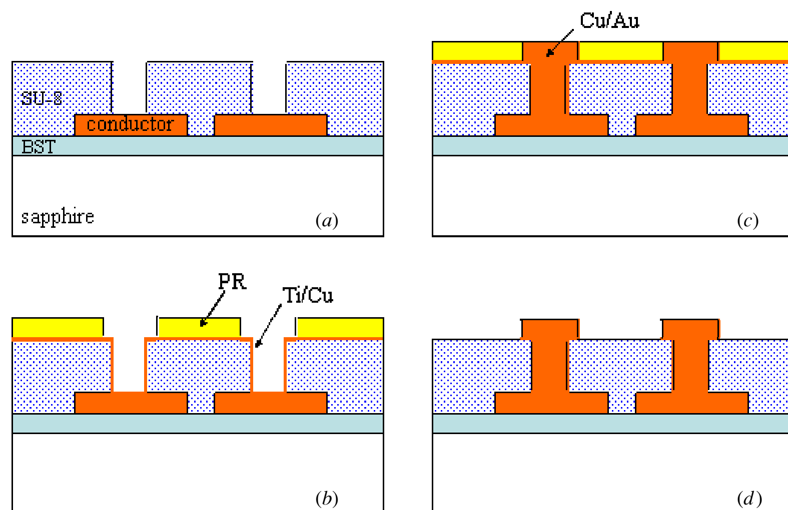


Figure 13. The fabrication process of passivation and probe pads for an embedded ferroelectric gap capacitor.

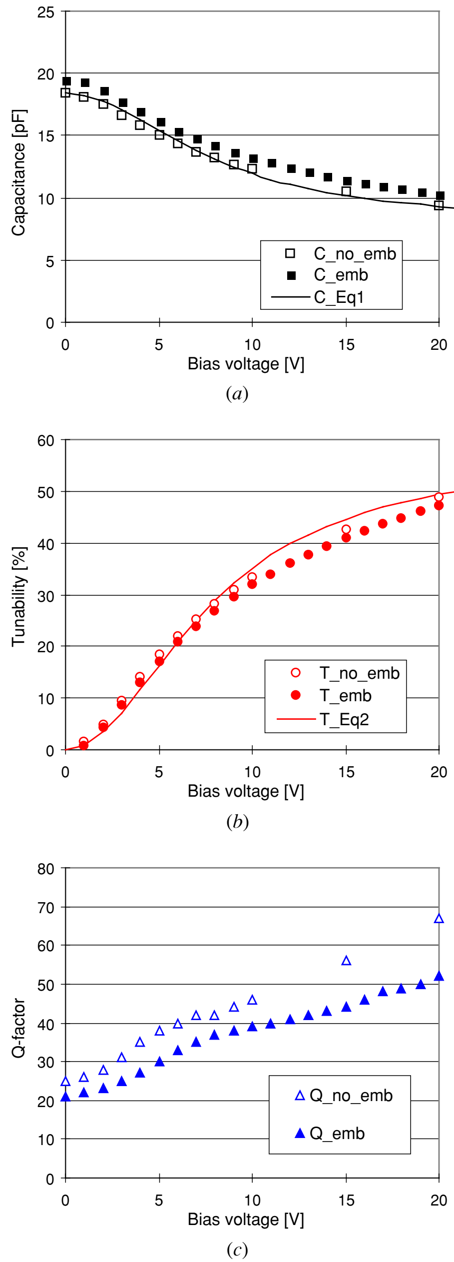


Figure 15. Characterization of a 102-finger interdigitated capacitor at 100 kHz: (*a*) capacitance, (*b*) tunability and (*c*) *Q*-factor as a function of bias voltage.

passivation, the capacitor shows a capacitance of 17.8 pF at zero bias, a tunability of 33% at 10 V bias and a quality factor of 46 at 10 V bias. Capacitance as a function of bias voltage has been expressed using equation (1) with the coefficients summarized in table 3. The solid lines in figures 15(*a*) and (*b*) show the simulated curves from equations (1) and (2). The capacitance between fingers with a gap g of 1.5 μm and a finger width w of 18.5 μm and the capacitance between the finger and the end pad with a larger gap of 10 μm and a width w of 100 μm have been calculated using equations (3)–(6) as well. In the case of the 102-finger interdigitated capacitor, the coupling length for a gap of 1.5 μm is approximately 10 mm (100 μm $\times$ 100), producing a capacitance of 16.27 pF, and the coupling length for a gap of 10 μm is

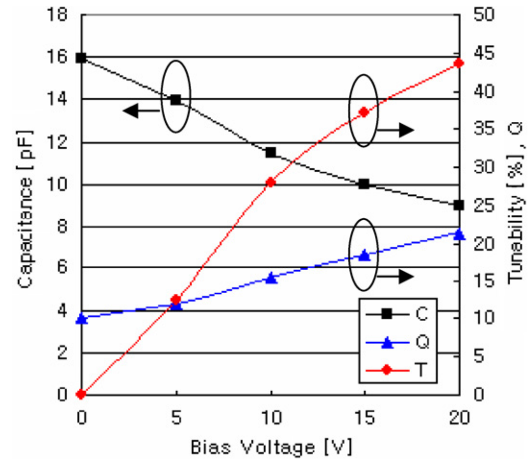


Figure 16. Capacitance, tunability and *Q*-factor as a function of bias voltage for a 102-interdigited capacitor at 1 GHz.

Table 3. Coefficients for capacitance and tunability of the 102-finger interdigitated capacitor.

	C_{nt} (pF)	C_0 (pF)	k (V^{-2})
Capacitor in figure 12	7.9	18.4	0.016

approximately 1.9 mm (18.5 μm $\times$ 102), producing 0.86 pF. The total calculated capacitance is the sum of the two capacitances, being approximately 17.13 pF, which slightly underestimates the measured value of 18.4 pF at zero bias from figure 15(*a*). This may be attributable to underestimated parasitic capacitance in the finger edges. Also, non-simplified models [38, 40] for interdigital capacitors are expected to provide better estimation.

The structure is embedded in a 25 μm thick SU-8 epoxy layer for passivation with probe pads extended to the top surface. After embedding, a slight degradation in *Q*-factor and tunability is observed, primarily attributed to additional dielectric loss of the non-tunable SU-8 material replacing the (lower dielectric constant) air between the electrodes. The overall capacitance is slightly increased due to the additional dielectric contribution from the SU-8. The capacitor demonstrates a capacitance of 18.9 pF, a tunability of 32% at 10 V and a quality factor of 39 (at 10 V bias) as shown in figure 15. In the range of 0–20 V bias voltage, a quality factor decrease of 15–25%, tunability decrease of 2–3% and capacitance increase of 6% are observed after passivation as shown in figure 15. Measurements in figure 15 have been performed at a frequency of 100 kHz.

The embedded capacitor has been characterized at 1 GHz from *S*-parameter measurement and its extraction as described in the previous section. The measurement shows 15.9 pF of capacitance, 28.1% of tunability at 10 V and a quality factor of 16 (at 10 V bias) as shown in figure 16.

Although polymer passivation adds additional loss and tunability reduction, it will enhance device reliability and provide convenience for further chip treatment and handling such as flip–chip bonding or chip-scale packaging. In addition, the passivation layer can serve as a mechanical support for further multilayer fabrication processes without increasing device footprint. For example, an inductor can be fabricated

directly on top of the passivation layer to form a compact tunable filter or a tunable resonator.

5. Conclusions

A thick low-loss microelectrode fabrication process using reverse-side exposure through the transparent BST/sapphire substrate combined with the lift-off process has been demonstrated for a tunable ferroelectric interdigitated gap capacitor application. A single-finger test capacitor with an electrode gap of 1.2 μm and an electrode thickness of 2.2 μm has been fabricated using this process. The fabricated capacitor has been tested and characterized at both low frequency and high frequency. A tunability of 33% at 10 V and 54% at 30 V has been achieved at 100 kHz.

Capacitance as a function of both voltage and gap has been characterized with interdigited gap capacitors. A simplified model for voltage dependent capacitance is utilized. Coefficients are empirically determined using measured data. Q-factors for two capacitors with different electrode thicknesses (0.1 μm and 2.2 μm) have been extracted from S-parameter measurement between 100 MHz and 6 GHz. The Q-factors at 2.4 GHz are 13.45 and 19.83 for the 0.1 μm thick device and 2.2 μm thick device, respectively. The capacitor with thick electrodes fabricated from the proposed fabrication process shows Q-factor improvement by means of effective RF conductor loss reduction.

A 102-finger interdigitated capacitor has been fabricated, embedded in SU-8 epoxy for passivation, and characterized. These multi-finger devices demonstrate that the reverse-side exposure approach to electrode fabrication shows good scalability. After embedding, a slight degradation in properties is observed due to the embedding material. The embedded structure has been characterized at 100 kHz and at 1 GHz. A Q-factor decrease of 15–25%, tunability decrease of 2–3% and capacitance increase of 6% are observed after passivation at 100 kHz. High-frequency properties of the capacitor have been measured to be 15.9 pF of capacitance, 28.1% of tunability at 10 V and a quality factor of 16 (at a 10 V dc bias) at 1 GHz.

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References

[1] Muralt P 2000 Ferroelectric thin films for micro-sensors and actuators: a review *J. Micromech. Microeng.* **10** 136–46

[2] Udayakumar K R, Bart S F, Flynn A M, Chen J, Tavrow L S, Cross L E, Brooks R A and Ehrlich D J 1991 Ferroelectric thin film ultrasonic micromotors Presented at *IEEE Microelectromechanical Systems (Nara)* pp 109–13

[3] Willing B, Kohli M, Muralt P, Setter N and Oehler O 1998 Gas spectrometry based on pyroelectric thin-film arrays integrated on silicon *Sensors Actuators* A **66** 109–13

[4] Dong L, Yue R and Liu L 2004 Monolithic dielectric BST infrared sensor arrays using a novel silicon-ferroelectric integration scheme based on improved porous silicon micromachining *IEEE Microelectromechanical Systems (Maastricht)* pp 576–9

[5] Liu Y, Taylor T R, Speck J S and York R A 2002 High-isolation BST-MEMS switches Presented at *IEEE Int. Microwave Symp. (Seattle, WA)* **1** pp 227–30

[6] Tagantsev A K, Sherman V O, Astafiev K F, Venkatesh J and Setter N 2003 Ferroelectric materials for microwave tunable applications *J. Electroceram.* **11** 5–66

[7] Kingon A I, Maria J P and Streiffer S K 2000 Alternative dielectrics to silicon dioxide for memory and logic devices *Nature* **406** 1032–8

[8] Scott J F 1998 High-dielectric constant thin films for dynamic random access memories (DRAM) *Annu. Rev. Mater. Sci.* **28** 79–100

[9] Koutsaroff I P, Bernacki T, Zelner M, Cervin-Lawry A, Kassam A, Woo P, Woodward L and Patel A 2004 Microwave properties of parallel plate capacitors based on (Ba,Sr)TiO_3 thin films grown on SiO_2/Al_2O_3 substrates *Material Research Society Symp.* **784** pp 319–25

[10] Watt M M, Woo P, Rywak T, McNeil L, Kassam A, Joshi V, Cuchiaro J D and Melnick B M 1998 Feasibility demonstration of a multi-level thin film BST capacitor technology *IEEE Int. Symp. Applications Ferroelectrics* pp 11–14

[11] Sarjeant W J, Clelland I W and Price R A 2001 Capacitive components for power electronics *Proc. IEEE* **89** 846–55

[12] Isom R, Hawkins M, Richins J, McEwan S, Iskabder M and Grow R 2000 Comparative evaluation of MEMS and ferroelectric technology in phase shifter design *IEEE Int. Symp. Antennas Propagation Society* vol 2 pp 808–11

[13] York R, Nagra A, Erker E, Taylor T, Periaswamy P, Speck J, Streiffer S and Auciello O 2001 Microwave integrated circuits using thin-film BST *IEEE Int. Symp. Applications Ferroelectrics* vol 1 pp 195–200

[14] Romanofsky R R, Bernhard J T, Van Keuls F W, Miranda F A, Washington G and Canedy C 2000 K-band phased array antennas based on $Ba_{0.6}Sr_{0.4}TiO_3$ thin-film phase shifters *IEEE Trans. Microw. Theory Tech.* **48** 2504–10

[15] Kim D, Choi Y, Allen M G, Kenney J S and Kiesling D 2002 A wide-band reflection-type phase shifter at S-band using BST coated substrate *IEEE Trans. Microw. Theory Tech.* **50** 2903–9

[16] Yoon Y-K, Kim D, Allen M G, Kenney J S and Hunt A T 2003 A reduced intermodulation distortion tunable ferroelectric capacitor-architecture and demonstration *IEEE Trans. Microw. Theory Tech.* **51** 2568–76

[17] Kim D, Choi Y, Ahn M, Allen M G, Kenney J S and Marry P 2003 2.4 GHz continuously variable ferroelectric phase shifters using all-pass networks *IEEE Microw. Wirel. Compon. Lett.* **13** 434–6

[18] Je S, Kim D S, Kenney J S and Polley T 2003 Effects of annealing and sintering on the structural and electrical properties of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown on sapphire by combustion chemical vapor deposition (CCVD) *Asia-Pacific Microwave Conf. (Seoul)*

[19] Kim D, Je S, Kenney J S and Marry P 2003 Tunable $Ba_{0.6}Sr_{0.4}TiO_3$ interdigital capacitor for microwave applications Presented at *Asia-Pacific Microwave Conf. (Seoul)*

[20] Koutsaroff I P, Woo P, McNeil L, Zelner M, Kassam A, Capanu M, Chmiel L, McClelland B and Cervin-Lawry A 2002 Dielectric properties of (Ba,Sr)TiO_3 MOD films grown on various substrates *IEEE Int. Symp. Applications Ferroelectrics* pp 247–50

[21] Cho H J, Park J B, Yu S S, Roh J S and Yoon H K 2000 Low temperature MOCVD of BST thin film for high density DRAMs *IEEE Int. Symp. Applications of Ferroelectrics* vol 1 pp 55–8

[22] Oljaca M, Luten H A, Tomov T, Sundell S and Hunt A T 2003 Deposition of $Ba_xSr_{(1-x)}TiO_3$ in atmospheric pressure flame: combustion monitoring and optimisation of thin film properties *Surf. Eng.* **19** 51–7
[23] Wang Z, Liu J, Ren T, Liu L and Li Z 2002 $Ba_{0.5}Sr_{0.5}TiO_3$ ferroelectric thick films with uniform thickness and its applications to RF MEMS devices *IEEE Int. Symp. Application Ferroelectrics* pp 475–8
[24] Shoup S S, Shanmugham S, Cousins D, Hunt A T, Paranthaman M, Goyal A, Martin P and Froeger D M 1999 Low-cost combustion chemical vapor deposition of epitaxial buffer layers and superconductors *IEEE Trans. Appl. Supercond.* **9** 2426–9
[25] Dimos D 1995 Ferroelectric thin films for photonics: properties and applications *Annu. Rev. Mater. Sci.* **25** 273–93
[26] Yoon Y-K, Allen M G and Hunt A T 2003 Tunable ferroelectric capacitor with low-loss electrodes fabricated using reverse side exposure *IEEE Electronic Components Technology Conference* pp 1534–40
[27] Thomasson D B and Jackson T N 1998 Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer *IEEE Electron Device Lett.* **19** 124–6
[28] Chung D-S *et al* 2002 Carbon nanotube electron emitters with a gated structure using backside exposure processes *Appl. Phys. Lett.* **80** 4045–7
[29] Peterman M C, Muie P, Bloom B M and Fishman H A 2003 Building thick photoresist structures from the bottom up *J. Micromech. Microeng.* **13** 380–2
[30] Yoon Y-K, Park J-H, Cros F and Allen M G 2003 Integrated vertical screen microfilter system using inclined SU-8 structures *IEEE Microelectromech. Syst. (Kyoto)* pp 227–30
[31] Sato H, Kakinuma T, Go J S and Shoji S 2003 A novel fabrication of in-channel 3-D micromesh structure using maskless multi-angle exposure and its microfilter application Presented at *IEEE Microelectromech. Syst. (Kyoto)* pp 223–6
[32] Kim K, Park D S, Lu H M, Che W, Kim K, Lee J-B and Ahn C H 2004 A tapered hollow metallic microneedle array using backside exposure of SU-8 *J. Micromech. Microeng.* **14** 597–603
[33] Yoon Y-K, Park J-H and Allen M G 2005 Multidirectional UV lithography for complex 3-D MEMS structures *J. Microelectromech. Syst.* submitted
[34] Acikel B, Liu Y, Nagra A S, Taylor T R, Hansen P J, Speck J S and York R A 2001 Phase shifters using $(Ba,Sr)TiO_3$ thin films on sapphire and glass substrates *IEEE Int. Microwave Symp.* vol 2 pp 1191–4
[35] Tombak A, Ayguavives F T, Maria J P, Stauf G T, Kingon A I and Mortazawi A 2001 Tunable RF filters using thin film barium strontium titanate based capacitors *IEEE Int. Microwave Symp.* vol 3 pp 1453–6
[36] Vendik O G 1976 Dielectric nonlinearity of the displacive ferroelectrics at UHF *Ferroelectrics* **12** 85–90
[37] Jona F and Shirane G 1962 *Ferroelectric Crystals* (New York: Pergamon)
[38] Gevorgian S S, Martinsson T, Linner P L J and Kollberg E L 1996 CAD models for multilayered substrate interdigital capacitors *IEEE Trans. Microw. Theory Tech.* **44** 896–904
[39] Vendik O G, Zubko S and Mikolski M 1999 Modeling and calculation of the capacitance of a planar capacitor containing a ferroelectric thin film *Tech. Phys.* **44** 349–55
[40] Carlsson E and Gevorgian S S 1999 Conformal mapping of the field and charge distribution in multilayered substrate CPW's *IEEE Trans. Microw. Theory Tech.* **47** 1544–52
[41] Vandamme E, Schreurs D and van Dinther C 2001 Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test structures *IEEE Trans. Electron Devices* **48** 737–42
[42] Yoon Y-K and Allen M G 2005 Embedded conductor technology for micromachined RF elements *J. Micromech. Microeng.* **15** 1317–26