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Embedded conductor technology for micromachined RF elements

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Abstract

A surface-micromachined, multilayer, embedded conductor fabrication process is presented. The process is based on high-aspect-ratio MEMS via formation and subsequent conformal/plate-through-mold metallization. Using this process, the fabrication of epoxy-embedded, high-Q electroplated RF inductors is demonstrated. This process has two attractive features. First, the embedded nature of these interconnects and inductors allows conventional handling and packaging of inductor/interconnect/chip systems without additional mechanical consideration for the inductor structure and without its significant electrical degradation after further packaging. Second, since the embedding material forms a permanent structural feature of the device, embedding materials that would otherwise be difficult to remove during the fabrication process are instead very appropriate for this technology. The epoxy-based implementation of this technology is low temperature and compatible with post-processing on CMOS foundry-fabricated chips or wafers. Multiple solenoid-type inductors with varying numbers of turns and core-widths are fabricated on a silicon substrate using this technology. A six-turn solenoid type inductor shows an inductance of 2.6 nH and a peak Q-factor of 20.5 at 4.5 GHz.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Many radio frequency (RF) systems, e.g. cellular phones, pagers, GPS receivers and Bluetooth transceivers, demand the integration of passive components with CMOS circuitry for compact, high performance and cost-effective system implementation. It has been demonstrated that RF inductors can be fabricated in a CMOS-compatible fashion [1–3]. An important issue for integrated RF inductors on silicon is minimization of parasitic effects, e.g., coupling capacitance between the inductors and the substrate, and losses caused by induced eddy currents in the substrate. In order to reduce substrate coupling effects, there has been much effort in substrate variation or structure modification, which includes bulk etching the silicon substrate underneath the inductors [3, 4]; placing a patterned ground shield between the inductors and the substrate [5]; using a high-resistivity silicon substrate or silicon-on-sapphire [6, 7]; or out-of-plane coil approaches [8–10]. Alternatively, the substrate coupling can be reduced by placing a large dielectric gap between the inductors and the substrate. A surface micromachined solenoid-type inductor with an air gap between the coil and the substrate has been reported in [11], and spiral-type inductors with an air gap between inductor and substrate have been reported in [12, 13]. While these inductors show good RF performance on a variety of substrates, the resultant structures suspended over the wafer or in the etched wafer may be too delicate to withstand conventional injection-molding-based or other chip packaging approaches. To increase mechanical stability and packaging compatibility of those inductors, embedding of surface micromachined RF devices during the fabrication process can be performed [14, 15]. A large gap between the inductors and the substrate requires a thick via or interconnect layer, where a vertical interconnect through the thick dielectric layer becomes a challenging issue.

In this paper, a surface micromachined epoxy-embedded conductor fabrication process for high-aspect-ratio vertical interconnect and lateral conductors is presented. The

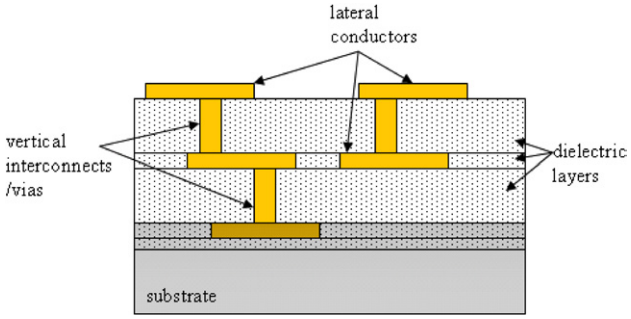


Figure 1. Multi-layer interconnects.

embedded vertical interconnect process uses a high-aspect-ratio via mold formation from photosensitive SU-8 epoxy and subsequent conformal/plate-through-mold metallization, ultimately retaining the SU-8 mold as a part of the substrate for both subsequent processing steps and ultimate packaging. As part of this process description, via fabrication techniques currently used for both back-end IC processes as well as other MEMS processes are described and compared as well. To illustrate the process, surface micromachined epoxy-embedded high-Q inductors are fabricated. The inductors combine the desirable features of: (1) being supported by both electroplated posts and a deposited thick dielectric layer, thereby separating them from the lossy silicon substrate; and (2) being embedded in the epoxy molds from which they are formed, minimizing microphonics and allowing sufficient mechanical stability such that the chips bearing the inductors can be packaged using standard injection-molding processes. An additional processing benefit from the embedded structure is that the epoxy mold used to form the inductors need not be removed in a lengthy etch step.

2. Surface micromachined epoxy-embedded conductors

Both active and passive integrated electrical elements are increasing in three-dimensional complexity to meet the requirements of highly compact, high-performance systems. For passive elements, devices are typically made of three-dimensional multilayers. Each layer consists mainly of conductors and dielectrics, where the metallic conductors are categorized as either a lateral conductor or a vertical interconnect (via) as shown in figure 1. The aspect ratio (height to width ratio) of the metallic via is continually increasing for two reasons: the isolating dielectric layers are increasing in thickness in order to reduce capacitive coupling or other parasitics; while the via widths are becoming narrower in order to increase integration density.

In the MEMS area, high-aspect-ratio via fabrication techniques using UV lithography and plate-through-mold technologies were applied to various electromechanical parts, such as gears [16], magnets [17] and RF inductors [11–13]. In the plate-through-mold approach, the plating time is lengthened proportionally to the depth of the mold to fill. In addition, the mold is required to be removed after the plating, which prolongs the process time further. Moreover, removal of some polymeric molds such as polyimide or SU-8 often relies on expensive dry etching processes such as reactive ion etching (RIE) etc, which is unfavorable for a cost-effective manufacturing process, especially as the mold becomes thicker.

Recently, IBM introduced the damascene process for multi-layer interconnects using copper electroforming through an oxide mold [18]. Conformal copper electrodeposition into a nonplanar surface/trench was performed, leaving an excess of grown copper over the entire surface. This excess copper was removed by a chemical mechanical polishing (CMP) process, leaving electrodeposited copper only in the trench. The oxide layers bounding the copper were intended to remain at the end of the process. These remaining oxide layers serve as a supporting layer for the subsequent processes and provide mechanical stability to withstand later harsh packaging processes such as an injection-molding process.

In some micromachining applications, keeping the mold as a part of a device or a system is advantageous for the process as in the case of vias in IC chips discussed above. For example, Keller *et al* reported the HEXSIL process where molded polysilicon and molded metal in polysilicon were implemented using deeply etched silicon molds and conformal plating to make micro tweezers or other actuators [19, 20]. They used lapping and polishing processes to get rid of excess portion of metal or poly silicon. Cros *et al* reported a molded metal process in SU-8 for magnetic-cored spiral coils [21], where the polymer mold was intended to remain after the process as a part of the device. They used a conformal plating process followed by a wet etching step instead of a polishing step to remove the excess metal portion. The wet etching makes a large recess in the metal portion when the via opening size is large relative to the height. For a successful via process, an aspect ratio (of height to opening) greater than 5 was recommended [21]. This effect was intentionally exploited to allow for the deposition of differing materials into different aspect ratio molds.

In contrast to these approaches, an alternative fabrication process for an embedded conductor in polymer is proposed, which is especially suitable for MEMS interconnect or RF passive component fabrication. This embedded conductor fabrication uses mold formation and a combination of two simultaneous plating processes: a conformal plating process through non-removable lower via mold and a conventional plate-through-mold process through a removable upper conductor mold. The via conductors are embedded in the mold from which they are formed and the mold is not removed after structures are completed. This eliminates a long etching step for the mold removal, which simplifies the process. Also, the electroplating to fill the via mold is carried out by conformal plating, the process duration of which does not increase with increasing via height. Finally, because the conductors are embedded in the mold, the resultant embedded conductor is mechanically strong and robust. This reduces microphonics as well as enables devices fabricated using this technique to survive subsequent electronic packaging processes (such as injection molding or other chip packaging treatments). It should also be noted that the fabrication is carried out at temperatures as low as 100 °C, which makes it compatible with post-processing on top of foundry-fabricated CMOS circuitry.

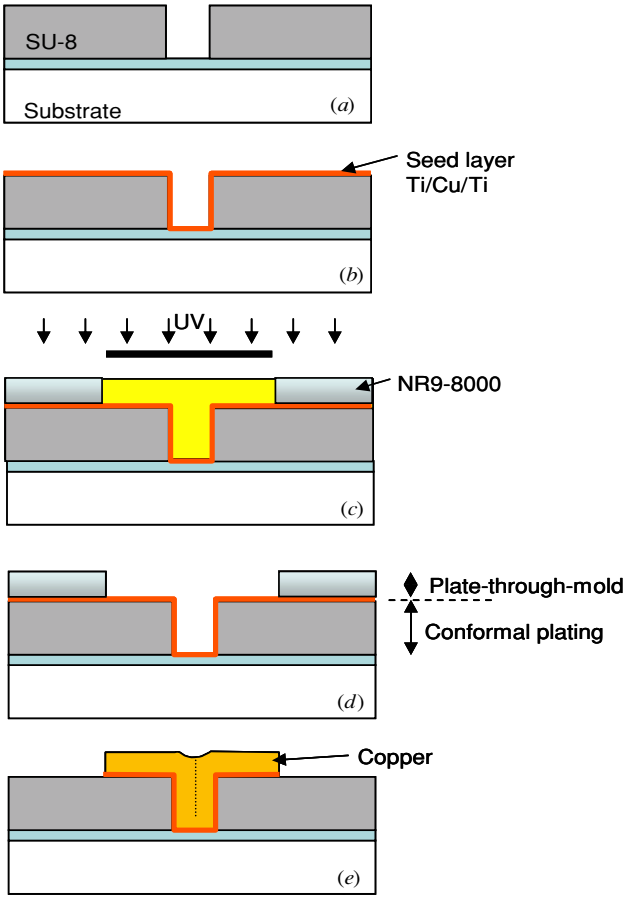


Figure 2. Fabrication process for epoxy-embedded conductors.

3. Embedded conductor technology

The typical fabrication process uses negative tone photosensitive epoxy (SU-8, Microchem, Inc.) as the non-removable polymer mold, negative photoresist (NR9–8000, Futurrex, Inc.) as the removable polymer mold, and copper (Cu) for electroplating. Figure 2 details the fabrication process. An SU-8 epoxy layer (ranging from a few μm to a few hundred μm depending on the application) is spin-coated, baked and patterned for via definition on the substrate (figure 2(a)). The sample is treated with oxygen plasma to enhance adhesion of the subsequently-deposited seed layer. After the seed layer (Ti/Cu/Ti, 20 nm/200 nm/20 nm) is deposited using a dc-sputterer, a thick (20 μm) negative photoresist NR9–8000 is spin coated and baked (figure 2(b)). This thick photoresist layer may trap air in the via areas. This trapped air can expand during the baking step, making subsequent photolithography difficult; this can be avoided by baking at lower temperatures for longer times, e.g., 50 °C for 5 h. Alternatively, a dry film photoresist can be used (e.g., DuPont Riston dry film), by which upper mold patterning can be achieved even with air trapped in the underlying via holes. The mask for defining the upper electrode and the via area is aligned and exposed using UV (figure 2(c)). Note that the use of negative photoresist allows application of a uniform optical dose for the exposed regions of the removable photoresist, since the 'extra' thickness of the material that has accumulated in the vias is not UV-exposed in this process. After developing the photoresist, a double-layer mold is formed (figure 2(d)). A single electrodeposition will fill the double-layer mold simultaneously: a conformal plating process for the via mold and a conventional plate-through-mold process for the upper electrode pattern. Depending on the required aspect ratio, degassing from the via hole prior to electroplating may be useful and can be achieved by a vacuum system. Additional details regarding vacuum plating for deep trenches can be found in [22]. Non-uniform growth along with the via wall can occur due to non-uniform electric field or limited convective flow of plating solution within the deep via. Plating in a weak current density condition associated with low electric field will reduce the non-uniform growth. The current density used is approximately 5 mA cm^{-2} at the deposition rate of 5 to 6 μm hr^{-1}. The copper bath composition is given in [23]. With this condition, via aspect ratios up to 3:1 have been achieved. Various additives or surfactants can be used to obtain conformal plating along with higher aspect ratio vias or trenches (>3:1) [24]. After plating, the top photoresist (NR9-8000) is dissolved in acetone or PR remover (RR4, Futurrex, Inc.). The seed layer (Ti/Cu/Ti) is time-etched using a diluted hydrofluoric acid (5%) for titanium etching and a sulfuric-acid-based copper etchant (H_2SO_4:H_2O_2:DI water =1:1:10) for copper etching to complete the process (figure 2(e)). The SU-8 mold surrounding the via as well as the electroplated Cu structure remain. Note that both the via post and the SU-8 mold will strengthen mechanical stability for the upper structures, serving as a platform for the next layer processes.

Fabrication processes for various via schemes are sketched and compared in figure 3 in the case of one via and one upper conducting layer configuration. The characteristics of each process are summarized in table 1.

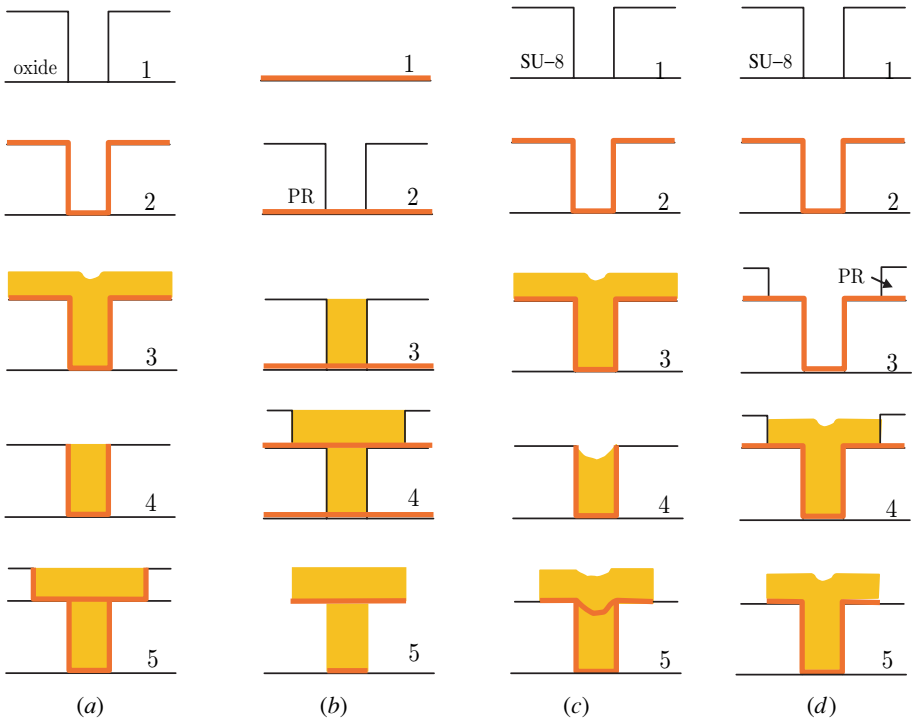
Figure 4 shows a fabricated three-layer embedded structure. The first lower conductor and the second via conductor are embedded in SU-8 while the third upper conductor is not embedded. The vias show concave patterns, which appear after the conformal plating when the via hole is relatively wider than the plating thickness. Those concave via conductors should not exhibit poorer RF performance than their solid-via counterparts as long as the plated metal is thicker than several skin depths in the frequency range of interest, since current is confined to the outermost surface due to the skin effect in the RF frequency range. Using this approach, a variety of multilayer embedded RF components can be implemented, such as inductors, capacitors and waveguides.

The embedding material used here was SU-8, but this approach is not restricted to SU-8. Various polymers (whether photodefinable or not) such as other epoxies, polyimide, polymethylmethacrylate (PMMA), polydimethylsiloxane (PDMS), benzocyclobutene (BCB), polyurethane (PU), liquid crystalline polymer (LCP) and others can be used for the molding material. Non-photodefinable polymer can be patterned by way of dry etching.

The thickness of the polymer layer can be in the range of several μm to several hundred μm. Note that the deposition time using conformal metal deposition is independent of the via layer thickness. This process is low temperature and compatible with an underlying CMOS process.

Table 1. Various processes for via conductor fabrication.

	Damascene [18]	Conventional plate-through-mold process [11]	Conformal plating process with etch-back [21]	Conformal plating process without etch-back (this work)
Mold material	Oxide (ceramic)	Polymer (organic)	Polymer (organic)	Polymer (organic)
Mold removal	No	Yes	No	No
Metal deposition time	Short	Long	Short	Short
Number of plating per two layers	2	2	2	1
Excess metal removal	Polishing (CMP)	No	Chemical etching	No
Mold erosion or metal dishing	Susceptible during CMP	N/A	Metal dishing during etch-back	N/A
Metal source usage	Non economical	Economical	Non economical	Economical
Device packaging	Injection molding	Polymer or cavity packaging	Injection molding	Injection molding
Applications	IC interconnect	actuators, RF passives, MEMS interconnect, Power devices	RF passives, MEMS interconnect, Power devices	RF passives, MEMS interconnect, Power devices



(*a*)	(*b*)	(*c*)	(*d*)
1. Oxide via mold *2. Conformal seed layer* *3. Conformal electroplating* *4. Polishing* *5. Repeat 1–4*	*1. Seed layer* *2. PR via mold* *3. Plate-through-mold* *4. Repeat 1–3* *5. Remove PR and seed layer*	*1. SU-8 mold* *2. Conformal seed layer* *3. Conformal electroplating* *4. Wet etching* *5. Follow (b)3–5*	*1. SU-8 mold* *2. Conformal seed layer* *3. PR patterning for upper layer* *4. Conformal+plate through mold* *5. Remove PR and seed layer*

Figure 3. Fabrication process comparison for one via and one upper conducting layer configuration: (*a*) damascene process; (*b*) conventional plate-through-mold process; (*c*) conformal plating process with etch-back; (*d*) conformal plating without etch-back.

4. Embedded inductors

Schematics and cross-sectional views of solenoid-type, toroid-type, spiral-type and meander-type inductors compatible with embedded conductor technology are shown in figure 5. Among these configurations, a solenoid-type inductor is developed because the magnetic flux produced by the inductor is parallel to the substrate, thereby reducing substrate interaction.

The schematic of an embedded solenoid inductor is shown in figure 6, where the embedding polymer layer is omitted in figure 6(*a*) for the purpose of structural clarity and is presented in figure 6(*b*). A variety of inductor geometries have

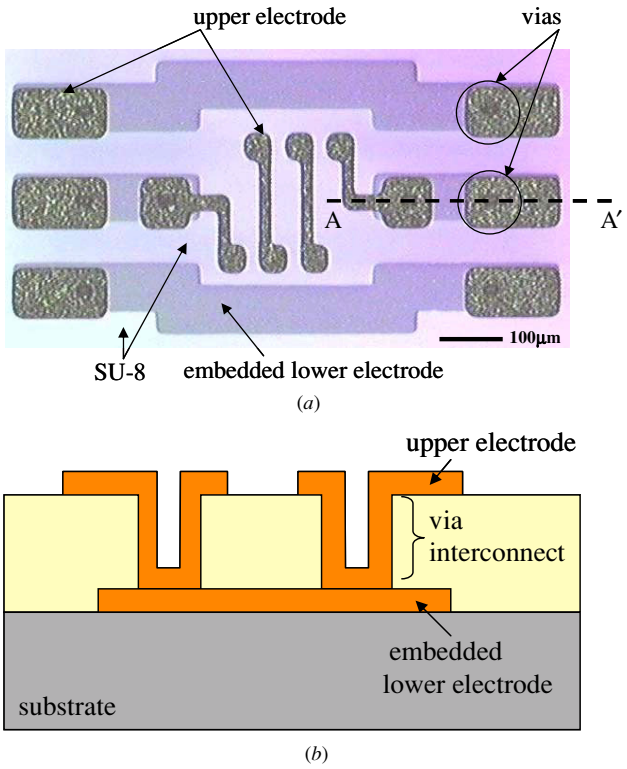


Figure 4. Fabricated three-layer embedded conductors: (*a*) top view; (*b*) schematic of cross-section view (A–A′).

been designed and analyzed using an inductance calculation program, MEMCAD [25]. The main considerations for the design are: (1) to reduce coupling effects between the silicon (Si) substrate and the coil by separating them by a substrate gap g; and (2) to reduce turn-to-turn stray capacitance between the lines by orienting the lines in parallel [11] and by adjusting the spacing between lines s and the layer-to-layer core height h. In the final design, a line spacing s, a core height h and a gap g of 60 μm, 40 μm and 25 μm, respectively, have been used. The thickness t of the metal layers is 10 μm and the line width w of the coil is 20 μm. Since the skin depths of copper at 1 GHz and 10 GHz are approximately 2 μm and 0.66 μm, respectively, the designed w and t are not a limiting factor for high-Q inductors. In addition, inductors with varying numbers of turns and varying solenoid core width w_c have been analyzed. To enable electrical probing of the test inductors, extended pads are designed since the inductor structure itself will be inaccessibly embedded in epoxy.

The inductor fabrication process follows the embedded conductor process discussed in the previous section, and is described in detail in figure 7. A 10 μm thick copper layer for ground and signal lines is patterned using a seed layer deposition and subsequent electrodeposition step, followed by removal of the seed layer using timed etching. An SU-8 epoxy layer (25 μm) is spin coated and patterned for the first via definition (figure 7(*b*)). After seed layers (Ti/Cu/Ti) are deposited using a dc-sputterer, a thick (10 μm) negative photoresist NR9-8000 is spin coated and patterned for the lower metal layer of the coil and the first via hole (figure 7(*c*)). Two metal layers (the first via hole and the coil lower metal layer) are formed simultaneously with a single electroplating step. After the first electroplating, the photoresist mold and seed layers are removed, but the SU-8 mold surrounding the via as well as the electroplated Cu structure remains. Note that both the via post and the SU-8 mold mechanically support the entire solenoid coil thereafter (figure 7(*d*)). Steps (*b*) through (*d*) are repeated for the next via (40 μm thick) and the coil upper metal layer. Note that the core of the embedded inductor is filled with SU-8 (figure 7(*e*)). Since the core of the inductor has already been filled, and is mechanically robust, the inductance and Q-factor of the inductor are not expected to change after a subsequent packaging process, such as plastic injection molding. However, the electrical properties of the epoxy may influence the inductor properties in this configuration.

Figure 8 shows photomicrographs of fabricated test inductors on silicon substrate with resistivity of 5–10 Ω cm. An inductor 'library' consisting of devices with various number of coil turns (3, 6, 9 and 12) and various core width (100 μm, 200 μm, 300 μm and 400 μm) is shown in figure 8(*a*). (Note that the inductors with 400 μm core width are not captured in this figure due to a limited camera span.) A top view and an oblique view of a 6 turn inductor with a core width of 300 μm are shown in figures 8(*b*) and (*c*), respectively. Since epoxy is transparent, the embedded metal part as well as the exposed metal part can be seen. The brighter and the darker metal parts in figure 8(*b*) are exposed metal and embedded metal portions, respectively.

Figures 9(*a*) and (*b*) show SEM views of a fabricated six-turn embedded inductor. In figure 9(*a*), the exposed metal probe pads and upper metal of the coil can be seen while the embedded part cannot because the electron beam does not penetrate through the SU-8 epoxy to give an image. Note that the SEM image has been taken without applying a thin metal coating over the structure in this case and the nonuniform charge distribution results in a discoloration on the SU-8 surface. Figure 9(*b*) shows an SEM view of the device after the embedding epoxy has been etched away for clarity. The solenoid coil is 25 μm above the Si substrate. The coil width w is 20 μm, the turn-to-turn pitch p ($=w+s$) is 80 μm, and the height of the solenoid core h_c ($=h+t$) (i.e., the distance between the center of the lower metal layer of the coil and the center of the upper metal layer of the coil) is 50 μm. The via has a cross section of 25 μm $\times$ 30 μm.

5. Testing and results

S-parameter measurement of the embedded inductors is carried out in the frequency range of 100 MHz to 10 GHz using an HP8510C vector network analyzer with standard air coplanar G–S–G probe tips (150 μm pitch) (Cascade Microtech) after a standard SOLT calibration. Inductance and Q-factor are extracted from the measured S-parameters [26]. Figure 10 shows the measured inductance and Q-factor of an embedded test inductor with six turns and a core width, w_c, of 400 μm. The peak Q-factor and inductance at 4.5 GHz are 20.5 and 2.6 nH, respectively. The measured data have been compared with MEMCAD simulation results for the same geometry. The inductance results of measurement and simulation are consistent up to 6 GHz.

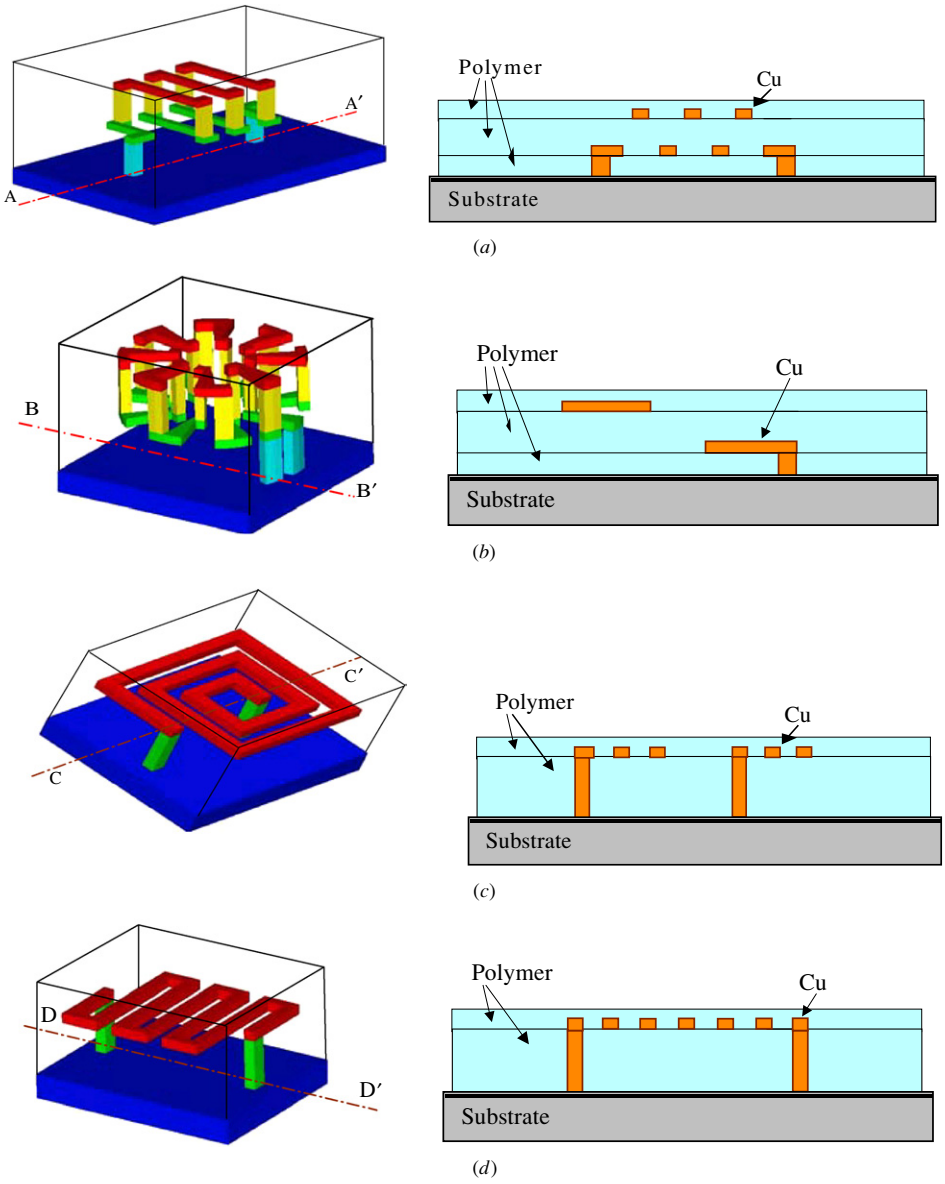


Figure 5. Schematics and cross-section view of various 3-D micromachined embedded inductors: (*a*) solenoid-type inductor; (*b*) toroid-type inductor; (*c*) spiral-type inductor; (*d*) meander-type inductor.

The inductance for an ideal solenoid coil can be expressed in equation (1).

$$L = N^2 \mu_c \frac{w_c h_c}{l_c} \tag{1}$$

where N is the number of turns, μ_c is the core permeability, w_c is the core width, h_c is the core height, and l_c is the core length. The micromachined solenoid-type inductor is not ideal in the sense that the core is not cylindrical in shape, and the wire is not wound closely enough to have the magnetic flux only inside the core. In addition, the geometric constraint of a single coil winding yields a linear relationship between pitch and core length such as $l_c = Np$. As a result, the inductance for the micromachined solenoid-type inductors can be written as

$$L = \kappa N \mu_c \frac{w_c h_c}{p} \tag{2}$$

where κ is a constant of proportionality which is determined experimentally, and the geometric substitution $l_c = Np$, where p is the turn-to-turn pitch, has been made.

Figure 11 shows the measured inductance and Q-factor, and simulated inductance, of six-turn inductors at 4.5 GHz as functions of core width (100 μm, 200 μm, 300 μm and 400 μm). The inductance values calculated from equation (2) are plotted with proportionality constant of 1.35, which gives good agreement with measured data. A similar analysis for number of turns with a core width of 200 μm is shown in figure 12, with a proportionality constant of 1.25. The agreement of the data with simulation as well as the lumped-element equation (2) indicates that the inductors formed from the embedded conductor process are performing as expected. Given an inductor height and a turn-to-turn pitch defined by a fabrication constraint, inductors with large inductance (e.g. 5–10 nH) can be achieved by increasing number of turns or increasing core width as projected by equation (2).

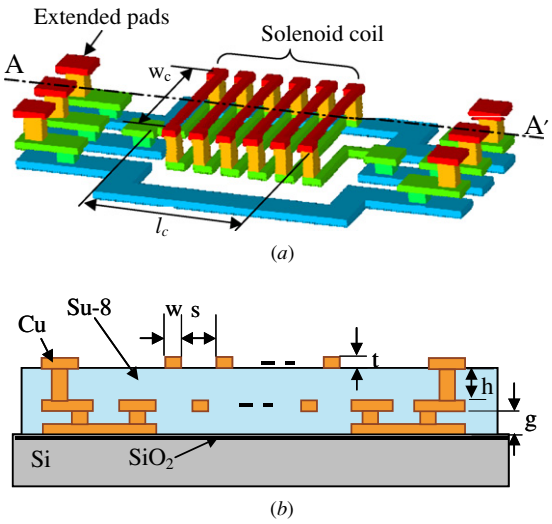


Figure 6. Schematic of solenoid inductor: (*a*) perspective view (SU-8 mold is not illustrated for structural clarity); (*b*) cross-section view of A–A′.

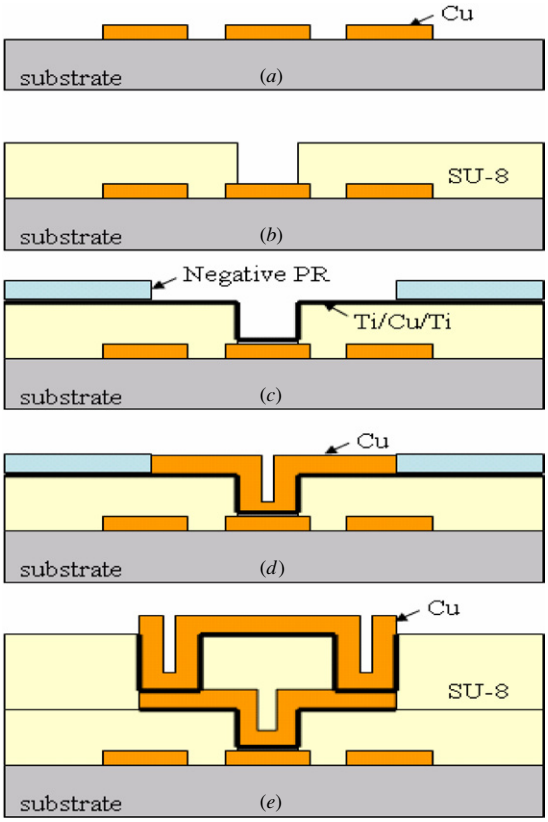


Figure 7. Fabrication process for embedded inductors.

6. Discussion

A simplified lumped element model for an inductor is shown in figure 13, where L represents inductance, R_{esr} equivalent series resistance, and C_p parasitic capacitance. Capacitance between the probe pads and the substrate is not included in this model and C_p is mainly attributed to the stray capacitance between neighboring conductors. R_{esr} includes dc loss and RF loss of conductors, eddy current loss of the conductive substrate, and

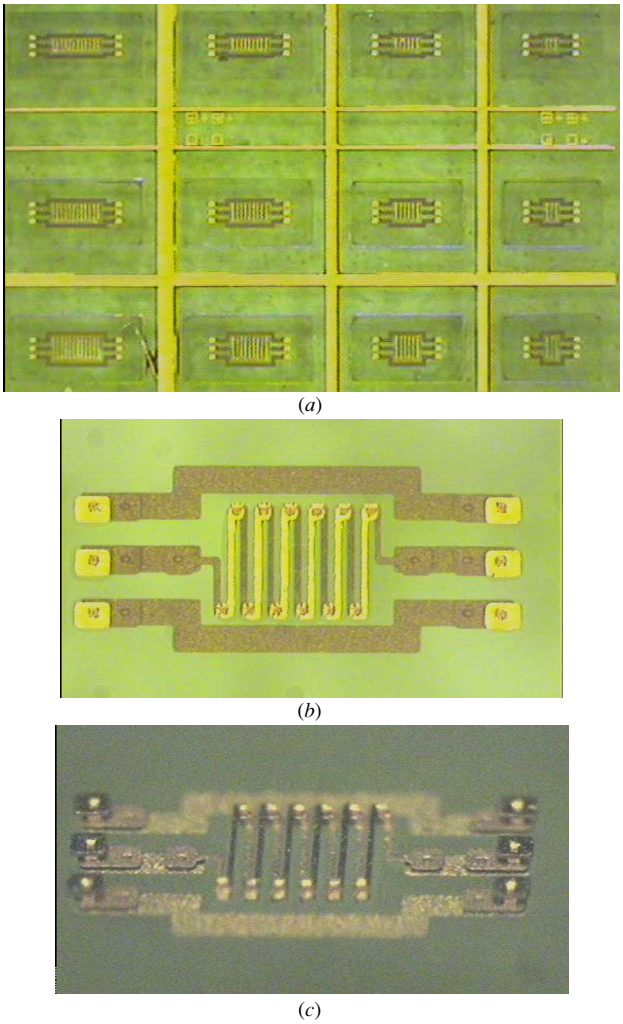


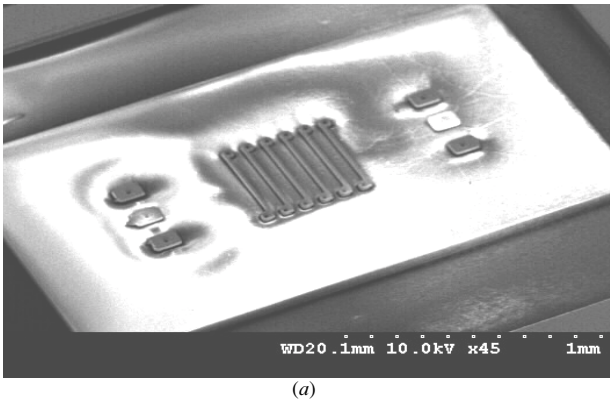
Figure 8. Photomicrograph of fabricated inductors: (*a*) a set of inductor library; (*b*) top view of a six-turn inductor; (*c*) oblique view of a six-turn inductor.

dielectric loss of the polymer between the conductors. The Q-factor for this circuit is given in equation (3) for frequencies up to and including the self-resonance frequency [27]:

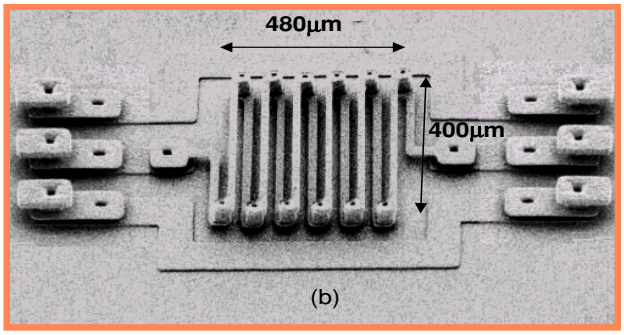
$$Q = Q_0\left[1 - x^2\left(1 + \frac{1}{Q_0^2}\right)\right] \tag{3}$$

where $Q_0 = \omega L/R_{esr}$, $x^2 = \omega^2 LC_p = (f/f_r)^2$, ω is angular operating frequency, and f and f_r are operating frequency and resonant frequency, respectively. When the parasitic capacitance is small, the Q-factor is approximately equal to Q_0, which is the case of a purely inductive-resistive circuit. The presence of the parasitic capacitance causes the Q-factor to be reduced from Q_0 to Q and also self-resonance to occur.

When the inductor is embedded in polymer, the device Q-factor is affected by the presence of polymer surrounding it. First, the parasitic capacitance increases due to the increased dielectric constant of the material (e.g. relative dielectric constant of SU-8 is 3–4 [28]), resulting in a decrease in the overall Q-factor. Second, the additional dielectric loss of the polymer (e.g. loss tangent of SU-8 is greater than 0.08 [29]) will contribute to an increase of R_{esr}, also resulting in decrease of the overall Q-factor. This kind of degradation can



(*a*)



(*b*)

Figure 9. SEM images of the fabricated six-turn embedded inductor: (*a*) embedded; (*b*) after removal of SU-8.

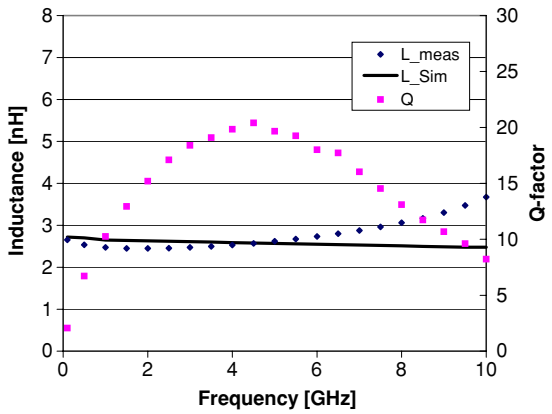


Figure 10. Measured inductance (diamonds) and Q-factor (squares) of the fabricated embedded inductor (six turns and 400 μm core width). The solid line is a simulation of the inductance using MEMCAD.

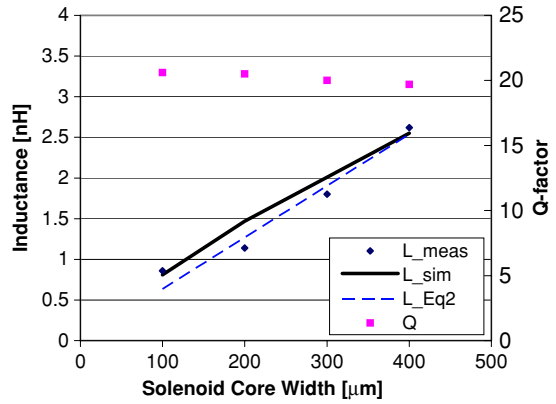


Figure 11. Measured inductance (diamonds) and Q-factor (squares) at 4.5 GHz of six-turn embedded inductors as functions of core width. Simulation (solid line) and equation (2) (dashed line) are shown as well.

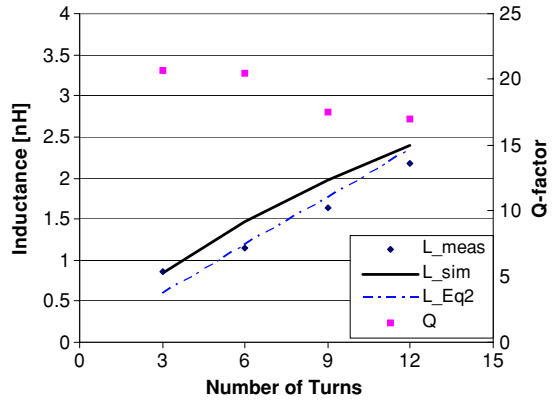


Figure 12. Measured inductance (diamonds) and Q-factor (squares) at 4.5 GHz of 200 μm wide embedded inductors as functions of the number of turns. Simulation (solid line) and equation (2) (dashed line) are shown as well.

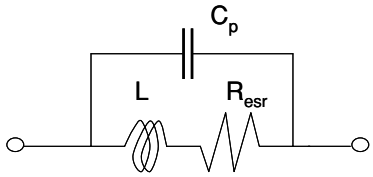


Figure 13. Simplified lumped parameter model for the inductor.

be reduced by using a dielectric material with low dielectric constant and low dielectric loss as a molding material such as BCB ($\varepsilon_r = 2.65$, loss tan $= 0.0008$) [30] or LCP ($\varepsilon_r = 2.9$, loss tan $= 0.002$) [31].

Further increasing the gap between the inductor and the substrate can reduce not only parasitic capacitance between the inductor and the substrate, but also the magnetic flux linkage to the lossy substrate, resulting in improved Q-factor. Also, given fabrication-constrained shapes for cross-sectional core areas, a square cross section of the inductor core is preferred to a wide rectangular-shaped core to achieve a high Q-factor device. The inductor geometry (line width, pitch and height to width ratio etc) could be further optimized. More details regarding the geometry issue can be found in [27].

Table 2 shows a property comparison of spiral and solenoid inductors on a silicon substrate in terms of Q-factor, inductance and the device footprint etc. Solenoid-type inductors in this work consume relatively large area compared to spiral-type inductors. But such solenoid inductors can be placed directly over the circuitry (thus consuming no additional space) while simultaneously minimizing magnetic and parasitic interaction with the underlying circuitry and substrate. An alternative approach that maintains these desirable features would be a spiral inductor with a sufficiently large inductor-to-substrate gap as shown in figure 5(*c*).

Table 2. Spiral and solenoid inductors on a silicon substrate.

	Q-factor	Inductance (nH)	Area	Frequency at Q_{max} (GHz)	SRF (GHz)	(Reference) Primary author
Spiral	3–8	1.9	115 μm × 115 μm	2	9.7	[1] Nguyen
	5.7	3.2	170 μm × 170 μm	>1	>5	[2] Craninckx
	N/A	100	440 μm × 440 μm	N/A	3	[3] Chang
	35	2.7	120 μm × 120 μm	5.5	6.5	[4] Jiang
	6.76	7	300 μm × 300 μm	2	3.6	[5] Yue
	5	∼5	300 μm × 300 μm	>3	>5	[6] Reyes
	3.6	4.0	150 μm × 150 μm	1	9.2	[7] Johnson
	14–18	10–25	500 μm × 500 μm	0.1	>2	[12] Park
Solenoid	30	4.8	450 μm × 500 μm	1	>4	[32] Young
	17	2.7	1600 μm × 80 μm	2.4	>10	[33] Yoon
	20.6	2.6	480 μm × 400 μm	4.5	>10	[14] Yoon and this work

7. Conclusions

A surface micromachined multi-layer embedded conductor fabrication technique has been demonstrated using SU-8 as a permanent mold material, NR9-8000 as a removable mold material, and copper as an electroplating material. Two layers of conductors (a vertical via conductor and a lateral conductor) are formed simultaneously in a single electroplating step, combining conformal plating over an uneven surface with plate-through-mold process for the upper lateral electrode. The process requires fewer electroplating steps and does not require removal of the via mold, thereby contributing both to fabrication cost reduction as well as increased mechanical strength and stability of the structures. This increased stability will allow these surface micromachined devices to withstand subsequent harsh packaging steps. To illustrate the process, embedded solenoid-type inductors are fabricated using a multi-layer embedded conductor fabrication process. They are characterized in the RF range of 100 MHz to 10 GHz, showing high quality RF performance. A six-turn inductor shows Q-factor of 20.5 at 4.5 GHz with 2.6 nH on a normal silicon substrate. This fabrication technique can be applied to 3-D implementation of various passive RF components, radiating structures, and MEMS interconnects.

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