Electroplated Metal Buried Interconnect and Through-Wafer Metal-Filled Via Technology for High-Power Integrated Electronics

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***Abstract*—In this paper, we present the design, fabrication process, and experimental results of an electroplated metal buried interconnect and through-wafer via technology suitable for extremely low resistance interconnection of microelectronic devices. The technology is demonstrated using a 3-D daisy-chain test structure comprised of electroplated through-wafer vias buried in the silicon substrate to form the respective interconnect. In contrast to the conventional daisy-chain structures used in flip chip joining and packaging, the designed structure is fabricated on a single substrate without requiring a subsequent bonding process. The top connectors formed on the front-side of the substrate are connected to bottom connectors buried inside the substrate (buried interconnects) through 61-μm-high, void-free, fully-filled, electroplated vias. The metal electroplated buried interconnects are fabricated at the bottom surface of 232-μm-deep trenches formed on the backside of the substrate. Processes for forming deep trenches with rounded-off edges and photoresist spray coating have been developed to fabricate the buried interconnects and complete the daisy-chain structure. Developed processes enable conformal photoresist deposition inside the deep vertical trenches with excellent step and sidewall coverage, surpassing the limitations of conventional fabrication approaches. Furthermore, electroplating molds were perfectly patterned at the bottom of these deep trenches. Through-wafer vias with controllable height are fabricated by direct bottom-up plating from the buried interconnect without additional preparation, such as wafer bonding or hole filling processes. The interconnection scheme developed in this research considerably reduces the height of narrow vertical vias, compared to conventional through-wafer vias, and enables a high density array of interconnect structures. Moreover, low resistance interconnect suitable for high power applications can be realized with thick electroplated copper and fully-filled vias. Buried interconnect can be also utilized in high voltage transistor applications. Resistance testing has been performed to validate the electrical integrity of the fabricated daisy-chain structure, and the results are compared with simulation and analytical calculations.**

***Index Terms*—Electroplated metal, interconnection, spray coating, through-wafer via.**

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I. Introduction

THROUGH-WAFER interconnect technology, in which metal interconnections extend through a portion of the bulk silicon wafer, has gained noticeable research momentum in the field of integrated circuit (IC) fabrication, packaging, and micro-electro-mechanical systems (MEMS). In addition to the evident efficiency in utilizing the front and backside of the substrate, through-wafer interconnect provides compact packaging and many other advantages resulting from shorter connection distance compared to conventional interconnection technologies. Such characteristics as reduced total resistance, lower parasitics, reduced delay of signal, and low power consumption can be especially beneficial for radio-frequency (RF) and power devices [1]–[4].

Several techniques have been developed to fabricate MEMS-based through-wafer interconnections on silicon or silicon-on-insulator (SOI) substrates. In general, cavities formed by wet anisotropic etching, vertical through-wafer vias formed using the Bosch process [5], or the combination of the two, are used in the fabrication of through-wafer interconnects [1]. The electrical connection from the front-side of the substrate to the backside is typically made by metal or polycrystalline silicon layers formed on the cavity surface or through metal-filled vias. One of the common techniques is to fabricate a separate wafer with through-wafer interconnects and bond the die with circuitry or interconnections on the front and backside of the wafer with interconnects. Typically, as the perforations for the via holes are formed on the substrate, a hole sealing process or separate substrate with seed layer is required to have a void-free fully metal filled through-wafer interconnect [1]. The vertical through-wafer via whose height equals the substrate thickness, can be fabricated with deep silicon etch using the Bosch process and subsequent conductive material deposition inside the via holes, but the aspect ratio of the via is limited by the inherent characteristics of the Bosch process itself. For vertical trenches with a closed bottom surface, a void-free bottom-up fill with electroplated metal can be obtained with the aid of additive control, fountain plating, reverse pulse plating, and dissolved-oxygen enrichment [6], [7].

The novelty of this research is in demonstrating a more efficient interconnection scheme where through-wafer vias are coupled with thick patterned electrical connectors on both the front and backside of the substrate. Fig. 1 illustrates a cross section of the proposed through-wafer interconnection scheme. The via height (h_{via}) can be adjusted by modifying the depth

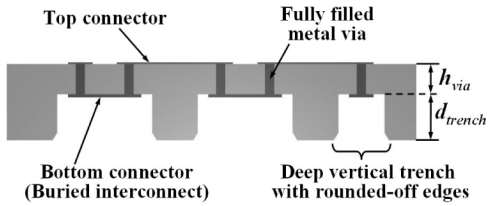


Fig. 1. Schematics of the proposed structure.

of the larger trench (d_{trench}), since the substrate thickness remaining under the deep trench equals the via height. The proposed and fabricated through-wafer vias are desirable both in that they reduce the interconnect length and provide efficient use of substrate real estate. By fabricating the interconnect structure with thick electroplated metal layers, the field of application can be extended to circuitry requiring higher power handling capability. Moreover, the fabrication processes for these structures are readily applicable to chip stacking and packaging applications, such as wafer-level packaging of MEMS devices [8].

Up to the present, controlling the through-wafer via height and simultaneously having patterned metal interconnections at the bottom surface of the via has been challenged mainly by process limitations. Partial thinning of the substrate by wet anisotropic etching has been widely used [1], but the crystallographic axis dependence of the wet etch process has certain drawbacks. While providing angled sidewalls suited for subsequent lithographic processes, cavities formed by wet etching take up larger area at the opening which increases with the cavity depth.

In this research, we propose an interconnect structure comprising top connectors formed on the front-side of the substrate, though-wafer vias formed with fully-filled metal, and buried interconnects as the bottom connectors. The buried interconnect is an array of electroplated metal structures fabricated at the bottom of deep trenches formed on the backside of the substrate. For the fabrication of the buried interconnect structure, a combined etch process for the trench formation and spray coating process have been developed. The trench formation process combines the dry isotropic silicon etch and Bosch process to fabricate a trench with vertical sidewall and angled top-side edges, which enables a high density array of trench formation in contrast to the wet etching process. The angled top-side edges of the trench enable sufficient coverage during the spray coating and lithography process for 300-μm-deep trenches. Details of the combined silicon etch and spray coating process are described in [9]. The through-wafer vias can be fabricated by bottom-up electroplating from the buried interconnect to form a void-free metal filled via. As the via is formed directly on top of the buried interconnect, additional steps for via plating are not required. The height of the through-wafer via can be controlled by changing the depth of the trenches formed on the backside, since the substrate thickness remaining on top of the buried interconnect determines the via height. To illustrate the process, a daisy-chain test structure is proposed. The daisy-chain structure discussed here differs from conventional daisy-chains used in flip-chip joining or packaging in that connectors are formed on the top and bottom surfaces of a single substrate and no bonding process is involved [10], [11].

II. Design

Fig. 2(a) shows the perspective cut plane view of the buried interconnect. For the validation of the daisy-chain scheme, a periodic plated metal structure where the top and bottom metal structures are connected by a plated via has been designed. Fig. 2(b) shows the perspective view of the daisy-chain structure composed of three electroplated copper layers. The top connectors are formed on the front-side of the substrate, and connected to the bottom connectors (buried interconnect) through vias filled with plated copper. Instead of fabricating the bottom connectors at the backside of the substrate, metal connectors are buried inside the deep trenches as shown in Fig. 2(c). The lateral distance between the connectors, and thus the distance between the trenches on the backside, is 300 μm. To fabricate trenches having the same active area and spacing at the bottom with a wet chemical etching process, the trench depth is limited to 212 μm to prevent the overlapping of the nearby cavity opening [9].

An SOI substrate was used to demonstrate process compatibility with SOI substrates having circuitry, such as power electronics, on the device layer. The three layers of the daisy-chain structure are fabricated with electroplated copper for thick metal connectors having minimum resistivity. The via filling process also benefits from electroplating due to higher deposition rate and capability to form a thick void-free metal structure, compared to conventional metallization processes such as sputtering and evaporation. As shown in Fig. 2(d), all the contact area between the plated copper structures and substrate are covered with insulation layers to avoid leakage current through the silicon. The daisy-chain scheme combines the advantages of 3-D and through-wafer interconnections using thick metal lines, resulting in a reduction of footprint for interconnections on the device layer, reduced ohmic loss due to reduced via depth, and an on-chip fabrication process which does not require any wafer bonding and polishing processes. Moreover, heat dissipation through the wafer thickness can be achieved by exploitation of the inherent thermal vias formed through this process.

For a complementary metal–oxide semiconductor (CMOS) compatible backend process, the temperature limit is set to 400 °C, and the actual highest temperature during the process is the plasma enhanced chemical vapor deposition (PECVD) oxide deposition temperature of 250 °C. Table I summarizes the overall dimensions of the designed daisy-chain structure.

III. Fabrication Process

The fabrication process comprises the backside process including the trench formation and electroplating, via etch and filling, and front-side electroplating process. The first stage of the fabrication process is the buried interconnect formation on the backside of the substrate. Buried interconnect not only reduces the through-wafer via height but also enables via filling through a simple bottom-up plating process. For deep vertical

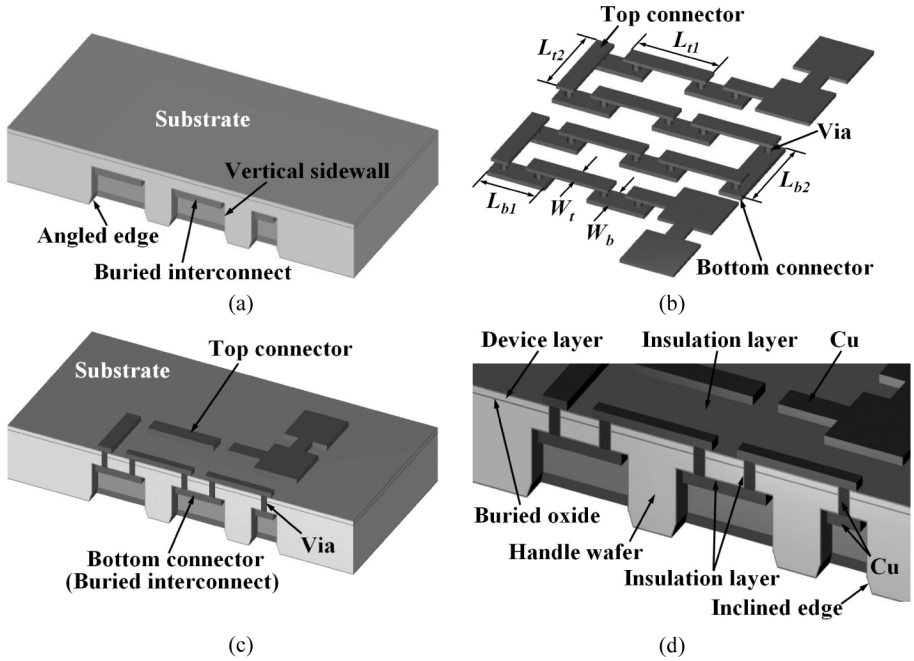


Fig. 2. Designed structure: (a) cut plane view of the buried interconnect on the substrate; (b) perspective view of the daisy-chain without substrate; (c) cut plane view of the daisy-chain on the substrate; (d) close-up view of the cut plane and details of the structure.

trenches fabricated with the Bosch process, it is very challenging to have complete photoresist coverage on the top-side edges and vertical sidewalls even with spray coating process [12], [13]. Although some alternative approaches have shown good results [14], [15], spray coating process is preferable if sufficient coverage of edge and sidewall can be obtained for vertical trenches having hundreds of microns of depth. To address the coverage issues, the conventional Bosch process and an isotropic silicon etch process are combined to form rounded-off top-side trench edges. As a result, the top-side edge and sidewall coverage of the spray coated photoresist is greatly improved. Furthermore, photoresist patterning of plating molds at the bottom surface of the deep trenches is possible. The modified etch process combines the advantages of anisotropic wet etching and silicon deep etching to fabricate a high density array of deep trenches having angled top-side edges and vertical sidewalls. This is realized by initial isotropic dry etch of silicon and subsequent Bosch process, followed by a final blanket isotropic etch process. All etch processes are performed in the same inductively coupled plasma reactive ion etch (ICP RIE) chamber. Compared to conventional wet etch processes, the increase of the trench opening is minimal and is independent of the total trench depth. The depth of angled edges can be controlled by the amount of initial isotropic etch process. Moreover, the slope of the edges can be controlled by modifying the isotropic etch parameters. Fig. 3 shows typical etch results of the combined silicon etch process.

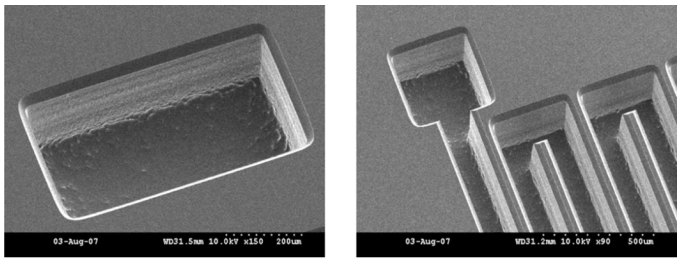
For the formation of plating mold at the bottom of deep trenches, a spray coating process has been used. By optimizing the solids content of the photoresist, baking conditions, and spray pressure together with multiple coatings, the top-side edges and vertical sidewalls were successfully coated. As shown in Fig. 4, conventional trenches fabricated by Bosch process could not be fully covered even with the optimized spray coating conditions. A standard contact aligner (MA/BA-6, Suss MicroTec) was used for the alignment and exposure. As the patterns were generated at the bottom surface of the deep trenches, the mask did not make direct contact with the photoresist regions to be exposed, resulting in a proximity effect.

A. Buried Interconnect Fabrication

The fabrication process of the daisy-chain structure starts with an SOI substrate having device layer, buried oxide, and handle wafer thicknesses of 2.2, 1, and 675 μm, respectively. Initially, the substrate was thinned down to 310 μm by etching the backside of the handle wafer with a 40wt% potassium hydroxide (KOH) solution at 92 °C. After the patterning of backside trenches, the substrate was mounted on a 4-in dummy wafer for the ICP RIE and spray coating processes. For the buried copper interconnect fabrication at the bottom, 232-μm-deep trenches are formed on the backside of the substrate by the combined silicon etch process. Due to the final blanket isotropic etch in the combined etch process, the substrate thickness was reduced to 293 μm, and 61-μm-thick layer of silicon and buried oxide was remaining under the trenches. For electrical isolation between the copper interconnects and silicon substrate, a 500-nm-thick PECVD oxide was deposited on the backside of the substrate [Fig. 5(b)]. Subsequently, a titanium–copper–titanium seed layer having respective thicknesses of 30 nm, 1 μm, and 30 nm is deposited for the copper electroplating process. The bottom titanium layer is used as an adhesion layer for the copper, and the top titanium layer is used to protect the oxidation of copper and to promote the adhesion of the photoresist. A 1-μm-thick copper seed layer was used in order to guarantee a good electrical connection through the vertical sidewalls to the bottom of the deep trenches. The

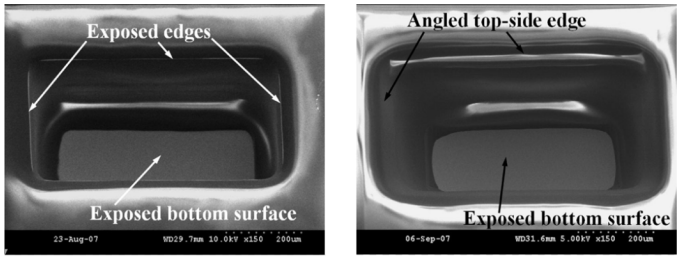
TABLE I
MASK DIMENSIONS OF THE DESIGNED DAISY-CHAIN STRUCTURE [DEFINED IN FIG. 2(B)]

Label	L_{t1}	L_{t2}	W_t	L_{b1}	L_{b2}	W_b	Via diameter
Dimension [μm]	760	760	160	480	760	160	60



(a) (b)

Fig. 3. SEM images of the 300–μm-deep silicon trenches fabricated with combined etch process: (a) rectangular trench; (b) serpentine test pattern.



(a) (b)

Fig. 4. SEM images of the 300-μm-deep trenches covered with patterned photoresist: (a) spray coated photoresist on a conventional trench; (b) spray coated photoresist on a trench with angled top-side edges.

front-side of the substrate (device layer) is also covered with 500-nm-thick PECVD oxide for insulation and passivation. The buried bottom copper structures are then electroplated using the spray coated and patterned photoresist as the mold [Fig. 5(c)]. The plating mold is removed after the plating process, where as the seed layer is preserved for via plating process.

B. Via and Top Connector Fabrication

The via holes are formed on the front-side of the substrate by subsequent etch of oxide and silicon layers down to the seed layer formed on the bottom surface of the trench [Fig. 5(d)]. For the insulation of the via sidewall, a 1-μm-thick PECVD oxide is deposited and etched back using RIE such that only the vertical via hole sidewalls are covered with the oxide. The vias are filled with copper by electroplating process [Fig. 5(e)]. The seed layer deposited on the backside of the substrate is used, and the backside of the substrate is covered with tape during the plating process. Since the vertical sidewall of the via is covered with oxide layer while the seed layer for buried interconnect is exposed at the bottom surface of the via, a void-free copper filled trench can be obtained by simple electroplating with a dc current

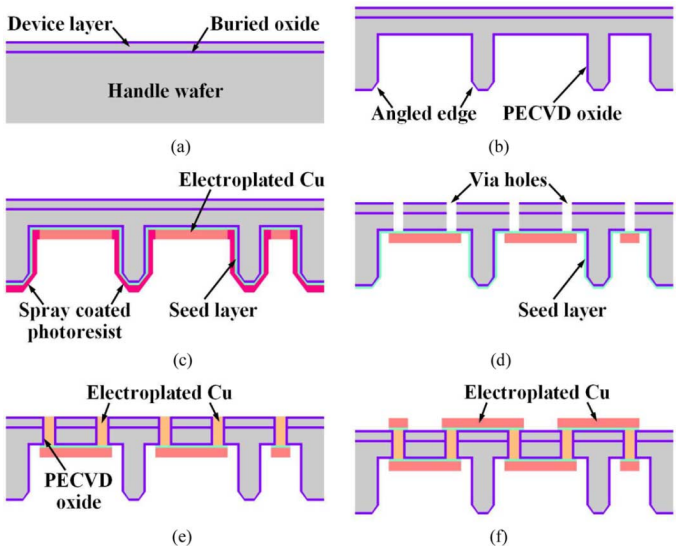


Fig. 5. Cross-sectional view of the daisy-chain fabrication process: (a) substrate with nitride passivation layer on top surface; (b) trench formation and PECVD oxide deposition on the backside; (c) seed layer deposition, plating mold formation, and Cu plating at the bottom of the trench; (d) via formation on the front-side; (e) via sidewall passivation and Cu plating inside the via; (f) top-side structure formation by Cu plating.

source. The top copper structures are then formed by seed layer deposition, mold patterning, and copper plating [Fig. 5(f)].

IV. RESULTS AND DISCUSSION

A. Fabrication Results

Daisy-chain structures were successfully fabricated based on electrical continuity testing. As shown in Fig. 6(c) and (d), buried interconnect structures are well-defined at the bottom surface of the trench without any plated structures on the sidewalls or edges, which in turn proves the good coverage of these regions during the plating process. Although some unwanted plating may be observed due to pin-holes formed on the top-side edges during the electroplating process, the artifacts are removed during the seed layer removal process.

The dimensions of the fabricated buried interconnect structure were measured with white light interferometry. Due to the combined silicon etch process, the planar dimensions of the trenches are increased compared to the mask opening size (300×620 μm^2). The increase of the opening size ($381 \times 692\,\mu$m^2) is attributed mainly to the initial and final isotropic etch steps, while the bottom area of the trench is increased due to the final isotropic etch process. The increase of bottom connector width (211 μm), compared to the mask dimension (160 μm), is mainly caused by the proximity effect

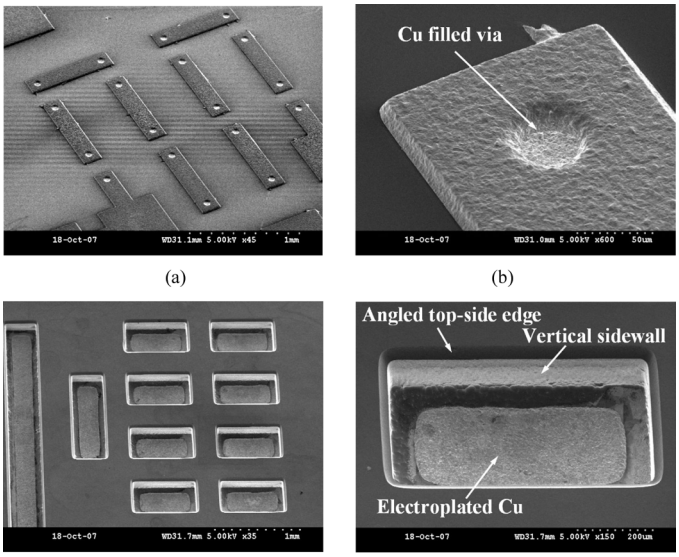


Fig. 6. SEM images of the fabricated daisy-chain structure: (a) top connectors; (b) close-up view of (a); (c) bottom connector; (d) close-up view of (c).

during the mold formation process. To maintain the structural integrity of the 61-μm-thick etched silicon regions, the substrate was mounted on a 500-μm-thick silicon dummy wafer with 10-μm-thick photoresist during the spray coating and lithography processes. As the lithography conditions detailed in [9] were optimized for a 500-μm-thick standard silicon substrate, the variation of overall sample thickness may have affected the optimal prebaking and exposure conditions. Since well-defined patterns were obtained by increasing the prebaking time by 100%, in-depth investigation on these conditions has not been performed. A better pattern definition with reduced size increase is expected with optimized prebaking conditions for substrates mounted on a dummy wafer. Control of the buried interconnect feature sizes, including the planar dimensions of the trench, can be achieved by compensating the mask design to account for dimensional variations due to processing.

The fabricated chain structure was partially diced and polished, and the cross section of the device was observed with scanning electron microscope (SEM) (Fig. 7). As shown in Fig. 7, three different layers of electroplated copper structures are well defined and connected as designed, without any void formed in the via. The bottom connector is slightly convex due to the curvature at the bottom surface of the deep etched trench, which is more evident in the white light interferometry profile in Fig. 8. The contact area of the top connector, joining the top surface of the copper filled via, is buried inside the via hole region due to the insufficient via plating process. The depth of the via hole $(h_{\mathrm{via-hole}})$, and thus the thickness of the silicon diaphragm on the front-side, was 61 μm and the thickness of the filled copper (h_{via}) was 46–51 μm [Fig. 7(d)]. The average thickness of the top and bottom connectors measured at five different positions on the substrate, were 12.5 and 20.3 μm, respectively.

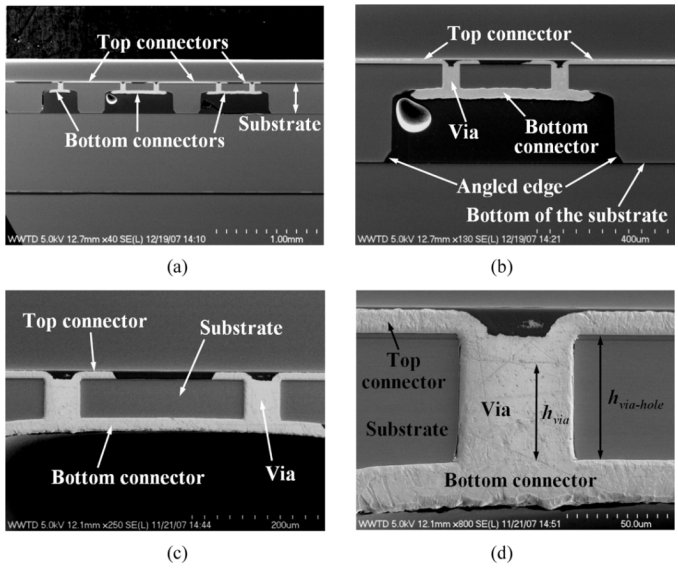


Fig. 7. SEM images of the cross-section: (a) full view of the cross-section of the daisy-chain structure; (b) close-up view of the trench, connectors, and via; (c) close-up view of the connectors and via; (d) close-up view of the via region.

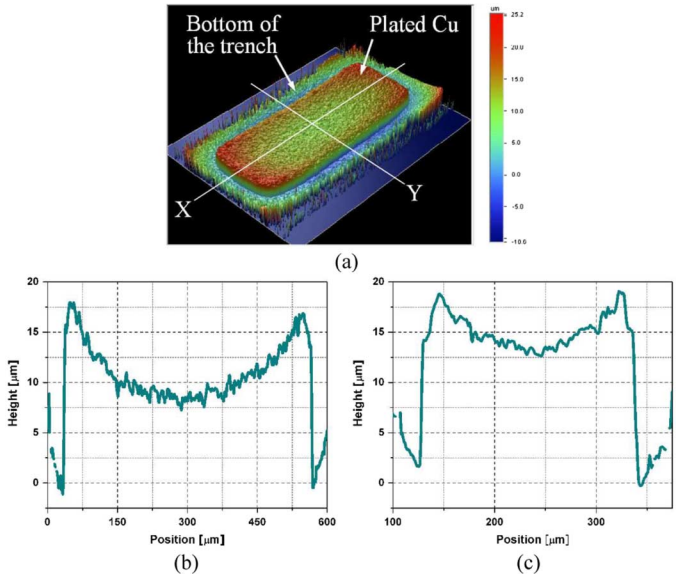


Fig. 8. Profile of the copper plated at the bottom of the trench: (a) 3-D profile; (b) X profile; (c) Y profile.

B. Electrical Characterization

The resistance of the fabricated daisy-chain structures were measured and compared with the analytic calculation and simulation results. Fig. 9 shows the resistance measurement result of 20 different positions on the substrate. The measured resistance ranged from 73.7 to 86.7 mΩ, with the average value of 80.1 mΩ, and standard deviation of 4.0 mΩ.

The resistance calculation and simulation were performed from one end of the pad to the other using the average value of the measured dimensions and copper resistivity (ρ) of 17.6 n$\Omega\cdot$ m. Fig. 10(a) shows the 3-D solid model used in the resistance simulation. The bottom connectors were assumed to be flat, and to better reflect the geometry of the fabricated

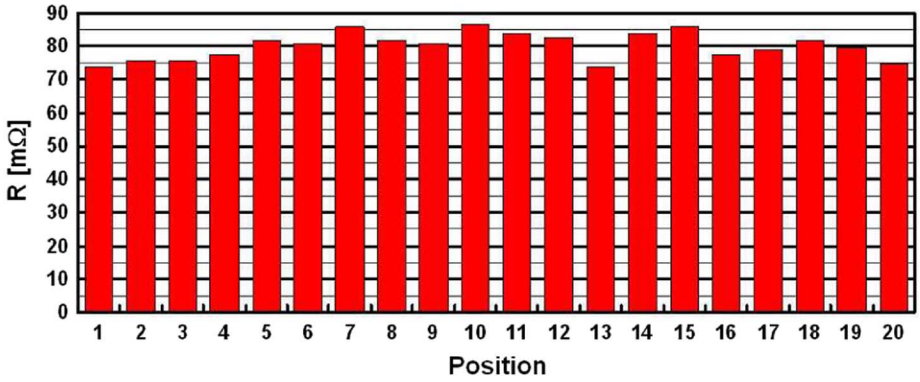
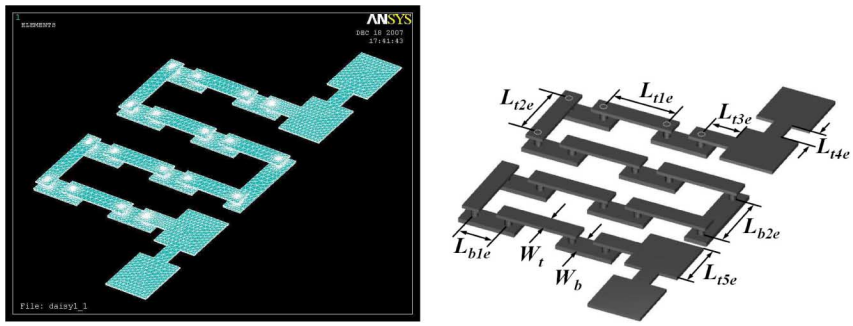


Fig. 9. Measured resistance of the fabricated daisy-chain structures.



(a) (b)

Fig. 10. Models used in resistance simulation and calculation: (a) solid model with elements used in the simulation; (b) geometry used in the resistance calculation and definition of dimensions ($L_{t1e} = 600\ \mu$m, $L_{t2e} = 600\ \mu$m, $L_{t3e} = 300\ \mu$m, $L_{t4e} = 200\ \mu$m, $L_{t5e} = 500\ \mu$m, $L_{b1e} = 320\ \mu$m, $L_{b2e} = 600\ \mu$m).

TABLE II
DIMENSIONS OF THE DAISY-CHAIN STRUCTURE USED IN RESISTANCE CALCULATION [DEFINED IN FIG. 10(B)]

Dimension [μm]	W_t	T_t	W_b	T_b	T_v	Via diameter
Mask	160		160			60
Measured value	158.7	12.5	210.8	20.3	61	66

daisy-chain structure, 46-μm-high partially filled via and conformally deposited top copper layer was considered in the solid model generation.

The resistance ($R_{\text{calculated}}$) was calculated as follows:

$$R_{\text{calculated}} = \rho \left\{ \frac{6L_{t1e} + 2L_{t2e} + 2(L_{t3e} + L_{t4e}) + 4L_{t5e}}{W_t T_t} + \frac{8L_{b1e} + L_{b2e}}{W_b T_b} + \frac{18T_v}{S_v} \right\} \quad (1)$$

where T_t and T_b are the thicknesses of the top and bottom connectors, and T_v and S_v are the height and cross-sectional area of the via, respectively. A 61-μm-high fully-filled via having diameter of 66 μm was used in the calculation. As the lateral distance between the vias, and thus the effective length of each top and bottom connectors [$L_{t1e}, L_{t2e}, L_{t3e}, L_{t4e}, L_{t5e}, L_{b1e}$, and L_{b2e} in Fig. 10(b)], were not affected by the processing, the dimensions defined in the mask were directly used in the calculation. The thickness and width of the connectors are measured at five different positions on the substrate and averaged. As summarized in Table II, the top connector width was slightly smaller than the mask dimension due to the narrowing of electroplating mold resulting from the overexposure of negative tone photoresist. The bottom connector width was increased due to the proximity effect during the lithography process. The calculated and simulated values of the resistances were 75.3 mΩ and 77.4 mΩ, respectively. The average value of the measured resistance is in good agreement with the calculation and simulation results, confirming the low resistivity and well defined geometry of the electroplated structure. The measured average resistance was 6.4% and 3.5% larger than the calculated and simulated resistances, respectively, indicating the resistivity of the electroplated copper approaches that of bulk copper. No shorts between neighboring structures were observed.

The power handling capabilities of the fabricated daisy-chain structure was tested by applying dc current to the fabricated structure. As shown in Fig. 11, the fabricated structure was able to support input power up to 9 W without structural damage,

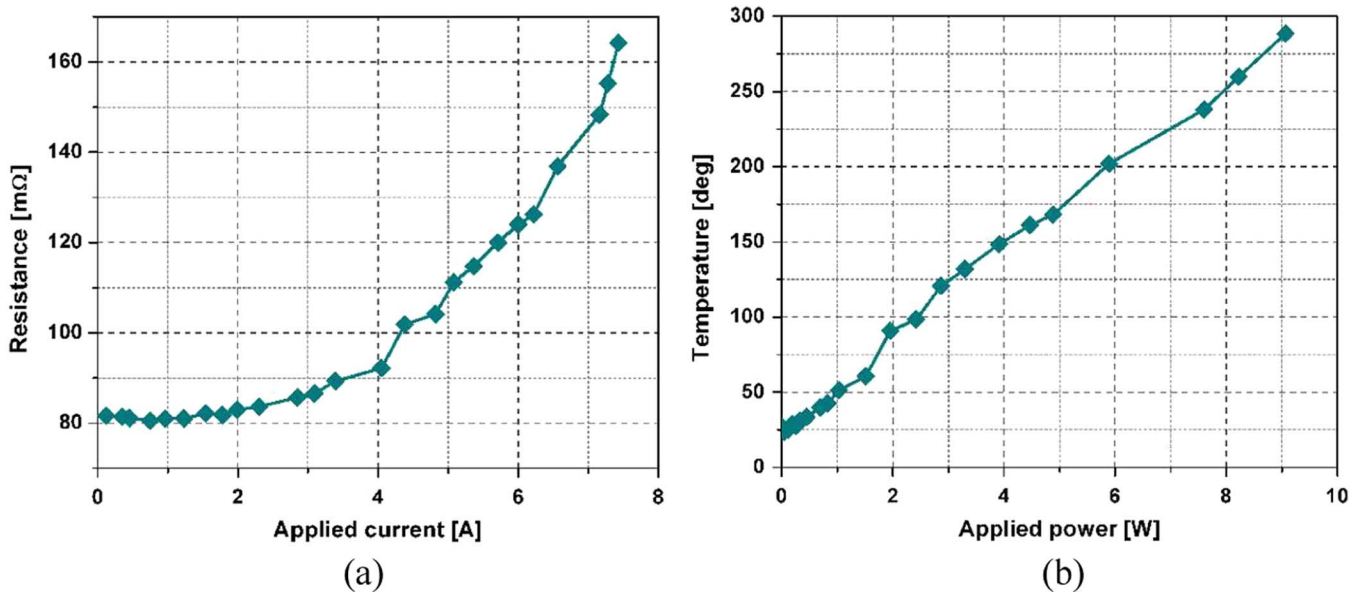


Fig. 11. Power handling characteristics of the fabricated daisy-chain structure: (a) applied current versus resistance; (b) estimated input power versus temperature (estimated from copper resistivity-temperature relations).

confirming the high power handling capability, as well as operation under the temperatures (up to 300 °C) produced by this high current flow.

V. Conclusion

We have successfully fabricated and characterized an electroplated daisy-chain structure with through-wafer via made of fully-filled metal, and buried interconnect as the bottom connector. For the fabrication of buried interconnects, a combined silicon etch process and a spray coating process optimized for deep trenches were used. A simple bottom-up plating process was applied for the filling of through-wafer vias having reduced height of 61 μm. The fabricated daisy-chain structure has been verified by cross-section observation of the final structure and electrical characterization. The resistance of the fabricated structure was measured and compared with the analytical and simulation results based on the measured dimensions. The measured average resistance of 80.1 mΩ was in good agreement with the calculated resistance of 75.3 mΩ and simulation result of 77.4 mΩ. The proposed structure and fabrication process can be useful for applications that require through-wafer interconnection or wafer-level packaging that require integrated electrical interconnections. The unique approach of thick metallization inside deep vertical trenches and height control of the through-wafer via obviates the need for substrate lapping/polishing and secondary bonding processes, while maintaining a lower resistance of interconnects.

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