CMOS Compatible Hermetic Packages Based on Localized Fusion Bonding of Fused Silica

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***Abstract*— Hermetic packages compatible with complementary metal–oxide–semiconductor (CMOS) processes and capable of transmitting RF and optical energy are in high demand. A hermetic packaging process based on the localized fusion bonding of patterned and stacked fused silica wafers to encapsulate a CMOS chip has been successfully demonstrated. The process also allows for feedthroughs to be fabricated within the package for wired interconnection to encapsulated devices. A carbon dioxide laser is applied to achieve localized fusion bonding of the fused silica stack. Exploiting vector motion of the laser, simultaneous bonding and dicing is achieved within 2 s. The low thermal conductivity of fused silica thermally isolates the CMOS chip from the bond area. The heat diffusion during the process is examined both experimentally and using finite element analysis. The temperature falls to CMOS compatibility levels (under 400°C) within a distance of 660 μm from the bond line. The viability of the packaging process and the hermeticity of the package are simultaneously evaluated by encapsulating a commercial MEMS humidity sensor within the package and monitoring the internal package humidity as a function of time. The packaged sensor was placed in an external relative humidity environment of 85% at 24°C and the relative humidity change inside the package was measured over a time span of 300 days. A water vapor leakage rate less than 4.6×10^{-14} atm·cm^3/s was observed. These preliminary results suggest that the hermeticity of the package can meet the criterion of implantation in human body for more than 70 years for a package with an inner volume of 0.0012 cm^3. [2018-0280]**

***Index Terms*— Fused silica, hermetic MEMS package, localized fusion bonding, MOEMS.**

I. Introduction

IMPLANTABLE microelectromechanical systems (MEMS) sensors and actuators have been widely adopted to monitor human health condition, improve quality of life, or save lives [1]–[3]. However, the packaging of the electronic circuitry for signal processing and wireless power transmission of these biocompatible devices are extremely challenging. Implantable packages should protect the transducers and associated electronic circuitry from the hostile environment of the human body, as well as maintain biocompatibility [4], [5]. For long duration implantations, these requirements often imply the need for a hermetic package.

In addition to the strict requirements of hermeticity and biocompatibility, provision must be made to communicate with the packaged devices. Recently, much attention has been focused on developing electromagnetically transparent packages [6]. Transparency at radio frequencies is necessary to realize wireless power and signal transmission. Metal, ceramic, and silicon dioxide are proved long-term hermetic and biocompatible materials which have been successfully applied in pacemakers [7], skeletal prostheses [8], vision prostheses [9], and so on. However, chronically implanted metallic packaged devices typically require battery replacement [10] or an external coil or antenna [11], due to the attenuation of radio frequency power through the metal. Transparency at optical frequencies enables the cooperation with micro-opto-electro-mechanical systems (MOEMS). Thus, nerve excitation/inhibition by light [12], visual monitoring, implantable optical sensors, etc. can be realized. Typical ceramic packages are not optically transparent; thus, a transparent port or window is required to enable light transmission [13], [14]. Silicon dioxide (fused silica/glass) is preferred as the protection cap because it is mechanically robust, chemically stable, and transparent to both optical light and radio frequencies [15].

Common silicon dioxide wafer bonding approaches include direct bonding (fusion bonding), anodic bonding, and intermediate layer bonding.

Packages including a glass cap have been studied by several groups. Ziaie *et al*. presented glass-to-silicon anodic bonding (at 320°C with 2000 V for 10 min) for microstimulators and performed in vivo tests in guinea pigs [16]. Cheng *et al*. reported silicon-to-glass bonding with an aluminum interlayer. A microheater was fabricated to realize localized bonding at 700°C in 7.5 min [17]. Chiao *et al*. bonded a glass and silicon substrate using aluminum as a bonding solder by rapid thermal processing with a peak temperature of 990°C for 2 seconds [18]. Glass has also been bonded to ceramic as a transparent window for digital micro-mirror devices (DMD) or optical MEMS using polymer adhesives with additional getters or using solder paste [19], [20].

Some researchers have also investigated whole fused silica/glass packages with intermediate layers. Nagarkar *et al*. presented fused silica-to-fused silica bonding exploiting an intermediate metal bonding layer for neural interfaces [21].

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Ji *et al*. demonstrated glass-to-glass bonding using benzocyclobutane (BCB) as an adhesive [22].

Direct fusion bonding without interlayers is considered a very robust bonding technique [23]; nevertheless, it is frequently criticized for the requirement of overall high temperature (600–1200 °C) and long processing time [24]. These conditions may render direct fusion bonding unsuitable for encapsulating lower temperature materials, including complementary metal oxide semiconductor (CMOS) [25]–[27] MEMS and circuitry. CMOS-compatible processes are often limited to temperatures less than 400°C [28], lower than typical fusion bonding temperatures.

The simultaneous requirements of high fusion temperature and low CMOS-compatibility temperature may be overcome by the exploitation of localized heating at interfaces. Laser assisted local bonding technologies, with their high precision, good selectivity, high speed, and low overall heat-induced distortion, are attractive approaches for localized heating and are being progressively used in industrial applications [29]–[31]. This approach has also been extended to wafer substrates. Localized direct bonding of glass-silicon has been achieved by using transmission bonding technology with a Neodymium: Yttrium Aluminum Garnet (Nd:YAG) laser, where the laser beam is transmitted through the top glass wafer and is absorbed by the surface region of the silicon substrate. At this silicon-glass interface, this absorbed energy melts a local region of the silicon surface and a thin layer of glass, resulting in a local bonding of the two wafers [32]. W. Watanabe *et al.* reported femtosecond laser-assisted direct bonding of borosilicate glass - borosilicate glass and fused silica - fused silica. At the interface of the two wafers, localized melting and quenching occur [33]. This technique provides bonding velocities up to 1 mm/s for borosilicate glass substrates and up to 0.01 mm/s for fused silica substrates. Several laser-assisted bonding methods with intermediate layers have been studied for silicon-silicon, silicon-glass, silicon-ceramic, or glass-glass bonding, including benzocyclobutene (BCB) polymer [34], glass frit [35], indium [30], aluminum [36], lead-tin solder (Pb37/Sn63) [37], gold-tin solder (Au80/Sn20) [38], etc. It is also possible to utilize laser approaches for the dicing of individual wafers. Laser-assisted dicing for glass [39], [40] and ultrathin silicon wafers [41], [42] has the merits of dry processing, reduced mechanical stress, and the ability to create irregular shapes when compared to traditional blade dicing.

In this paper, we demonstrate a carbon dioxide (CO_2) laser-assisted local heating technology that simultaneously bonds and dices fused silica wafer stacks, while maintaining CMOS-compatible temperatures within cavities embedded in the wafer stacks. The process exploits the highly localized heating of a vector-position-controlled laser, together with the high thermal isolation of fused silica, to prevent significant heat from propagating between the fusion bond and the encapsulated chip. This approach can be performed while maintaining a rapid bonding velocity in excess of 15 mm/s. Further, multiple feedthroughs into the cavities are demonstrated without compromising package hermeticity. The thermal effects of the process are studied by a customized aluminum film calibration approach, and are numerically modeled to understand the relationship between package geometry, laser power, and CMOS-compatibility.

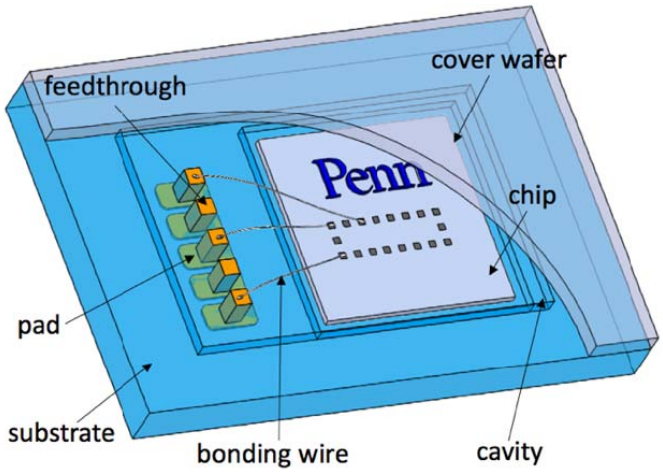

Fig. 1. Schematic illustration of a fused silica package with optional feedthroughs for hermetic sealing of encapsulated devices. There is no interlayer between the cover wafer and the fused silica substrate.

Key features of packages produced using this process include: 1) Biocompatibility, good hermeticity to moisture, transparency to radio frequencies and visible light; 2) Multiple feedthroughs for electronic access; 3) Localized fusion bonding with a safety distance of 660 μm from the edge of the package to the device; 4) Simultaneous bonding and dicing within 2 seconds. This wafer level technology will be very useful for other implantation and MOEMS applications.

In addition to localized fusion bonding by using a CO_2 laser, fused silica patterning (e.g., to create cavities within silica wafer stacks) by excimer laser is also introduced. This excimer laser technology provides an optional fabrication method to realize the patterned stacks of fused silica to be subsequently fusion bonded. In the following sections, the package design and principle of the technology is presented. The fabrication process for the package and the characterization of the thermal distribution during the fusion bonding is studied. Finally, the hermeticity of the package is discussed.

II. Package Design and Principles

A. Package Concept

Fig. 1 shows a schematic illustration of the hermetic package. The package comprises two fused silica layers. The first layer is a base substrate into which a cavity has been formed that will hold the electronic devices to be encapsulated. This cavity can be optionally configured with multiple feedthroughs and underlying connection pads; these feedthroughs can be electrically connected to the encapsulated electronic devices using typical interconnection approaches such as wire bonding or bump bonding. The second layer is a cover wafer which is bonded to the first base substrate layer utilizing localized fusion bonding. This localized bonding technology provides the mechanical strength and hermeticity for the package.

Also note that the fused silica fabricated package is transparent to optical and RF frequencies.

B. Package Design

As discussed above, the fused silica package comprises a base substrate layer with a cavity, and a cover layer for encapsulation. To pattern the cavity within the base substrate, multiple approaches are available, including dry etching, wet etching, physical etching, and laser ablation. In this work, excimer laser ablation (IPG IX-255, wavelength 193 nm) is utilized [43] due to its maskless nature, rapid process time, and inherent anisotropy. One drawback of this approach is that the cavity surface roughness may be higher using this approach.

Traditional fusion bonding, in which the entire sample is heated, would subject the encapsulated devices to unacceptably high temperatures. Thus, localized fusion bonding of the base substrate layer to the cover layer is utilized. To achieve this highly localized bonding, the high degree of flatness of the fused silica wafer surfaces is exploited. The fused silica layers are cleaned and Van der Waals bonded to form a temporary unitary structure. Cleaning should be carried out in a cleanroom environment. Piranha solution (H_2SO_4:H_2O=3:1) at 80°C for 20 minutes was used to remove any organic contaminants on fused silica substrate. This cleaning was followed by sonication with deionized (DI) water for 30 minutes. Localized fusion bonding is performed by a vector-controlled, focused CO_2 laser operating at 10.6 μm. The high absorptivity of the fused silica at this wavelength causes extreme (> 1000°C) local heating, forming Si-O-Si bonds [44] as well as melting and partially or entirely vaporizing regions of the fused silica. This technique enables the simultaneous fusion and dicing of fused silica with various packaging shapes. Due to the extremely low thermal conductivity of fused silica, these hot regions formed during laser irradiation do not extend into the encapsulation cavity region.

Fig. 2 illustrates this localized fusion bonding technology by bonding two fused silica wafers. The two wafer stack comprises a lower wafer into which a cavity has been formed, and an upper cover wafer. Each wafer has a thickness of 500 μm. The two wafers are Van der Waals bonded at room temperature, and the perimeter of the wafer stack is singulated using a CO_2 laser. Note that the bond regions far from the package edge show a distinct boundary; however, at the fusion region near the package perimeter, the two wafers appear completely fused and the boundary disappears. Although the resultant bond strength was not quantitatively measured, the produced packages are qualitatively robust.

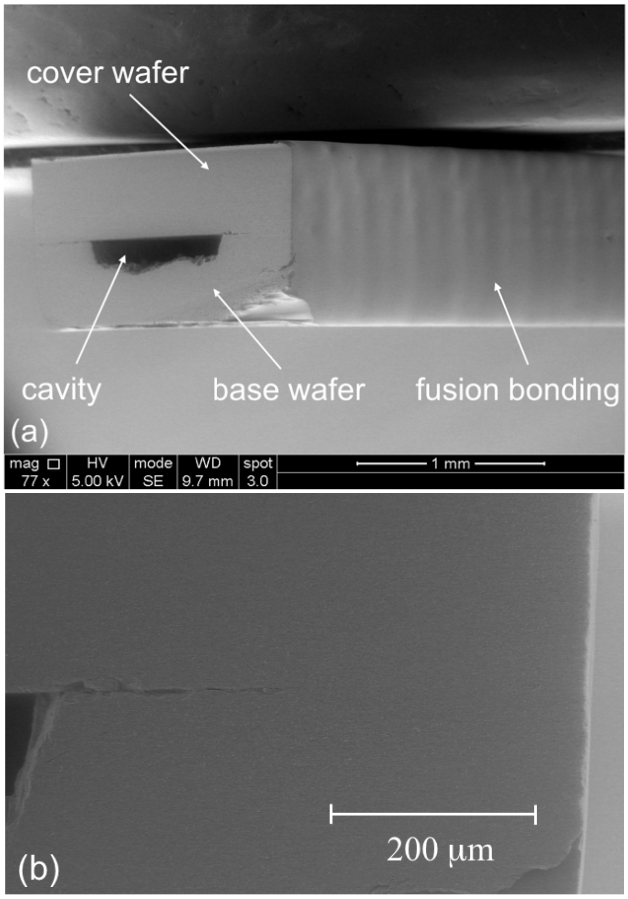

Fig. 2. (a) Localized fusion bonding of two fused silica wafers. The wafers were mechanically diced post-bonding to realize this cross-sectional profile. The damage in the lower right face of the package is a dicing artifact; (b) detail of bonding cross section.

III. Heat Distribution During Localized Fusion Bonding

In order to investigate the thermal distribution during the laser bonding process, as well as to identify the safety region where the temperature has fallen sufficiently to allow the devices within the package to retain functionality, the heat transfer during the process is simulated using COMSOL to yield the spatial and temporal temperature profiles of the package during the process. These simulations are verified experimentally using a deposited thin film aluminum indicator.

A. COMSOL Simulation

To simulate the temperature distribution during the fusion process, a COMSOL multiphysics simulation is performed using the heat transfer module. In this simulation, heat conduction and heat radiation are taken into consideration. To simulate the dicing process, the laser is vector-directed to dice a rectangular shape of 6 mm × 6 mm on a 20 mm diameter silica wafer. The simulation follows the path of a square shape from point A, to point B, C, D sequentially, and then back to point A, as shown in Fig. 3(a).

During the laser dicing, the incident heat flux from the laser is absorbed by the top surface of the wafer. Part of the energy diffuses over the entire wafer by heat conduction. The rest of the heat is radiated to the 25°C environment at an emissivity of 0.67 [45]. The laser spot is a Gaussian shape with a diameter (−3 to +3 standard deviation) of 130 μm and an average power of 75 W. The 6 mm × 6 mm square is traced in 1.6 second yielding a speed of 15.24 mm per second. The chosen simulation parameters conform with typical experimental parameters.

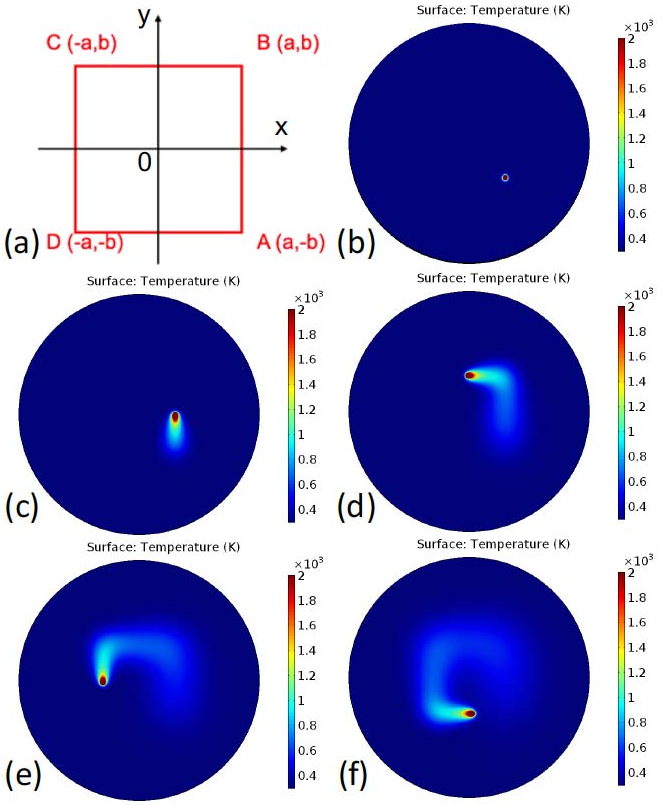

Fig. 3. COMSOL simulation, (a) Laser motion from A to B , C, D and back to A. (b) t = 0.01s; (c)t = 0.2 s; (d) t = 0.6 s; (e) t = 1 s; (f) t = 1.4 s.

Fig. 3 (b–f) presents the heat distribution over time and space during the laser dicing. The laser spot shows the highest temperature and the heat diffuses to the outer area. Since the heat diffusion takes time, a 'diffusion tail' develops along the laser path. As time passes, the 'tail' spreads out and gradually disappears.

In order to quantitatively investigate the thermal impact over time, consider the temperature distribution along the x-axis as shown in Fig. 3(a). The maximum temperatures should occur at the points where the laser spot crosses the x-axis, namely x = ±3 mm. Given the starting position of the laser spot, as the laser spot is moving from position A to position B in Fig. 3(a), the spot crosses the x-axis at t = 0.2 s, then continues away from the x-axis in the y-direction. The spot re-crosses the x-axis at x = −3 mm, which occurs at t = 1 s.

Fig. 4 shows the simulated temperature distribution as a function of position from x = −6 mm to x = 6 mm, parameterized by times between 0.2 second and 1.4 second. When the laser spot first reaches the x-axis at x = 3mm, the heat distribution is a narrow and sharp curve indicating a small and hot spot that reaches the melting temperature of fused silica (approximately 2000 K). After 0.2 second, the laser passes this line and the temperature curve becomes flatter and spreads over a larger distance due to thermal diffusion, with concomitant fall in temperature. Later, as the laser crosses the x-axis again at $x = -3$mm, a second narrow and sharp temperature curve is developed, which also diffuses with time. The region between these two curves

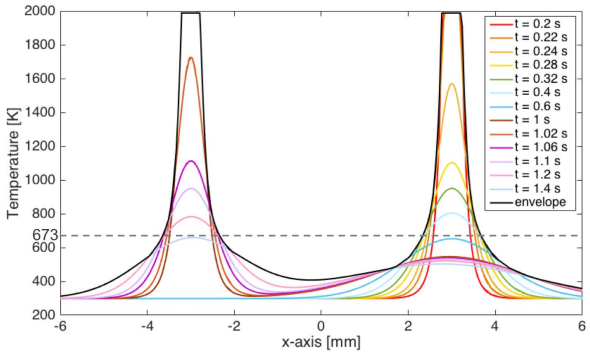

Fig. 4. Heat distribution within the fused silica wafer as a function of position along the x-axis and parameterized by time. Note the laser spot, moving in the y-direction, crosses the point x = 3 mm at time t = 0.2 s, and crosses the point x = −3mm at time t = 1s. The central region between the spots comprises the package, which maintains a temperature of less than 400°C at a distance from either spot that exceeds 660 microns.

(−3 < x <3 mm) ultimately will comprise the hermetic package. The low temperature achieved in the package after completion of the process is 134°C.

Of interest in package design is how close a packaged device can be placed to the edge of the package. This can be determined by considering the *highest* temperature achieved at any particular point within the package area at *any* time. Drawing the curve that circumscribes all of the simulation curves, yields the maximum temperature achieved as a function of distance from the laser spots. Taking 400°C (dashed horizontal line) as the maximum tolerable CMOS-compatible temperature suggests that a distance of 660 μm removed from either laser spot is the minimum safe distance for packaging these devices.

B. Heat Distribution Verification

The heat distribution simulation during laser dicing is verified by using a deposited thin film aluminum temperature indicator. Aluminum was chosen as an indicator material since (i) the appearance of the thin film aluminum does appreciably change over these temperature ranges; (ii) deposited aluminum is an easily integrable material with fused silica; and (iii) deposited aluminum is likely the material in CMOS circuits most vulnerable to high temperature, thus providing a direct optical measurement of the effects of this packaging technique on aluminum. In the experiments, we first present the appearance difference of the thin film aluminum as a function of distance from the laser spot. The aluminum film indicator is then semiquantitatively calibrated at specific controlled temperatures to assess the accuracy of the simulation.

1) Laser Impact on Thin Film Aluminum: To form a test coupon, a 200 nm aluminum film is deposited on the top surface of a fused silica wafer (Kurt J. Lesker, PVD75 E-Beam Evaporator) and patterned into arrays of thirty strips of aluminum with 10 μm width and 10 μm spacing using standard photolithography. The test coupon is positioned in a CO_2 laser (PLS4.75, Universal Laser Systems) such that the laser cut line, when cutting the fused silica parallel to the length direction of the strip array, is sufficiently far from the array

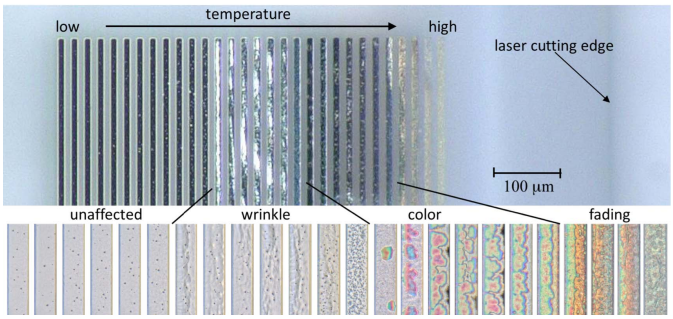

Fig. 5. Aluminum appearance change due to heat distribution of laser dicing.

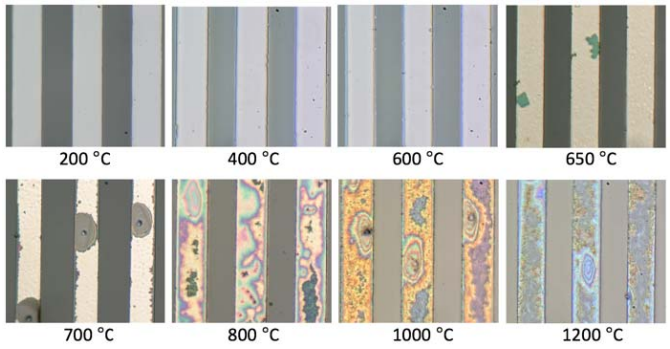

Fig. 6. Aluminum appearance change under temperatures from 200°C to 1200°C in furnace.

that all thirty array elements survive, yet sufficiently close to the array that a substantial portion of the array elements are affected. The laser setting is the same as in the simulation. After the laser cut, the aluminum sample shows variations in appearance with the difference of distances from the laser cut line, as shown in Fig. 5. From the nearest to the farthest spot from the laser cut edge, four regions are categorized: fading region, color region, wrinkle region, and unaffected region. The fading region is the nearest to the laser spot ($<$310 μm), thus under the highest temperature impact. The color region starts to appear at a distance of 310 μm to 450 μm from the laser spot. The wrinkle region (450 μm-590 μm) appears shiny in a zoomed-out view; and the unaffected region ($>$590 μm) does not show much difference from the original room temperature condition.

2) Aluminum Indicator Calibration: To identify the temperature corresponding to the appearance difference, we studied the appearance change of deposited thin film aluminum under specific temperature using a furnace. Thin film aluminum arrays are fabricated as described above. Arrays were then placed into a furnace at specific temperatures ranging from 200°C to 1200°C, and optically inspected upon removal.

The aluminum film changes are shown in Fig. 6. Below the melting point of aluminum, the sample appears unaffected. The color region, in which colorful spots appear, begins at approximately 650°C, which conforms to the melting temperature of aluminum at 660°C.

Based on the experiments, at a distance of 450 μm from the laser cut edge is the onset of the color region. Taking this point as the melting point of aluminum(660°C), it is possible to compare experiment and simulation. In the COMSOL simulation, the distance from the laser spot to 660°C is 425 μm (Fig. 4) which shows reasonable agreement with experiment. Note that the spot size and cut width have been neglected in the above analysis; however, the correspondence between this zero adjustable parameter model and experiment indicates the predictive utility of the model for future package design.

IV. Fabrication

The packaging process involves standard lithography, excimer laser etching, electrical interconnection, and CO_2-laser-based fusion bonding.

As described above, the package comprises a base wafer bearing a cavity to contain a chip and optional feedthroughs; and an encapsulating cover wafer. Fabrication proceeds on both the first side of the wafer (which will ultimately become the external surface of the base wafer), and the second side of the wafer (which will ultimately become the internal surface of the base wafer). A 700 μm thick fused silica wafer is employed as the base wafer. To fabricate the feedthroughs and connection pads on the base wafer, 30 nm of titanium and a 200 nm copper seed layer are deposited on the external surface of the base wafer, and photoresist electroplating molds for feedthrough pads are formed on top of the seed layer as shown in Fig. 7(a). A 40 μm thick copper pad is electrodeposited through the mold using a current density of 10 mA/cm^2. These pads will form the external connection points for the package. The photoresist and seed layers are then removed to facilitate optical alignment in subsequent steps (Fig. 7(b)).

After pad formation, the base wafer is rotated and fabrication proceeds on the internal side of the base wafer. Excimer laser (193nm) rastering in high fluence mode is implemented to form a 6 mm $\times$ 3.5 mm $\times$ 250 μm first cavity in the base substrate. Subsequently, five feedthrough vias of size 250 μm $\times$ 250 μm are formed by the excimer laser in this first cavity region and through the remaining thickness of the base wafer until the vias reach the copper pads on the external surface (Fig. 7(c)). To the right of the feedthrough, a second square cavity of 3.4 mm $\times$ 3.4 mm $\times$ 100 μm is further recessed using the excimer laser to accommodate the chip to be encapsulated. The feedthrough vias are then filled using electrodeposition with the aid of a redeposited and passivated seed layer formed on the external surface as shown in Fig. 7(d). This seed layer is then removed, completing the base wafer fabrication.

The next step in the packaging process is to place and encapsulate the chip. Two approaches will be investigated to illustrate this process: (i) encapsulation of a thinned SOI chip interconnected with wire bonding; and (ii) encapsulation of an epoxy-potted chip interconnected with bump bonding.

The SOI-based chip comprises a device layer and insulation layer (thickness of these layers is approximately 20 μm total), and a handle layer (thickness approximately 230 μm). To improve the volumetric efficiency of the package while maintaining chip functionality, the chip was thinned down to a total thickness of 110 μm using sulfur hexafluoride (SF_6)-based Deep Reactive Ion Etching (DRIE, SPTS Rapier Si DRIE). Chip electrical functionality was retained at even

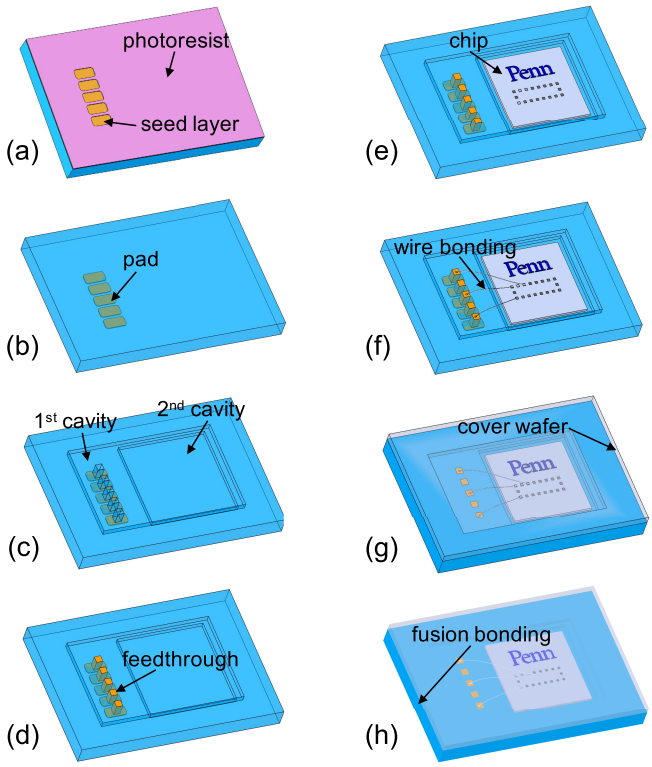

Fig. 7. Fabrication process of hermetic package: (a) deposit copper seed layer and fabricate photoresist mold; (b) copper electroplating for pads; (c) cavity and feedthroughs formed by excimer laser; (d) copper electroplating for feedthroughs; (e) chip attached to the cavity by die attach adhesive; (f) wire bonding between pads on chip and feedthrough; (g) cover wafer bonded to base substrate at room temperature; (h) CO_2 laser localized fusion bonding.

smaller thicknesses; e.g., down to complete removal of the handle layer. However, for demonstration purposes, as well as improved handling characteristics, the chip was thinned to 110 μm for subsequent packaging. The thinned chip is then fixed into the second cavity using die attach adhesive with the device layer oriented upwards, as presented in Fig. 7(e). Interconnection of power, ground, and output pads of the chip to the package feedthroughs is achieved using 25 micron aluminum wire (Kulicke 4523 Wire Bonder) (Fig. 7(f)).

A cover wafer of fused silica 500 μm in thickness is affixed to the internal surface of the base wafer, as demonstrated in Fig. 7(g), and Van der Waals bonded at room temperature. A CO_2 laser is used to simultaneously fuse and dice the wafers at the edges, as shown in Fig. 7(h). The shape of the package is defined in an AutoCAD file and exported to the CO_2 laser controller. This fusion bonding process takes 1.6 second to fuse a 7.8 mm $\times$ 5 mm rectangular shape.

The packaged chip is shown in Fig. 8, with detailed views (top, bottom, and side) shown in Fig. 9. Since the fused silica is transparent, devices can be clearly seen from outside. From the top view, as shown in Fig. 9(a): the circuit is the square on the left and the feedthroughs are on the right side. Three bond wires internal to the package connect the chip and the feedthroughs. The nearest point from the laser spot to the chip is 0.7 mm which conforms to the safety distance of 660 μm from the simulation. In the package side view shown in Fig.

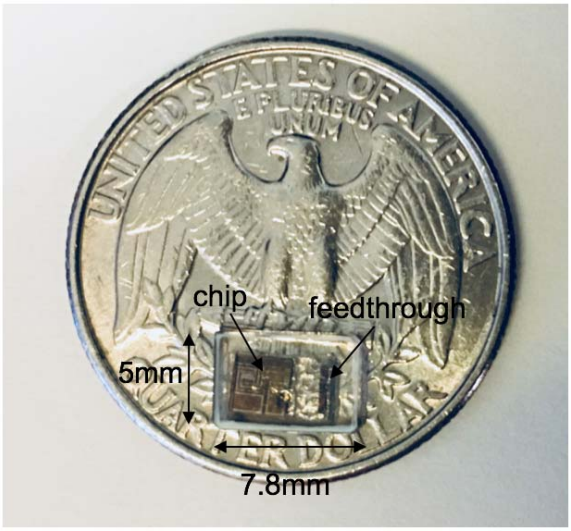

Fig. 8. Photograph of hermetically packaged device.

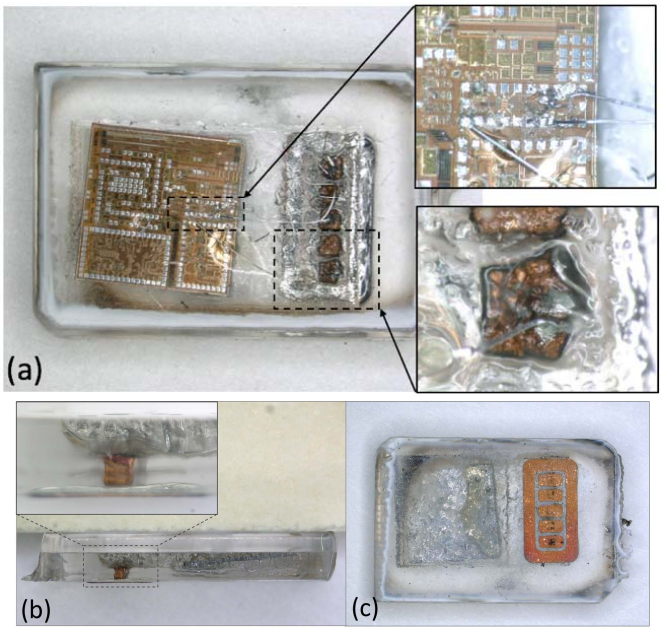

Fig. 9. SOI chip package with wire bonding: (a) top view; (b) side view; (c) bottom view.

9(b), the top wafer without cavity is the cover wafer and the bottom wafer with cavity is the base wafer. The feedthrough filled with electroplated copper can be seen. In the bottom view of Fig. 9(c), the interconnect pads for subsequent chip testing are evident on the right.

In addition to the package process illustrated above for the encapsulation of a thinned SOI chip interconnected with wire bonding, encapsulation of an epoxy-potted chip interconnected with bump bonding is introduced. The encapsulation process of the epoxy-potted chip, as shown in Fig. 10, follows the same initial fabrication steps as previously presented (Fig. 10(a-d)), with some alterations in dimensions. Fabrication begins with deposition of a copper seed layer on the external surface of a 700 μm thick fused silica base wafer and patterning of photoresist molds for feedthrough pads, as shown in Fig. 10(a),

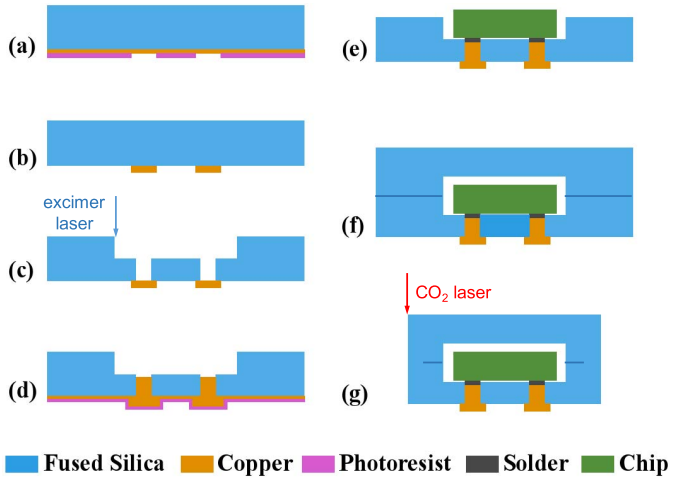

Fig. 10. Fabrication process of hermetic package for an epoxy-potted chip: (a) deposit copper seed layer and fabricate photoresist mold; (b) copper electroplating for pads; (c) cavity and feedthroughs formed by excimer laser; (d) copper electroplating for feedthroughs; (e) chip attached to the cavity by solder paste; (f) cover wafer with cavity bonded to base substrate at room temperature; (g) CO_2 laser localized fusion bonding.

and pads are electroplated as shown in Fig. 10(b). The mold patterns correspond to the pattern of the solder bumps of the chip to be encapsulated. Excimer laser patterning is utilized to fabricate a partial encapsulation cavity (2.3 mm $\times$ 1.9 mm $\times$ 350 μm, Fig. 10(c)). Subsequently, feedthrough vias of 250 μm $\times$ 250 μm are patterned by excimer laser through the cavity until the vias reach the electroplated copper pad on the external surface of the base wafer. These feedthroughs are later filled with electroplated copper, as illustrated in Fig. 10(d).

To connect and stabilize the chip to be packaged, solder paste is applied to the feedthrough pads on the internal side of the base wafer. The chip with solder bumps is then placed into the cavity, the bumps are aligned with the feedthrough pads, and the package is heated to 220°C on a hot plate, fixing the chip to the feedthrough pads (Fig. 10(e)).

The extra height of the potted chip and solder balls necessitates the formation of a complementary cavity in the cover wafer to accommodate the chip volume. A cavity recess (2.3 mm $\times$ 1.9 mm $\times$ 350 μm) is formed in a 700 μm cover wafer using excimer laser ablation. The cover wafer and the base wafer are then Van der Waals bonded at room temperature (Fig. 10(f)). Finally, the CO_2 laser is utilized to simultaneously dice the package and locally fuse the multilayer stack at the edges to fabricate a 6 mm $\times$ 6 mm package (Fig. 10(g)).

Fig.11 shows the encapsulated chip with solder bumps. This encapsulated chip is a commercialized digital relative humidity sensor (HDC1008, Texas Instruments, 2.04 mm $\times$ 1.59 mm $\times$ 675 μm) with 8 solder bumps at the bottom (Fig. 11(a)). From the top view of the package (Fig. 11(b)), the smallest rectangle in the middle is the sensor under the laser fabricated cover wafer and the copper pads on the bottom can be seen from the top view due to the transparency of silica wafer. From the bottom view, there are eight pads and seven laterally-extended regions for subsequent external connection (Fig. 11(c)). This asymmetric design of the laterally-extended regions provides an indication for orientation of the

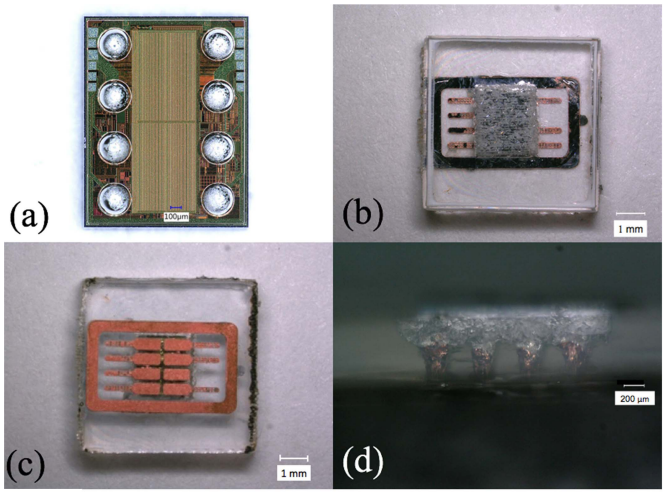

Fig. 11. Chip package with bump bonding: (a) humidity sensor with solder bumps; (b) top view; (c) bottom view; (d) side view.

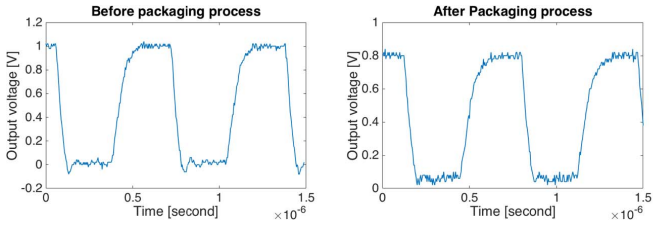

Fig. 12. SOI chip output clock signal before and after packaging. The SOI chip has undergone the thinning and packaging process without loss of functionality.

encapsulated chip. The cross-sectional view in Fig. 11(d) shows the feedthroughs are completely filled with electroplated copper with 500 μm spacing.

V. Results and Discussion

A. Circuit Testing

To verify the viability of the thinned SOI chip after the packaging process, as well as to demonstrate the feasibility of the bonding wire and feedthroughs, the encapsulated SOI chip containing a clock circuit was tested. The input of this clock circuit is a DC voltage of 1.5 V relative to ground with an output clock signal of 1.6 MHz. The dimensions of the chip were 3 mm $\times$ 3 mm $\times$ 110 μm (after thinning) with 50 μm $\times$ 50 μm pads for electronic connections. As shown in Fig. 12, the output clock signal after the packaging process is present and the pre-packaging clock frequency is maintained, verifying that the circuit, wire bonds, feedthroughs, and pads are all functional.

B. Hermeticity Testing

Since the solder bump interconnected chip is also a humidity sensor, it can in principle be used to monitor water vapor leakage and thereby evaluate the package hermeticity [46]. Inputs of this digital sensor include a 5 V DC supply relative to ground, address selection signal, clock signal, and data

TABLE I
PERFORMANCE OF VARIOUS PACKAGING TECHNOLOGIES

Paper	Material	Bonding method	Bonding condition	Cavity volume [cm^3]	Helium leakage rate [$atm \cdot cm^3/s$]	Testing method
This paper	fused silica-fused silica	laser assisted fusion bonding	~400 °C	1.2×10^{-3}	9.8×10^{-14}* (H_2O 4.6×10^{-14})	packaged humidity sensor
[38]	silicon-ceramic	laser assisted intermediate Au80/Sn20	—	0.05-0.5	$< 10^{-8}$	helium leak test
[49]	glass-silicon	laser assisted intermediate BCB polymer	~ 300 °C	2×10^{-4}	$\sim 10^{-10}$	helium leak test
[50]	glass-silicon	anodic bonding	~1000 V ~ 420 °C	1×10^{-2}	$< 10^{-9}$	helium leak test
[51]	glass-silicon	intermediate Au	~ 370 °C	—	3.5×10^{-14}* (Air 1.3×10^{-14})	packaged pressure sensor
[52]	silicon-silicon	intermediate AuSn	400 °C	$\sim 6.89 \times 10^{-3}$	2.3×10^{-9}* (Air 8.4×10^{-10})	diaphragm deflection measurement
[53]	silicon-silicon	intermediate Cu/Sn	260 °C	—	1.9×10^{-8}	helium leak test
[54]	silicon-silicon	intermediate Cu	250 °C	1.74×10^{-4}	9.6×10^{-16}* (Air 3.6×10^{-16})	residue gas analysis
[9]	ceramic-ceramic	intermediate glass	550 °C	0.05	$< 10^{-12}$	helium leak test
[5]	metal-ceramic	intermediate SnPb	350 °C	0.57	$< 10^{-12}$	helium leak test

*Calculated as equivalent helium leak rate using the method described in [48]; original data from cited papers is included in brackets.

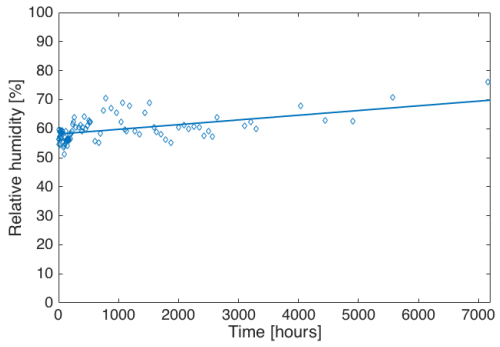

Fig. 13. Humidity inside the package.

signal. An external microcontroller MSP430F149 is utilized to generate the input signals for humidity detection. The output digital signals are then converted to corresponding relative humidity.

The initial humidity inside the package was approximately 58% because the bonding of the two wafers was performed in open air. If required, bonding can be performed in a wafer bonder under vacuum or other desired environment. The package with the humidity sensor was then tested by placing it in an external environment of 85% humidity and 24°C for more than 300 days, and measuring the relative humidity inside the package utilizing the encapsulated sensor. The results, shown in Fig. 13, exhibit a small increase of relative humidity with time, from which a water vapor transport rate could be calculated. Considering this relative humidity change, inner volume of 0.0012 cm^3, and the testing environment, the leakage rate of the package did not exceed 4.6×10^{-14} $atm \cdot cm^3/s$. As discussed in [16], four possible sources or water vapor leakage into the package are: 1) diffusion of water vapor through the fused silica; 2) water vapor leakage through any flaws present in the silica package layers, including the bonded regions; 3) water vapor leakage at interface between the fused silica and copper feedthroughs; and 4) potential outgassing of the encapsulated components. A getter located within the package could also improve the hermetic performance [47]. Table I presents package performance from various packaging technologies.

Assessment of this package leakage rate allows for the prediction of lifetime in various application scenarios. For example, consider hermetically-encapsulated electronic circuitry

embedded within the human body. One standard for this application is to predict the time necessary for the internal package environment to reach a water vapor concentration of 5000 ppm [2]. This time can be predicted from (1) [48]:

$$t = -\frac{V}{L_{H_2O}}[\ln(1 - \frac{Q_{H_2O}}{\Delta p_{i,H_2O}})] \quad (1)$$

where V is the available inner volume of the package; L_{H2O} is the water vapor leakage rate; Q_{H2O} is the maximum allowable concentration of water in the package (in this case, 5000 ppm); and $\Delta p_{i,H2O}$ is the initial difference between the water vapor partial pressure in the human body and the water vapor partial pressure inside the package. Substituting the values for the tested package of V =0.0012 cm^3, $L_{H2O} = 4.6 \times 10^{-14}$ atm·cm^3/s, and, assuming in actual application the package initially contains no water, $\Delta p_{i,H2O}$ =0.061 atm, (1) predicts a usable lifetime of 70.7 years in the human body environment before the interior water vapor concentration of the package reaches 5000 ppm.

VI. Conclusions

In this article, we have successfully packaged SOI based chips with fused silica by a localized fusion bonding technology based on laser machining. Two methods for internal electronic connections are exploited: wire bonding for chip with concentrated pads and solder bonding for chip with solder bumps. To determine heat impact during the laser bonding, a finite element simulation using COMSOL is performed. This simulation indicates that a minimum distance of 660 μm from the laser cutting edge to the device is sufficient to keep the CMOS device intact. Further experiment verifies the simulation is reasonable.

To demonstrate the process compatibility with foundry CMOS, a SOI chip was successfully encapsulated into the package and the functionality is verified after packaging. To evaluate the hermeticity, a commercial humidity sensor is encapsulated and tested over 300 days. Detected relative humidity change indicates a water vapor leakage rate not exceeding 4.6×10^{-14} atm·cm^3/s. This hermetic packaging technology can further be applied to various electronic devices for implantable human health detection systems incorporating radio frequencies and optical light transmission.

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References

[1] L. Du and M. G. Allen, "Silica hermetic packages based on laser patterning and localized fusion bonding," in *Proc. IEEE Micro Electo Mech. Syst.*, Belfast, U.K., Jan. 2018, pp. 551–554.

[2] G. Jiang and D. D. Zhou, "Technology advances and challenges in hermetic packaging for implantable medical devices," in *Implantable Neural Prostheses 2*. Berlin, Germany: Springer, 2010, pp. 27–61.

[3] A. Kiourti and K. S. Nikita, "A review of in-body biotelemetry devices: Implantables, ingestibles, and injectables," *IEEE Trans. Biomed. Eng.*, vol. 64, no. 7, pp. 1422–1430, Jul. 2017.

[4] L. Bisoni *et al.*, "Investigation on the hermeticity of an implantable package with 32 feedthroughs for neural prosthetic applications," in *Proc. 38th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Orlando, FL, USA, Aug. 2016, pp. 1967–1970.

[5] M. Schuettler *et al.*, "Fabrication and test of a hermetic miniature implant package with 360 electrical feedthroughs," in *Proc. 32nd Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Buenos Aires, Argentina, Aug./Sep. 2010, pp. 1585–1588.

[6] T. J. Harpster and K. Najafi, "Long-term testing of hermetic anodically bonded glass-silicon packages," in *Proc. IEEE Int. Conf. Micro Electro Mech. Syst.*, Las Vegas, NV, USA, Jan. 2002, pp. 423–426.

[7] W. H. Ko and T. M. Spear, "Packaging materials and techniques for implantable instruments," *IEEE Eng. Med. Biol. Mag.*, vol. 2, no. 1, pp. 24–38, Mar. 1987.

[8] S. F. Hulbert, F. A. Young, R. S. Mathews, J. J. Klawitter, C. D. Talbert, and F. H. Stelling, "Potential of ceramic materials as permanently implantable skeletal prostheses," *J. Biomed. Mater. Res.*, vol. 4, no. 3, pp. 433–456, 1970.

[9] J. Ordonez, P. Dautel, M. Schuettler, and T. Stieglitz, "Hermetic glass soldered micro-packages for a vision prosthesis," in *Proc. IEEE 34th Annu. Int. Conf. EMBS*, San Diego, CA, USA, Aug./Sep. 2012, pp. 2784–2787.

[10] V. S. Mallela, V. Ilankumaran, and N. S. Rao, "Trends in cardiac pacemaker batteries," *Indian Pacing Electrophysiol. J.*, vol. 4, no. 4, pp. 201–212, 2004.

[11] T. Campi, S. Cruciani, F. Palandrani, V. De Santis, A. Hirata, and M. Feliziani, "Wireless power transfer charging system for AIMDs and pacemakers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 633–642, Feb. 2016.

[12] L. Rudmann, S. D. Huber, J. S. Ordonez, and T. Stieglitz, "Fused silica microlenses for hermetic packages as part of implantable optrodes," in *Proc. 37th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Milan, Italy, Aug. 2015, pp. 7143–7146.

[13] Y. Peng, S. Wang, H. Cheng, and M. Chen, "Whole inorganic hermetic packaging technology using localized induction heating for deep ultraviolet light-emitting diodes," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 9, pp. 1456–1461, Sep. 2016.

[14] K. Gilleo and S. Corbett, "Getter—Molecular scavengers for packaging," in *Proc. HDI*, Jan. 2001, pp. 26–29.

[15] Z.-H. Liang, Y. T. Cheng, W. Hsu, and Y.-W. Lee, "A low temperature wafer-level hermetic MEMS package using UV curable adhesive," in *Proc. 54th IEEE Electron. Compon. Technol. Conf.*, Las Vegas, NV, USA, Jun. 2004, pp. 1486–1491.

[16] B. Ziaie, J. A. V. Arx, M. R. Dokmeci, and K. Najafi, "A hermetic glass-silicon micropackage with high-density on-chip feedthroughs for sensors and actuators," *J. Microelectromech. Syst.*, vol. 5, no. 3, pp. 166–179, Sep. 1996.

[17] Y. T. Cheng, L. Lin, and K. Najafi, "A hermetic glass-silicon package formed using localized aluminum/silicon-glass bonding," *J. Microelectromech. Syst.*, vol. 10, no. 3, pp. 392–399, Sep. 2001.

[18] M. Chiao and L. Lin, "Hermetic wafer bonding based on rapid thermal processing," *Sens. Actuators A, Phys.*, vol. 91, no. 3, pp. 398–402, Jul. 2001.

[19] K. Gilleo, "Photonics challenge to electronic packaging," *IEEE Trans. Compon. Packag. Technol.*, vol. 24, no. 2, pp. 309–311, Jun. 2001.

[20] F. Seigneur, Y. Fournier, T. Maeder, P. Ryser, and J. Jacot, "Hermetic package for optical MEMS," *J. Microelectron. Electron. Packag.*, vol. 6, no. 1, pp. 32–37, Jan. 2009.

[21] K. Nagarkar, X. Hou, N. Stoffel, E. Davis, J. Ashe, and D. Borton, "Micro-hermetic packaging technology for active implantable neural interfaces," in *Proc. IEEE 67th Electron. Compon. Technol. Conf.*, Orlando, FL, USA, Jun. 2017, pp. 218–223.

[22] Y. Ji, Q. Gan, L. Wu, J. Shang, and C.-P. Wong, "Wafer-level hermetic all-glass packaging for microalkali vapor cells of chip-scale atomic devices," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 11, pp. 1551–1558, Nov. 2015.

[23] Y.-T. Cheng, "Localized heating and bonding technique for MEMS packaging," Ph.D. dissertation, Dept. Elect. Eng., Univ. Michigan, Ann Arbor, MI, USA, 2000.

[24] F. Niklaus, G. Stemme, J.-Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding," *J. Appl. Phys.*, vol. 99, no. 3, 2006, Art. no. 031101.

[25] M. Shahriar Rahman, M. M. Chitteboyina, D. P. Butler, Z. Celik-Butler, S. P. Pacheco, and R. V. McBean, "Device-level vacuum packaging for RF MEMS," *J. Microelectromech. Syst.*, vol. 19, no. 4, pp. 911–918, Jul. 2010. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=5508328

[26] C. Harendt, H. G. Graf, B. Hofflinger, and E. Penteker, "Silicon fusion bonding and its characterization," *J. Micromech. Microeng.*, vol. 2, no. 3, pp. 113–116, 1992.

[27] D. Ando, K. Oishi, T. Nakamura, and S. Umeda, "Glass direct bonding technology for hermetic seal package," in *Proc. IEEE 10th Annu. Int. Micro Electro Mech. Syst.*, Nagoya, Japan, Jan. 1997, pp. 186–190.

[28] A. Grossi *et al.*, "Impact of the precursor chemistry and process conditions on the cell-to-cell variability in 1T-1R based HfO_2 RRAM device," *Sci. Rep.*, vol. 8, Jul. 2018, Art. no. 011160.

[29] D. O. Brien, F. Cros, J. W. Park, M. Fonseca, L. You, and M. G. Allen, "Method of manufacturing a hermetic chamber with electrical feedthroughs," U.S. Patent 7 662 653 B2, Feb. 16, 2010.

[30] C. Luo and L. Lin, "The application of nanosecond-pulsed laser welding technology in MEMS packaging with a shadow mask," *Sens. Actuators A, Phys.*, vols. 97–98, pp. 398–404, Apr. 2002.

[31] S. Theppakuttai, D. B. Shao, and S. C. Chen, "Localized laser transmission bonding for microsystem fabrication and packaging," *J. Manuf. Process.*, vol. 6, no. 1, pp. 24–31, 2004.

[32] A. A. Tseng and J.-S. Park, "Using transmission laser bonding technique for line bonding in microsystem packaging," *IEEE Trans. Electron. Packag. Manuf.*, vol. 29, no. 4, pp. 308–318, Oct. 2006.

[33] W. Watanabe, S. Onda, T. Tamaki, and K. Itoh, "Direct joining of glass substrates by 1 kHz femtosecond laser pulses," *Appl. Phys. B*, vol. 87, pp. 85–89, Mar. 2007.

[34] Y. Liu, J. Zeng, and C. Wang, "Accurate temperature monitoring in laser-assisted polymer bonding for MEMS packaging using an embedded microsensor array," *J. Microelectromech. Syst.*, vol. 19, no. 4, pp. 903–910, Aug. 2010.

[35] Y. Xiao, W. Wang, and J. Zhang, "Accurate predetermination of the process parameters for glass/glass laser bonding based on the temperature distribution analysis," *J. Electron. Packag.*, vol. 138, no. 2, Apr. 2016, Art. no. 021006.

[36] U. M. Mescheder, M. Alavi, K. Hiltmann, C. Lietzau, C. Nachtigall, H. Sandmaier, "Local laser bonding for low temperature budget," *Sens. Actuators A, Phys.*, vols. 97–98, pp. 422–427, Apr. 2002.

[37] Y. Tao, A. P. Malshe, and W. D. Brown, "Selective bonding and encapsulation for wafer-level vacuum packaging of MEMS and related micro systems," *Microelectron. Rel.*, vol. 44, no. 2, pp. 251–258, Feb. 2004.

[38] Y. Tao, A. P. Malshe, W. D. Brown, D. R. DeReus, and S. Cunningham, "Laser-assisted sealing and testing for ceramic packaging of MEMS devices," *IEEE Trans. Adv. Packag.*, vol. 26, no. 3, pp. 283–288, Sep. 2003.

[39] Y. Izawa *et al.*, "Debris-free high-speed laser-assisted low-stress dicing for multi-layered MEMS," *IEEJ Trans. Sensors Micromach.*, vol. 128, no. 3, pp. 91–96, Jan. 2008.

[40] Z. Q. Huang, M. H. Hong, T. B. M. Do, and Q. Y. Lin, "Laser etching of glass substrates by 1064 nm laser irradiation," *Appl. Phys. A*, vol. 93, no. 1, pp. 159–163, Oct. 2008.

[41] V. R. Marinov, O. Swenson, Y. Atanasov, and N. Schneck, "Laser-assisted ultrathin die packaging: Insights from a process study," *Microelectron. Eng.*, vol. 101, pp. 23–30, Jan. 2013.

[42] K. Venkatakrishnan and B. Tan, "Thin silicon wafer dicing with a dual-focused laser beam," *J. Micromech. Microeng.*, vol. 17, no. 12, pp. 2505–2515, 2007.

[43] R. D. Schaeffer, "Laser theory and operation," in *Fundamentals of Laser Micromachining*, 1st ed. Boca Raton, FL, USA: CRC Press, 2012, pp. 5–35.

[44] H. Moriceau *et al.*, "Overview of recent direct wafer bonding advances and applications," *Adv. Natural Sci. Nanosci. Nanotechnol.*, vol. 1, no. 4, 2010, Art. no. 043004.

[45] B. T. Barnes, W. E. Forsythe, and E. Q. Adams, "The total emissivity of various materials at 100-500Â°C," *J. Opt. Soc. Amer*, vol. 37, no. 10, pp. 804–807, Oct. 1947.

[46] T. J. Harpster, S. Hauvespre, M. R. Dokmeci, and K. Najafi, "A passive humidity monitoring system for *in situ* remote wireless testing of micropackages," *J. Microelectromech. Syst.*, vol. 11, no. 1, pp. 61–67, Feb. 2002.

[47] D. R. Sparks, S. Massoud-Ansari, and N. Najafi, "Chip-level vacuum packaging of micromachines using NanoGetters," *IEEE Trans. Adv. Packag.*, vol. 26, no. 3, pp. 277–282, Aug. 2003.

[48] H. Greenhouse, "Water in sealed packages," in *Hermeticity of Electronic Packages*, 2nd ed. Oxford, U.K.: Elsevier, 2012, pp. 243–288.

[49] F. Bardin *et al.*, "Laser bonding of glass to silicon using polymer for microsystems packaging," *J. Microelectromech. Syst.*, vol. 16, no. 3, pp. 571–580, Jun. 2007.

[50] T. Akin, B. Ziaie, and K. Najafi, "RF telemetry powering and control of hermetically sealed integrated sensors and actuators," in *IEEE 4th Tech. Dig. Solid-State Sensor Actuator Workshop*, Hilton Head Island, SC, USA, Jun. 1990, pp. 145–148.

[51] T. J. Harpster, "Hermetic packaging and bonding technologies for implantable microsystems," Ph.D. dissertation, Dept. Elect. Eng., Univ. Michigan, Ann Arbor, MI, USA, 2005.

[52] S.-A. Kim, Y. H. Seo, Y.-H. Cho, G. H. Kim, and J. Bu, "Fabrication and characterization of a low-temperature hermetic MEMS package bonded by a closed loop AuSn solder-line," in *Proc. 16th Annu. Int. Conf. Micro Electro Mech. Syst.*, Jan. 2003, pp. 614–617.

[53] Z. Wu, J. Cai, Q. Wang, J. Wang, and D. Wang, "Wafer-level hermetic package by low-temperature Cu/Sn TLP bonding with optimized Sn thickness," *J. Electron. Mater.*, vol. 46, no. 10, pp. 6111–6118, Oct. 2017.

[54] X. Wang, S. J. Bleiker, M. Antelius, G. Stemme, and F. Niklaus, "Wafer-level vacuum packaging enabled by plastic deformation and low-temperature welding of copper sealing rings with a small footprint," *J. Microelectromech. Syst.*, vol. 26, no. 2, pp. 357–365, Apr. 2017.

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