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Analysis and optimization of vertically oriented, through-wafer, laminated magnetic cores in silicon

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Abstract

This paper compares two fabrication methods for achieving through-wafer, laminated magnetic cores in silicon, intended for microfabricated magnetic devices where vertically oriented (normal to the wafer) magnetic laminations are required to reduce eddy current losses. Given certain fabrication constraints for each method, a theoretical framework is presented to permit the design of the optimal lamination scheme for a particular application. As an example, the analysis is applied to the optimization of laminations for a miniaturized synchronous permanent magnet motor/generator.

1. Introduction

Magnetic microelectromechanical systems (MEMS), such as motor/generators [1], pumps [2], valves [3], etc, require careful optimization of the magnetic and mechanical structures. In many cases, bulk micromachining of silicon can be used to fabricate complex, three-dimensional mechanical structures with stable and well-characterized mechanical properties. To maximize the electromechanical coupling, innovative fabrication methods can be employed to integrate relatively voluminous conductors (for high currents) and magnetic cores (for high magnetic flux) into a silicon structure. While electrodeposition has proven to be a simple and effective method for batch fabrication of relatively thick, three-dimensional structures of conductive and magnetic materials, several design challenges still exist.

For devices with time-varying magnetic fields, such as high-speed magnetic actuators [1–3] or integrated power conversion devices [4], one challenge is the minimization of frequency-dependent magnetic losses, resulting from hysteresis and eddy current effects. Hysteresis losses can be minimized by careful control of the ferromagnetic alloy composition and microstructure [5]. Also, eddy current losses can be minimized by using either high-resistivity magnetic materials (ferrites) or by laminating the magnetic material into dielectrically separated thin sheets [6]. Conductive ferrous magnetic alloys, such as NiFe, are often preferred over ferrites because they support larger saturation flux densities and thus higher power densities.

In macroscale magnetic devices, low-loss laminated cores are typically achieved by pressing together alternating layers of magnetic and insulating materials. In contrast, the incorporation of magnetic laminations in batch-fabricated microscale devices poses a manufacturing challenge. The lamination thickness should be reduced to the order of the magnetic skin depth (typically 1–100 μm range for operation in the 1 kHz–1 MHz range) while maintaining a large total core thicknesses (10 μm–1 mm) to prevent saturation [6]. These requirements dictate large numbers of thin, high-aspect-ratio laminations, which are difficult to achieve using conventional microfabrication techniques [7, 8], especially when vertically oriented laminations (normal to the wafer surface) are required.

In a macroscopic laminated core designed for relatively low frequencies (<10 kHz), the width of the dielectric dividers is typically very small relative to the lamination width. However, for microfabricated devices designed for high-frequency operation, where very thin magnetic laminations are required, the thickness of the lamination dividers cannot be neglected, and the overall lamination packing density is typically limited by various fabrication constraints.

Consider a laminated core and an unlaminated core subjected to a uniform, time-varying magnetic field, $H_z = H_0\,\mathrm{e}^{\mathrm{j}\omega t}$, as shown in figure 1. The laminated core, with laminations of $w_{\mathrm{lam}} \ll h$, has lower eddy current losses, but with a smaller total core volume due to the wasted space

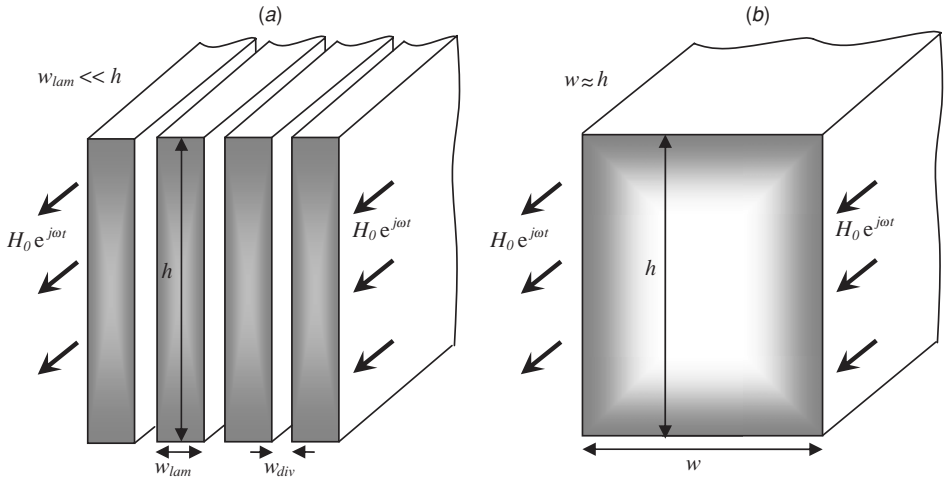

Figure 1. Schematic diagram of (*a*) low-loss laminated core and (*b*) lossy unlaminated core (magnetic flux density depicted by shading).

of the dielectric dividers (poor lamination packing density). This introduces a key design challenge: for a given operating frequency, determine the optimal lamination width based on certain fabrication constraints.

In a previous paper [8], a fabrication method was reported for incorporating vertically oriented, through-wafer, laminated magnetic cores within the thickness of a silicon wafer. This paper introduces a second, alternative fabrication method for achieving similar lamination structures. Then, based on specific fabrication constraints, a theoretical framework is developed to permit the design of an optimal lamination scheme for a particular application. As an example, the analysis is applied to the optimization of laminations for a miniaturized synchronous permanent magnet (PM) motor/generator.

2. Performance metrics for laminated cores

A laminated core typically consists of alternating layers of magnetic laminations and dielectric dividers of various widths, as shown in figure 1(*a*). One important scale-length for the analysis is the magnetic skin depth, δ, defined as

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{1}{\pi f \mu\sigma}}, \tag{1}$$

where $\omega = 2\pi f$ is the frequency of the time-varying magnetic field, and μ and σ are the magnetic permeability and conductivity, respectively, of the magnetic material. The skin depth is related to the depth of penetration of the imposed magnetic field. Using the skin depth as a benchmark length scale, several metrics are defined to enable the comparison of various cores.

2.1. Packing density

The packing density, α, is defined as the ratio between the magnetic cross-sectional area, A_{magnetic}, and the total cross-sectional area, A_{total}, of the core. For a typical core with many alternating magnetic and dielectric layers

$$\alpha = \frac{A_{\text{magnetic}}}{A_{\text{total}}} = \frac{w_{\text{lam}}}{w_{\text{lam}} + w_{\text{div}}}, \tag{2}$$

where w_{lam} is the magnetic lamination width and w_{div} is the divider width. Equation (2) can be written in terms of non-dimensional parameters,

$$\alpha(n, m) = \frac{w_{\text{lam}}/\delta}{w_{\text{lam}}/\delta + w_{\text{div}}/\delta} = \frac{n}{n+m}, \tag{3}$$

where n, defined as the lamination ratio, is

$$n = \frac{w_{\text{lam}}}{\delta} \tag{4}$$

and m, defined as the divider ratio, is

$$m = \frac{w_{\text{div}}}{\delta}. \tag{5}$$

2.2. Lamination efficiency

The total flux through a single lamination of width, w_{lam}, and height, h, is given by (see appendix),

$$|\phi| = w_{\text{lam}} h \mu H_0 \frac{\sqrt{2}}{n} \sqrt{\frac{\cosh n - \cos n}{\cosh n + \cos n}}. \tag{6}$$

Ignoring eddy current effects ($n \to 0$), this reduces to,

$$\phi_0 = w_{\text{lam}} h \mu H_0, \tag{7}$$

which is simply the lamination cross-section multiplied by the magnetic flux density at the wall. Thus, the lamination efficiency for a single lamination, β, is defined as the ratio of the actual flux divided by the flux capacity,

$$\beta(n) = \frac{|\phi|}{\phi_0} = \frac{\sqrt{2}}{n} \sqrt{\frac{\cosh n - \cos n}{\cosh n + \cos n}}. \tag{8}$$

2.3. Total core efficiency

From an engineering perspective, both packing density and eddy currents limit the total flux that can be passed through a physical core volume. The packing density captures the relative physical volume loss due to the inclusion of laminations, while the lamination efficiency represents an effective frequency-dependent volume loss. The combined effect can be captured by defining a total core efficiency, η, where

$$\eta(n, m) = \alpha(n, m)\beta(n). \tag{9}$$

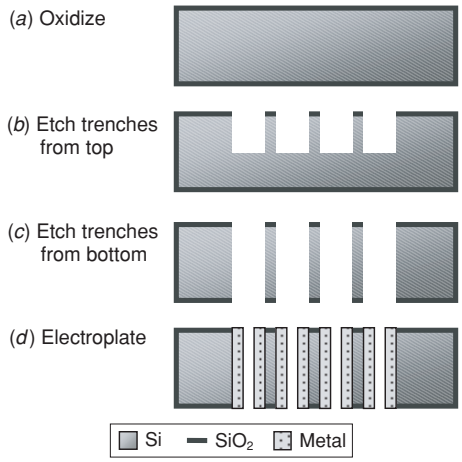

Figure 2. Process flow for vertically oriented, through-wafer, laminated magnetic cores in silicon using the partially filled trench method.

The total core efficiency can be interpreted as the percentage of 'useful' flux-carrying volume within the total volume occupied by the laminated, lossy core, as compared to a lossless, unlaminated core occupying the same volume.

Since power in a magnetic device is related to the square of flux, the lamination scheme should be designed such that the total core efficiency is maximized. In a microfabricated system, this requires careful optimization because of the microfabrication limitations on the geometries of the laminations and dielectric lamination dividers.

3. Fabrication methods

Two fabrication methods are described here to achieve vertically oriented, through-wafer, laminated magnetic cores. For the purposes of this paper, fabrication constraints are discussed based on direct experimental experience using current micromachining techniques on 100 mm diameter, 500 μm thick wafers.

3.1. Partially filled trench method

The first fabrication method [8] relies on direct electroplating onto the sidewalls of etched silicon trenches, as shown in figure 2. The fabrication process uses low-resistivity ($\rho = 0.001\ \Omega$ cm, $\sigma = 10^5$ S m^{-1}) silicon wafers. First, a 200 nm dry thermal oxide is grown, which later prevents electrodeposition on the top and bottom wafer surfaces (figure 2(*a*)). Next, photoresist is patterned as a mask for etching trenches in the oxide and silicon using deep reactive ion etching (DRIE). The through-etch is achieved by etching half way from the top of the wafer (figure 2(*b*)) and then repatterning and etching the remainder from the bottom side (figure 2(*c*)).

The photoresist is then stripped, and the wafer was cleaned in 'piranha etch' (3:1 H_2SO_4:H_20_2, 120 °C) for 10 min. A brief HF dip is used to remove the native oxide on the silicon sidewalls immediately before electroplating. A standard electroplating bath is used, with the low-resistivity silicon providing a conduction path for electrodeposition. The magnetic material is deposited only on the etched silicon sidewalls to a thickness such that an air gap remains between adjacent laminations (figure 2(*d*)).

For a wafer thickness of ~500 μm, the silicon divider width, w_{div}, is limited to ~20 μm (assuming a maximum etch aspect ratio of 25:1) by deep silicon etching technology. Reliably creating smaller Si dividers presents a substantial fabrication challenge (particularly when front-to-back alignment is used to etch from both sides). The air gap, w_{air}, is limited by electrodeposition non-uniformities caused by current crowding effects and restricted ion transport as the gap between the advancing plated layers is reduced [8]. This results in a tendency for the trench to 'pinch' or 'key-hole', leaving a void in the center region. To avoid pinching and to maintain reasonable uniformity (without bath additives), it was found that plating should be stopped when the laminations filled 2/3 of the trench width. Thus, for maximum packing density, the air gap is approximately equal to the lamination thickness ($w_{\text{air}} \approx w_{\text{lam}}$).

3.2. Fully filled trench method

The second method takes a more conventional approach, previously demonstrated for through-wafer electrical vias [9]. Oxidized silicon is used as a mold, and magnetic material is electroplated up from a seed wafer, which is temporarily bonded to the substrate, as shown in figure 3.

Using a standard silicon wafer, the fabrication process begins with by through-etching the lamination structures. For this step, etching can be performed from one or both sides, typically using either photoresist or silicon dioxide as a mask. After etching the trenches, a 1 μm wet oxide is grown to dielectrically isolate all surfaces, including the sidewalls, of the silicon (figure 3(*a*)).

Next, a separate 'seed wafer' with a sputtered Ti (20 nm)/Cu (200 nm) seed layer is bonded to the etched wafer. This can be achieved either by mechanically clamping the two wafers together or using a positive-tone photoresist as a photodefinable bonding layer. To use the photoresist, a thin layer is spun, and the wafers are pressed together and baked (figure 3(*b*)). The resist is then exposed and developed using the through-etched wafer as mask, selectively opening contacts to the seed layer (figure 3(*c*)).

A standard electrodeposition bath is then used to electroplate material up in the trenches (figure 3(*d*)). Once finished plating, the photoresist bonding layer is dissolved using a solvent (figure 3(*e*)), and a selective Cu etch is used to undercut the electroplated structures, releasing the plated wafer from the seed wafer (figure 3(*f*)). Any protrusions of metal can be polished (e.g. using chemical mechanical polishing) down flush to the surface if needed.

For this method, the magnetic laminations take the same form factor as the etched silicon trenches. Thus, the minimum lamination width is limited by the silicon etching technology. Using the same figure of merit from above this yields a minimum lamination width for a 500 μm thick wafer of ~20 μm (again, assuming a maximum etch aspect ratio of 25:1). The minimum silicon divider widths are also assumed to be ~20 μm.

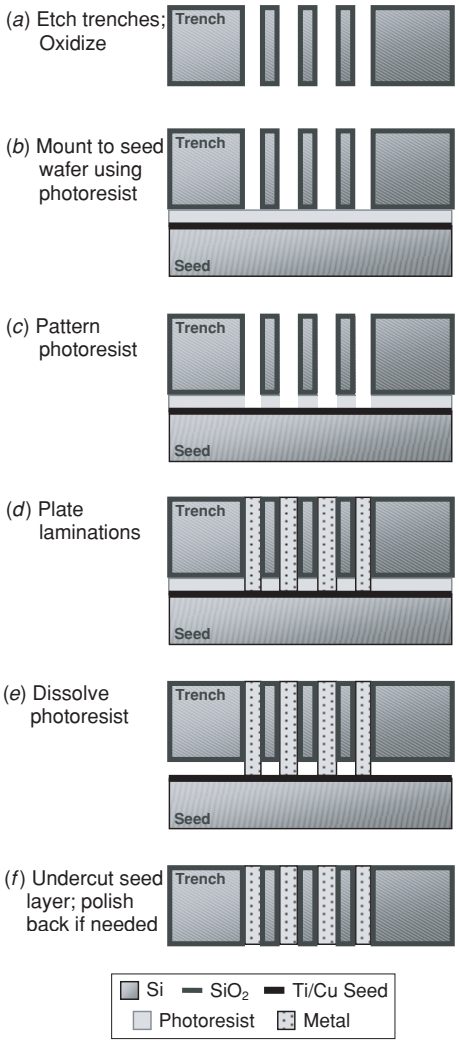

Figure 3. Process flow for vertically oriented, through-wafer, laminated magnetic cores in silicon using the fully filled trench method.

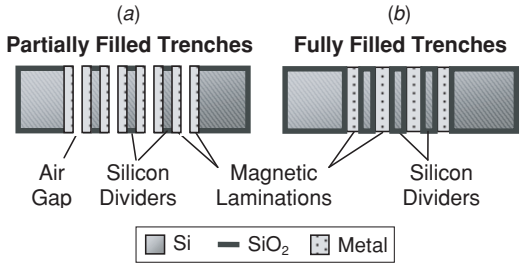

Figure 4. Schematic of vertically oriented, through-wafer magnetic laminations in silicon achieved using (*a*) partially filled trench method and (*b*) fully filled trench method.

4. Comparison of partially filled versus fully filled trench laminations

As depicted in figure 4(*a*), the partially filled trenches result in a structure with a repetitive lamination pattern of magnet—silicon—magnet–air. The packing density for this configuration is given by

$$\alpha_1 = \frac{2w_{\text{lam}}}{2w_{\text{lam}} + w_{\text{air}} + w_{\text{div}}}, \tag{10}$$

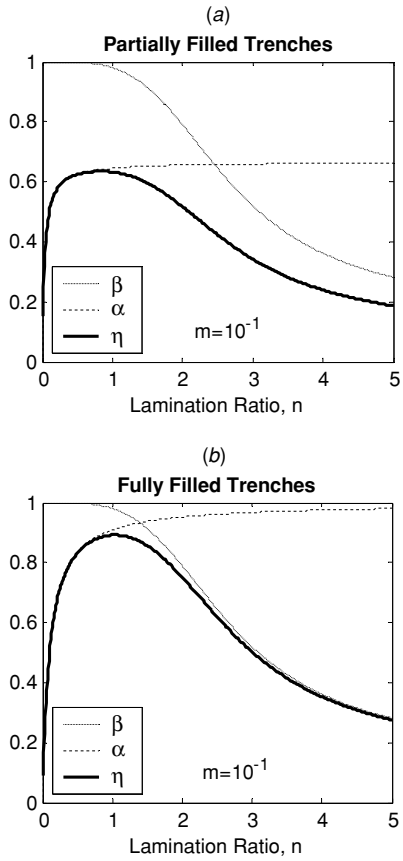

Figure 5. Efficiencies for (*a*) partially and (*b*) fully filled trenches: packing density, α, magnetic flux efficiency, β, and total core efficiency, η, for divider ratio $m = 0.1$. (Note: $n = w_{\text{lam}}/\delta$ and $m = w_{\text{div}}/\delta$).

where w_{lam} is the width of the magnetic lamination, w_{div} is the width of the silicon divider, and w_{air} is the width of the resulting air gap. Using the fabrication constraint of $w_{\text{air}} = w_{\text{lam}}$, the packing density reduces to

$$\alpha_1 = \frac{2w_{\text{lam}}}{3w_{\text{lam}} + w_{\text{div}}} = \frac{2n}{3n + m}, \tag{11}$$

where $n = w_{\text{lam}}/\delta$ and $m = w_{\text{div}}/\delta$. For this lamination scheme, the packing density asymptotes to only $2/3$, even as the silicon divider width goes to zero ($m \to 0$), due to the limiting constraint of the interlamination air gap.

Conversely, the fully filled trenches result in a repetitive lamination structure of magnet–silicon, as shown in figure 4(*b*). The packing density for this configuration is

$$\alpha_2 = \frac{w_{\text{lam}}}{w_{\text{lam}} + w_{\text{div}}} = \frac{n}{n + m}, \tag{12}$$

Here, as the divider width goes to zero ($m \to 0$), the packing density asymptotes to 1. However, for either partially or fully filled trenches, the minimum divider width is a function of the silicon etching precision, and m can be quite large, depending on the skin depth.

Using equations (8), (9), (11) and (12), the lamination efficiency, flux efficiency, and total core efficiency were calculated as a function of the lamination ratio, as shown in figure 5. As can be seen, there is an optimal lamination thickness to maximize the core efficiency. Very

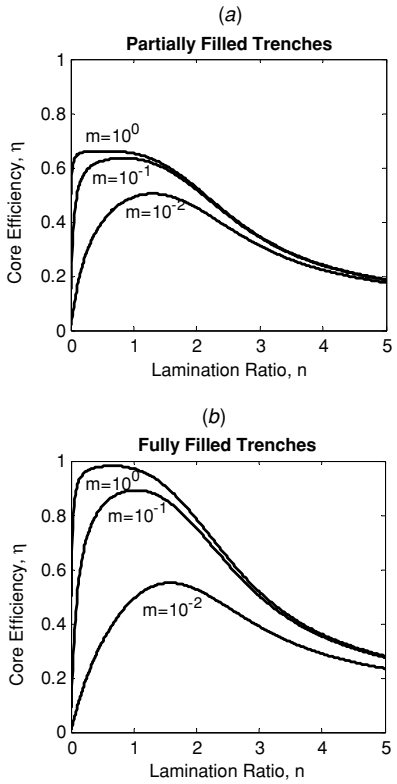

Figure 6. Total core efficiency, η, for (*a*) partially and (*b*) fully filled trenches for various divider ratios, m. (Note $n = w_{\text{lam}}/\delta$ and $m = w_{\text{div}}/\delta$).

thin laminations have low packing density, but very thick laminations have large eddy current losses. These plots are for a fixed divider ratio of $m = 0.1$. Figure 6 shows the dependence of the total core efficiency on silicon divider width; smaller silicon dividers result in higher packing densities and thus higher overall efficiency.

Both the partially and fully filled trench methods offer solutions for achieving high-aspect-ratio, vertically oriented, through-wafer laminated magnetic cores in silicon. However, there are clearly some advantages and disadvantages to each technique. The partially filled trench method offers lower core efficiencies, but can achieve finer laminations. Also, the 'sidewall-in' plating scheme requires minimal plating time. The fully filled trench method offers higher packing densities, but the minimum lamination width is limited by the minimum achievable trench ($\sim$20 μm in a 500 μm thick wafer). Also, this 'bottom-up' method takes significantly more plating time. A summary comparison of the two methods is shown in table 1.

Table 1. Comparison of two fabrication methods for achieving through-wafer, laminated magnetic cores in silicon.

Parameter	Partially filled	Fully filled
Lamination range	<1 μm–500 μm	20 μm–2000 μm
Maximum theoretical core efficiency ($m = 0$)	67%	100%
Limiting fabrication constraints	$w_{\text{div}} > 20$ μm $w_{\text{lam}} = w_{\text{air}}$	$w_{\text{div}} > 20$ μm $w_{\text{lam}} > 20$ μm
Plating time	Hours	Tens of hours
Advantages	Simple fab, better for smaller laminations	Higher packing density, better for larger laminations

5. Example: optimal laminations for synchronous magnetic machines

The theoretical analysis discussed in section 4 is applied to the design of a synchronous PM machine [10]. The machine operates using an eight-pole annular PM rotor to provide a time-varying flux to coils patterned on the surface of a ferromagnetic stator substrate. The time-varying fields from the spinning rotor result in large eddy current losses in the case of an unlaminated, high-conductivity ferromagnetic stator. To reduce the eddy current losses, this substrate should be replaced with a laminated, annular ferromagnetic stator core, achievable in silicon using either the fully or partially filled trench methods.

The skin depth, given by equation (1), depends on the electrical operating frequency and material properties. For a synchronous machine, the electrical operating frequency, $\omega_{\text{e}} = 2\pi f_{\text{e}}$, is directly related to the mechanical radial speed, ω_{m}, by the number of poles, p, [11]

$$\omega_{\text{e}} = \frac{p}{2}\omega_{\text{m}}. \tag{13}$$

Thus, the machine, having eight magnetic poles, has an electrical operating frequency four times faster than the mechanical speed. For these calculations, constant values of $\mu_r = 1000$, and $\rho = 50$ $\mu\Omega$ cm ($\sigma = 2 \times 10^6$ S m^{-1}) are used to approximate the properties of electroplated FeCoNi, a high-saturation, ferromagnetic material [12]. The previously discussed fabrication constraint of a minimum lamination divider width of 20 μm is also assumed.

The optimum lamination width, skin depth, and total core efficiencies are computed at various synchronous operating speeds up to 1 Mrpm ($f_{\text{e}} = 66.7$ kHz). The results are plotted in figure 7. At 1 Mrpm, the skin depth is 44 μm. The partially filled method has an estimated total core efficiency of 57% for 49 μm laminations, while the fully filled predicts 70% for 60 μm laminations. As expected, the partially filled method requires finer laminations because it has a poorer packing density. It is interesting to note that at 1 Mrpm, the optimal lamination widths for both methods are larger than the skin depth. This is a consequence of the limited packing densities achievable using these microfabrication methods.

It should be noted that while there would also be magnetic loss in the silicon divider structures, the loss would be much smaller than in the magnetic laminations. Even if using highly conductive silicon (as in the case of the partially filled trench method), the conductivity of silicon is $\sim$10 times smaller and the permeability is $\sim$1000 times smaller than the magnetic lamination. Thus, according to equation (1), the skin depth for silicon is at least 100 times larger than the magnetic lamination at any given frequency. Also, in any practical design, the silicon dividers would be thinner than the magnetic laminations. For these reasons, the magnetic loss in the silicon is typically ignored.

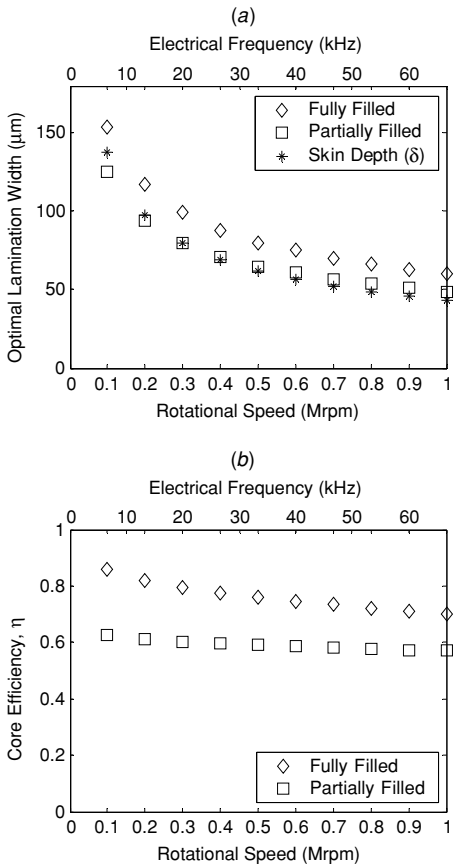

Figure 7. (*a*) Optimal lamination thickness and total core efficiency (*b*) for proposed magnetic machines, assuming $w_{\text{div}} = 20\ \mu$m, $\mu_r = 1000$, $\rho = 50\ \mu\Omega$ cm.

As for implementing either of these designs, there are several additional factors to consider. The fully filled method would require silicon through-etches of 49 μm ($w_{\text{etch}} = w_{\text{lam}}$), whereas the partially filled method requires only 180 μm wide silicon etches ($w_{\text{etch}} = 3 \times w_{\text{lam}}$), which are much easier to fabricate. Also, in this case, the fully filled method offers only a modest improvement in flux efficiency with the drawback of much longer deposition times. For these reasons, the partially filled method would be preferred.

6. Conclusions

This paper describes and comparatively analyzes two fabrication methods—partially filled and fully filled trenches—for achieving vertically oriented, through-wafer, laminated magnetic cores in silicon. A theoretical framework was developed to maximize the flux through a laminated core under the constraints of packing density and magnetic eddy current loss. This analysis was applied to the design of a laminated magnetic core for a synchronous PM machine. Optimal lamination thicknesses were calculated for various operating speeds. This example demonstrates how the analysis can be applied to practical applications and also illustrates some of the design tradeoffs for microfabricated laminated magnetic cores.

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Appendix. Magnetic diffusion in a single lamination

In order to facilitate understanding of the optimization analysis, the case of magnetic diffusion in a single infinite lamination is reviewed, following the theoretical treatments found in [6, 13]. Consider a single magnetic lamination with height, h, much larger than the width $w_{\text{lam}} = 2b$ and with infinite extent in the z-direction, as shown in figure 8.

Under the influence of a uniform, z-directed magnetic field, $\text{Re}[H_0\, e^{j\omega t}]$, at sinusoidal steady state with angular frequency ω, the field within the lamination is governed by a 1D magnetic diffusion equation,

$$\frac{\partial^2 H_z}{\partial x^2} = \mu\sigma \frac{\partial H_z}{\partial t}, \tag{A1}$$

where μ and σ are constants of permeability and conductivity for the magnetic lamination, respectively. Phasor solutions for the magnetic field, $H_z(x,t)$, magnetic flux density, $B_z(x,t)$, current density, $J_y(x,t)$, can thus be derived [6,13]:

$$H_z(x,t) = \text{Re}[\tilde{H}_z(x)\, e^{j\omega t}] \qquad \tilde{H}_z(x) = H_0 \frac{\cosh(kx)}{\cosh(kb)}, \tag{A2}$$

$$B_z(x,t) = \text{Re}[\tilde{B}_z(x)\, e^{j\omega t}] \qquad \tilde{B}_z(x) = \mu H_0 \frac{\cosh(kx)}{\cosh(kb)}, \tag{A3}$$

$$J_y(x,t) = \text{Re}[\tilde{J}_y(x)\, e^{j\omega t}] \qquad \tilde{J}_y(x) = -kH_0 \frac{\sinh(kx)}{\cosh(kb)}, \tag{A4}$$

where

$$k = \pm\frac{1+j}{\delta} \tag{A5}$$

and δ is the magnetic skin depth, defined as

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{1}{\pi f\mu\sigma}}. \tag{A6}$$

Figure 9 shows the magnetic flux density (normalized by the value at the wall) and relative current density across the thickness of the lamination for various values of the skin depth, δ. The smaller the skin depth (relative to the lamination width), the smaller the penetration depth of the magnetic wave. When the skin depth is much smaller than the lamination width, the flux in the center region of the lamination is nearly zero, and corresponding high current densities (eddy currents) are noted near the surfaces. This results in a dramatic reduction in the flux-carrying capacity of the lamination.

Furthermore, the flux can be obtained by integrating the magnetic flux density across the thickness of the lamination,

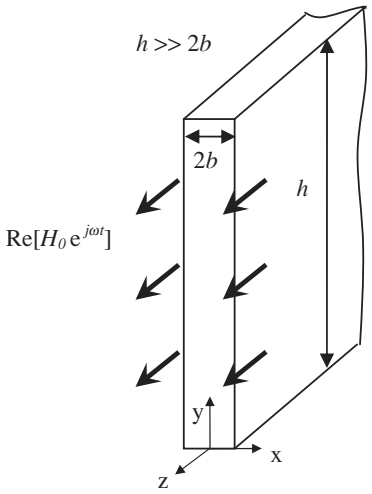

Figure 8. Schematic of infinitely long lamination of width $2b$ and height h, bounded on both sides by a uniform field of $\mathrm{Re}[H_0\,\mathrm{e}^{\mathrm{j}\omega t}]$.

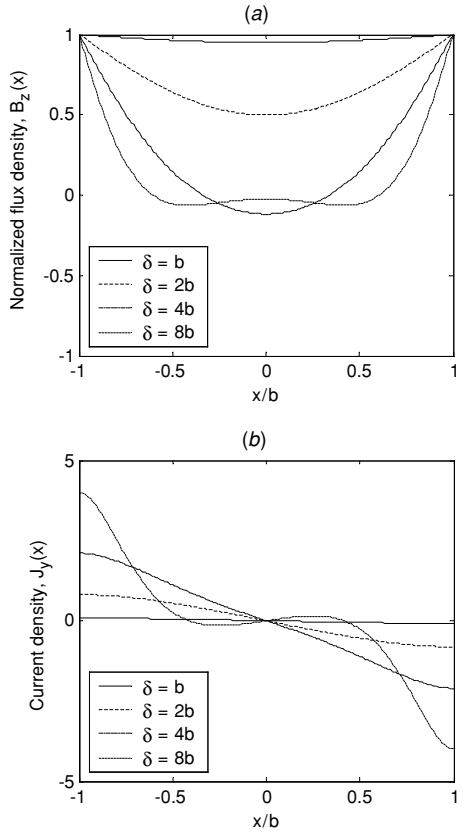

Figure 9. Normalized magnetic flux density, B_z, and current density, J_y, plotted as a function of the lamination width for various values of the skin depth, δ.

$$\phi(t) = \mathrm{Re}[\tilde{\phi}\,\mathrm{e}^{\mathrm{j}\omega t}] \quad \tilde{\phi} = h\int_{-b}^{b}\tilde{B}_z(x)\,\mathrm{d}x = 2bh\mu H_0\frac{\tanh(kb)}{kb}. \tag{A7}$$

Substituting for k from equation (A5) and making use of the identity

$$\tanh\left(\frac{x+jy}{2}\right) = \frac{\sinh x + j\sin y}{\cosh x + \cos y}, \tag{A8}$$

it can be shown that

$$|\phi(t)| = |\tilde{\phi}| = w_{\mathrm{lam}}h\mu H_0\frac{\sqrt{2}}{n}\sqrt{\frac{\cosh n - \cos n}{\cosh n + \cos n}}, \tag{A9}$$

where

$$n = \frac{2b}{\delta} = \frac{w_{\mathrm{lam}}}{\delta}. \tag{A10}$$

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