A Micromachined Chip-to-Board Interconnect System Using Electroplating Bonding Technology

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***Abstract*—We demonstrate a micromachined flexible chip-to-board chip interconnect structure for a chip scale package. Micromachined flexible interconnects enable robust operation in high thermal cycling environments, even for high pinout chips due to the flexible interconnect ability to absorb thermal expansion strain. The interconnects on the chip-side and printed wiring board (PWB)-side are united by electroplating bonding technology, a direct bonding technology resulting in solder-free, underfill-free, low temperature joining by means of copper (Cu) electroplating. Over 200 surface micromachined interconnects, which have a thermal relief geometry, are radially arranged on 1×1 cm^2 substrates. A chip surrogate consisting of glass with integrated platinum (Pt) microheaters mimics a real electronic device under varying thermal loads. The integrated microheaters can simultaneously test mechanical and electrical performance of the interconnects by generation of on-chip temperatures up to 150°C. Lateral and vertical displacement of the interconnects in the thermal environment are measured and simulated. A mechanical reliability test of the chip scale package is successfully performed for 5000 cycles with thermal cycles of 5 min between 40 °C to 147°C. No failures were observed during this period.**

***Index Terms*—Electroplating bonding technology, flexible interconnects, microheater, micromachined, thermal cycling.**

I. Introduction

IN ADVANCED electronic systems, chip packaging must satisfy requirements such as low cost and compactness [1]–[7]. Flip chip technology has received much attention for chip to package interconnection due to its good electrical performance, compactness, and high input/output (I/O) density [8], [9]. The excellent performance of the packaging can be obtained by direct solder bumping bridging the gap between silicon die and the printed wiring board (PWB). However, the mechanical and thermal characteristics of flip chip packaging may suffer from issues related to the thermal mismatch of substrates, polymer underfill, and the environmentally harmful solder bump [10]–[12]. The thermal mismatch is generated by difference of coefficients of thermal expansion (CTE) of the substrates when the system is operating and generating heat. This problem becomes more acute as die sizes increase. The thermal mismatch of substrates introduces mechanical stress on the ductile solder bump itself or its interface of solder bump and I/O pads. To decrease the thermal stress on the interconnect, a polymer underfill is typically dispensed into the interconnect layer. However, the polymer dispensing process requires additional processing steps [13], particularly in high performance systems with high I/O density.

The above-mentioned environmental and processing concerns have stimulated alternative approaches [14]–[16], such as conductive adhesives, although they have relatively high electrical resistivity. An attractive alternative to both solder and conductive adhesives that does not compromise conductivity or mechanical strength is to connect the chip to the substrate by electroplated metal such as electroplated copper, which provides high electrical and thermal conductivity.

In addition, the interconnects can also serve as probes for electrical connectivity and burn-in testing. Several groups have done this type of study using micromachined structures for probing purposes [17]–[19]. Micromachining approaches are advantageous because of low cost due to batch processing, better electrical performance and higher density. Micromachined spring-like structures can be designed with a high degree of vertical flexibility. This can help compensate for large variations in the height of the interconnects as well as any surface roughness of the substrate wafer during wafer level electrical and burn-in testing.

In this paper, a flexible and robust electroplating bonded chip interconnect system is demonstrated. The chip interconnect system is formed by micromachining and electroplating bonding. The S-shaped interconnect structures are radially arranged to obtain a flexible vertical and horizontal movement under thermal loads. Five microheaters are embedded in the system to apply heat to the system in a manner representative of actual application (i.e., hot chip on cooler PWB), thereby forming a microsystem that mimics real-world application.

II. Design Rules

Fig. 1 shows a schematic of the microheater embedded electroplating bonded flexible interconnect system. A glass die, integrated with microheaters, is used to simulate an operating silicon chip. This chip is attached to a printed wiring board with prefabricated flexible interconnect, then electroplating bonding is accomplished by flipping an upper substrate (glass) over a bottom substrate (PWB), clamping the substrates together, and electrodepositing Cu on interconnect junction between both substrates. The electroplating bonding is performed at room temperature and in aqueous plating solution. These bonding

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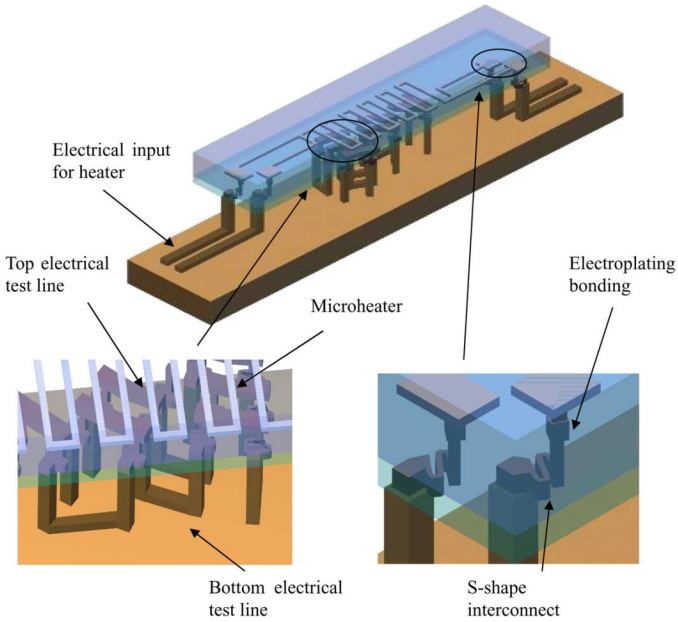


Fig. 1. Schematic of microheater embedded electroplating bonded flexible interconnect system.

conditions result in a low stress process and their batch nature has the potential for cost effectiveness.

Five Pt thin-film microheaters designed to mimic an operating silicon chip are embedded in a silicon dioxide layer on a glass chip substrate. The silicon dioxide, which is commonly deposited as a passivation layer on the chips, is layered on the substrate and microheaters to provide electrical isolation between the heaters and the flexible chip interconnect structures. As a prerequisite for heater operation, electrical connections from the current source to the microheaters must be designed because it is difficult for external wire connections to access the flipped heater pads. Thus, the electrical feeds for the heaters must originate from the substrate itself, which also is the manner in which electrical power would be supplied in actual application. For operating the five heaters, 20 electrical input paths, which include 10 voltage measurement-pads and 10 current source pads for resistance measurements, are electroplating bonded with the chip interconnects. The 216 chip interconnects comprising 196 chip interconnects and 20 microheater interconnects are radially placed on the 1×1 cm^2 substrates. The chip interconnects are comprised of vertically and horizontally flexible "S-shaped" structures intended to allow relief of coefficient of thermal expansion-related strain, as well as achieving a sufficient vertical displacement for reliable electrical contact during burn-in. The flexible interconnects have four metal parts: 1) electrical test lines for measuring electrical connectivity, 2) first posts for supporting S-shaped beam structures, 3) S-shape metal structures for achieving freely moving in any direction, and 4) second metal posts for bonding with the board using electroplating bonding. The configuration of the electrical test lines of the system is divided into four sectors. A sector is created with connections of 49 electroplating bonded interconnects and the four sectors are electrically connected with each other. If an interconnect between posts on the both substrates has electrically or mechanically disconnected by poor bonding quality or by thermally-induced mechanical failure, this sector approach can help pinout the discontinuity location.

III. Fabrication

A 2.5 cm $\times$ 2.5 cm glass (as a chip analog) and a 5 cm $\times$ 5 cm PWB substrate are utilized for the electroplating bonded chip interconnect system. Formation of the overall system is explained by four fabrication sequences: 1) microheater and electrical test line, 2) flexible interconnects, 3) electrical input structures and high aspect ratio interconnect, and 4) electroplating bonding. The microheater, electrical connection and flexible interconnects are formed on the glass, or "top" substrate. The other structures including electrical source input pad, tall interconnects, and electrical connectivity test pads are fabricated on the PWB, or "bottom" substrate.

A. Fabrication of Microheater and Electrical Connection Structures

Fig. 2(a) illustrates the fabrication process of the microheater and its associated electrical connection structures. The microheaters are fabricated on the top substrate using a liftoff process. The glass substrate is cleaned using a piranha clean (H_2SO_4: $H_2O_2 = 3:1$) to enhance adhesion between the substrate and subsequently deposited films. A 7-μm-thick NR9-8000 negative photoresist is spun on the substrate and the heater mold is developed. A thin film of 100 Å Cr/ 1000 Å Pt is evaporated on the mold and PR. After metal evaporation, the photoresist layer is removed by acetone with ultrasonic agitation. The resultant microheater is encapsulated by a 2-μm silicon dioxide layer (SiO_2) using PECVD. The SiO_2 films are patterned by using reactive ion etching (RIE) to form heater contacts. Then, a thin film (Cr/Cu/Cr) layer is deposited to make electrical connection to the heater. The connections are formed by photolithography and Cu electroplating. Fig. 3(a) shows a photograph of fabricated microheaters on the top substrate. Five microheaters are fabricated on a single chip. To understand the heater placement, the left-most heater is designated heater number 1 and the right-most is designated heater number 5.

B. Fabrication of Flexible Interconnects

Fig. 2(b) shows a fabrication procedure illustrating this process and photographs of fabricated flexible interconnects with microheaters on the upper substrate are shown in Fig. 3(b). A seed layer (Cr/Cu/Cr) for electrodeposition of the electrical test lines is deposited and lithographically patterned so as to electrically connect with the previously-fabricated heater structures. NR8-9000 negative photoresist is spun and patterned as an electroplating mold, and 10-μm-thick Cu structures are electrodeposited to form the electrical test lines. In selected areas on top of the electrical lines, 100 μm $\times$ 100 μm $\times$ 40 μm first posts are formed with SU-8 negative photoresist and electroplating. Another seed layer is then sputtered for the flexible interconnect beam structure and patterned for good mechanical and electrical connection between the first post and the beam structures, and 15-μm beam structures are fabricated using Cu electroplating. After removal of the photoresist for the

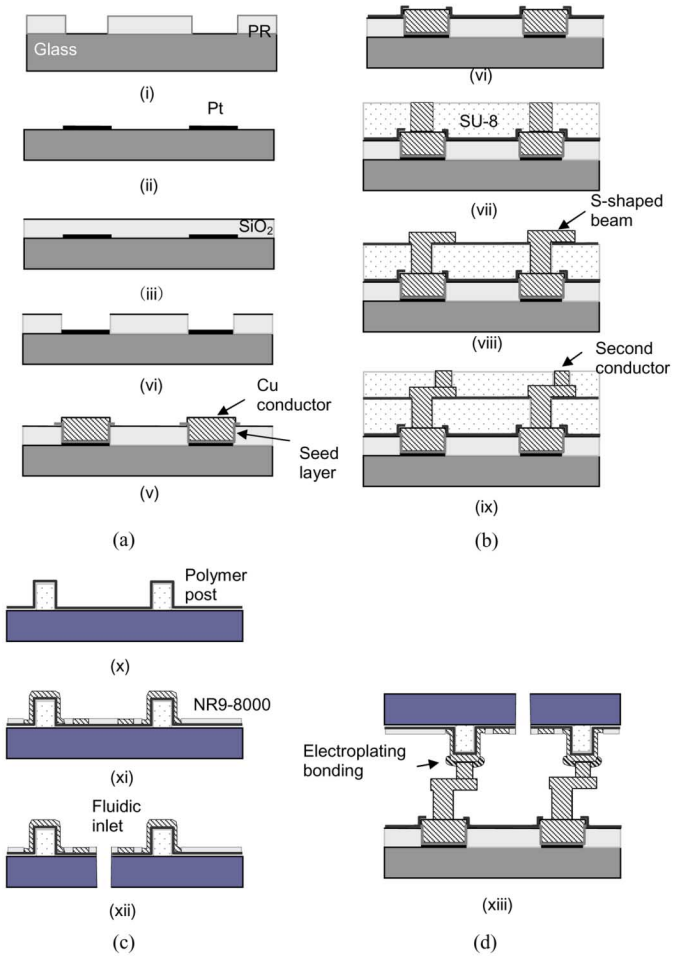


Fig. 2. Fabrication sequence for the system. (a) microheater, (b) S-shape flexible interconnects, (c) bottom interconnects structure, and (d) electroplating bonding.

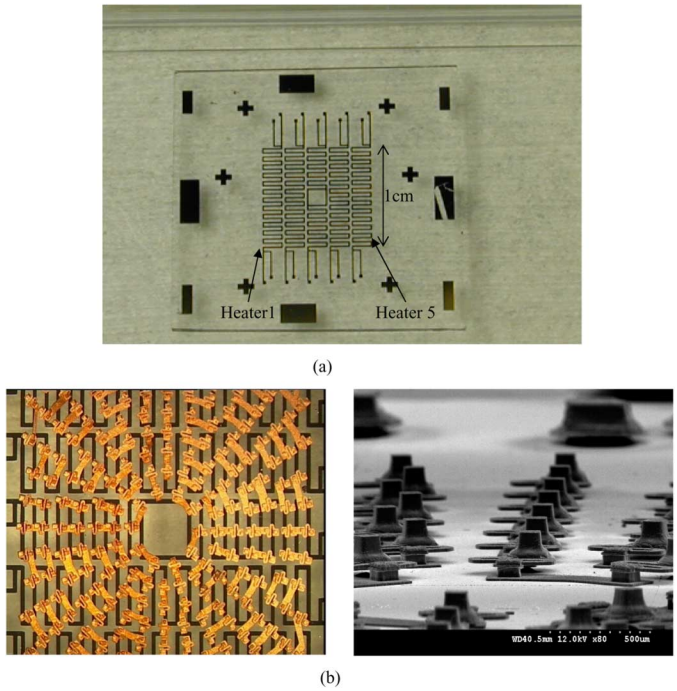


Fig. 3. Photographs of the fabricated structures: (a) microheater and (b) S-shaped flexible interconnects.

beam structures, 150 μm $\times$ 150 μm $\times$ 95 μm second posts are formed with SU-8 and Cu electroplating that will ultimately be used for mechanical contact with the bottom substrate during electroplating bonding. After formation of all structures, the SU-8 molds for post formation and seed layer are etched away by RIE and wet etching steps. After completion of the chip interconnect fabrication, a passivation polymer layer of thick (100 μm) NR9-8000 photoresist is deposited and patterned to hinder unwanted Cu-growth on the system during electroplating bonding. Fig. 3(b) shows fabricated S-shaped interconnects before the polymer layer covers the substrate and an (scanning electron microscope) SEM picture of the overhanging interconnect structures.

C. Fabrication of Bottom Electrical Test Lines, Electrical Input Structures and Bottom Interconnect Structure

The PWB substrate is prepared to mimic real chip packaging and to create a flow path for the plating solution for electroplating bonding of the chip interconnects, which facilitates uniform plating even in extremely high aspect ratio channels. Three functional structures are fabricated on the substrate; interconnect posts, electrical test lines, and heater operating electrical input structures. A polymer core post method [20] is used for the formation of 350 μm height interconnect posts designed for easier and faster electroplating bonding as illustrated in Fig. 2(c). SU-8 photosensitive epoxy, a-negative-working material, is used to easily fabricate high aspect ratio post performs. The posts are coated with metal layers (Ti/Cu/Ti) using dc sputtering for electrodeposition. The metal coated polymer structures are then covered and selectively patterned with negative NR9-8000 photoresist for electroplating of the electrical test lines, electrical input pads and interconnect structures. Then, the opened metal coated posts and the pads are electroplated with copper (Cu) or gold (Au). Patterning with negative photoresist offers the possibility of decreasing the number of mask processes required for the electrical connection line and heater electrical pads. After electroplating of the posts and pads, the electroplated metal posts and pads are covered with negative photoresist again. Fig. 2(c) shows the fabrication process.

D. Electroplating Bonding of Upper Structures and Bottom Structures

With the photoresist covered structures and substrates, preparation for electroplating bonding is deployed. First, a 1-mm-diameter hole is drilled in the center of the PWB substrate to form an electroplating solution flow channel. The channel circulates the electroplating solution to achieve uniform concentration of electroplating solution in the system [21]. The structures on both substrates are manually aligned, clamped together and electroplating bonded. After completion of the bonding, the seed layer deposited on bottom substrates for formation of the high polymer structures and pads should be etched away to achieve electrical isolation between the interconnects. Before the seed layer etching, the photoresist layer that covered

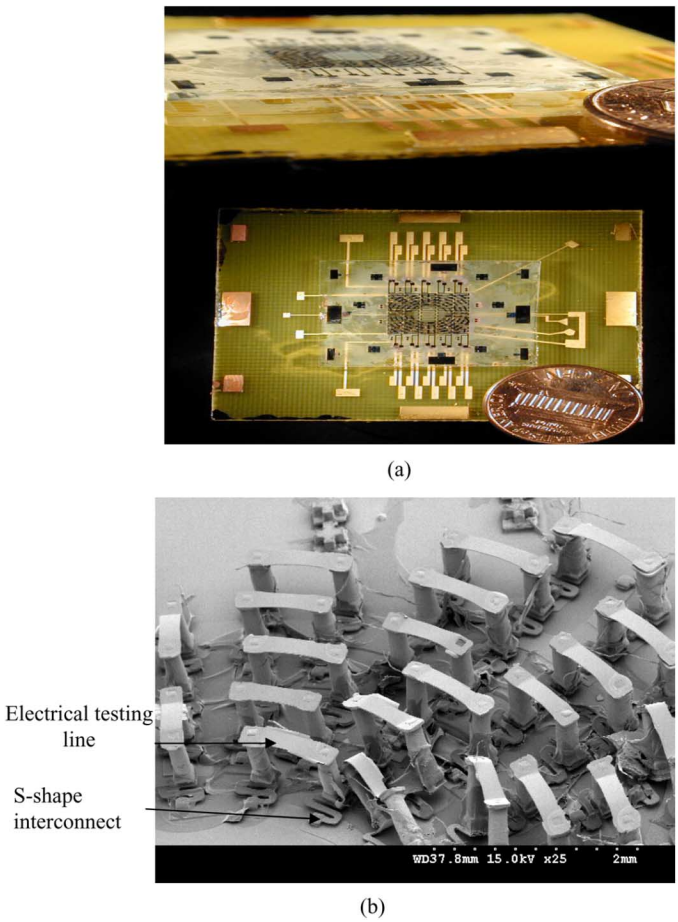


Fig. 4. Electroplating bonded interconnect system: (a) photograph of the electroplating bonded system and (b) SEM picture of system tested to destruction.

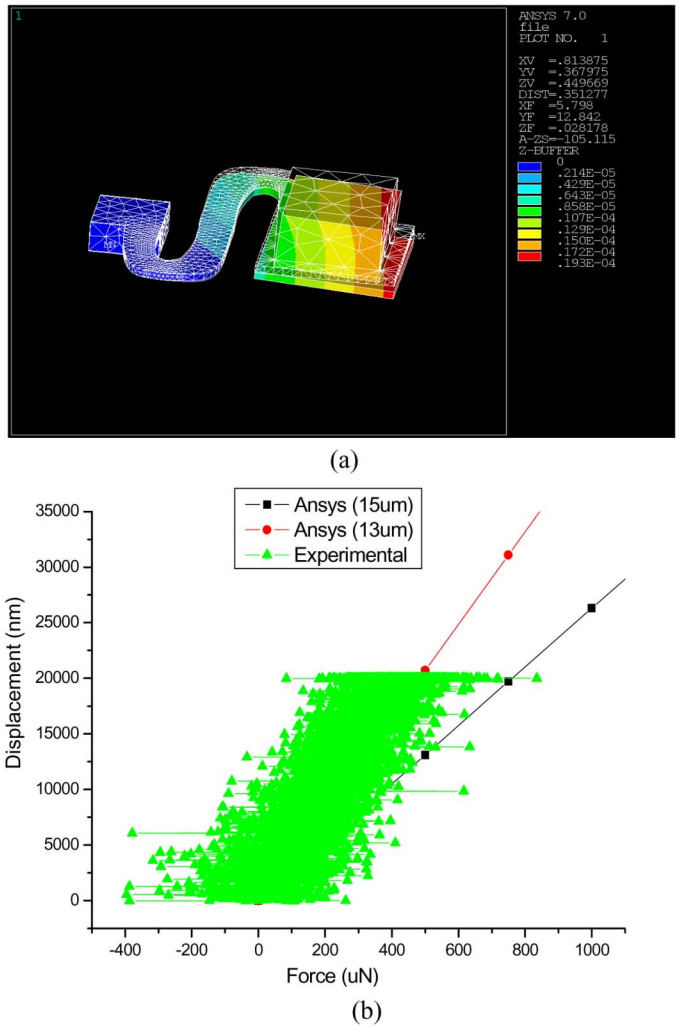


Fig. 5. Vertical displacement of the S-shaped interconnect (a) a figure of vertical displacement simulation and (b) comparison of simulation and measurement result of vertical deflection of S-shape interconnect.

the structures on upper and bottom substrates must be removed. The relatively thin photoresist layer on the bottom substrate is easily removed with acetone. The thicker (100 μm) NR9-8000 PR layer on the upper substrates is removed using an RR4 resist remover soak for 30 min, leaving the structure shown in Fig. 2(d). Fig. 4(a) shows the final electroplating bonded flexible chip interconnect system. After completion of the entire fabrication process, the electroplating bonded system is tested destructively by force to inspect the bonding status. Fig. 4(b) shows a posttesting SEM of the system. It is instructive to note that failure occurred on interfacial layer between the seed layer and the bottom substrate. This means that the electroplating bonded part of the structure has a strong mechanical connection.

IV. Characterization

A. *Characterization of Vertical Displacement of the Interconnects*

The extent of vertical movement of the flexible interconnect is a crucial parameter to compensate for nonuniformities of the interconnect height and the rough surface of the substrate during wafer level electrical and burn-in testing. The S-shaped interconnects as designed are simulated with the finite element method (FEM) simulation tool ANSYS, and the vertical displacement of fabricated interconnect is measured with a Hysitron TriboIndenter. For the simulation of the vertical movement of the interconnects, a nominal 15-μm thick beam structure is initially considered, resulting a 7 μm difference in its displacement when 0.5 mN force is applied. One potential reason for the dissimilarity is an inadequate measurement of the structural thickness, which strongly affects the structure compliance. Since contact surface profilometry cannot be used on these structures due to their compliance, the as-fabricated beam thickness is measured by a Wyko Noncontact Optical Profilometer and is found to be 13 μm. Another ANSYS simulation is done with a 13-μm thickness beam structure. During the simulation, the interconnect geometry for the simulation is imported from AUTOCAD with an SAT file to reduce the geometric distortion between the mask used in actual processing and the simulation. Fig. 5(a) shows the simulation result when 0.5 mN force is applied to a point on the second post. To overcome of the surface nonuniformity of the substrate, more than a 15 μm deflection is required for the vertical movement of the flexible interconnects [14], which is achieved. The result of the nanoindentor measurement shows a linearly proportional graph that implies linear elastic behavior for the flexible interconnect.

The comparison of simulation and measurement results is described in Fig. 5(b) and agrees well for a beam thickness of 13 μm.

B. Characterization of Microheater

After completion of the whole process for the chip package system, the characterization of the heater is performed to observe heater functionality and temperature distribution profile. The heater is operated by an electrical source that is applied through the electroplating bonded interconnects. The electroplating bonded system is also itself packaged by wirebonding to an external board for convenience as well as minimization of system damage during extensive testing, as shown in Fig. 6(a). A total of 28 wires are used, with the current source pads for the heater operation (10 wires), with voltage measurement pads for the heater (10 wires), and with the electrical connection testing pads (8 wires).

Typically, thermal reliability failure of the chip package is induced by the different coefficient of thermal expansion between the silicon substrate and PWB. Unlike a common thermal reliability testing chamber that is operated with uniform temperature in the whole chamber, the heater source is placed on the upper substrate in this system setup, i.e., the heat can be transferred to the PWB by heat conduction through the Cu interconnects from heater to the substrate in the same manner as in an actual application. So, it is necessary to observe the temperature profile of this system. In a typical test, one heater, e.g., heater number 2 in the position described Fig. 3(a), is operated. To obtain the temperature value generated by the microheaters, a thermocouple is attached on the backside surface of the glass substrate and a thermocouple is put into the gap of the substrates and attached to the bottom substrate. Both thermocouples are placed on the position of the heater number 1.

Fig. 6(b) shows the temperature comparison with the above test setup. The result comparison shows that the measurements had a 5 °C difference. It means that the generated heat seems to efficiently transfer to the PWB due to the relatively high thermal conductivity of the Cu interconnects. The heat profile is also utilized to determine appropriate boundary conditions in ANSYS simulations for the CTE-induced horizontal movement of the interconnect.

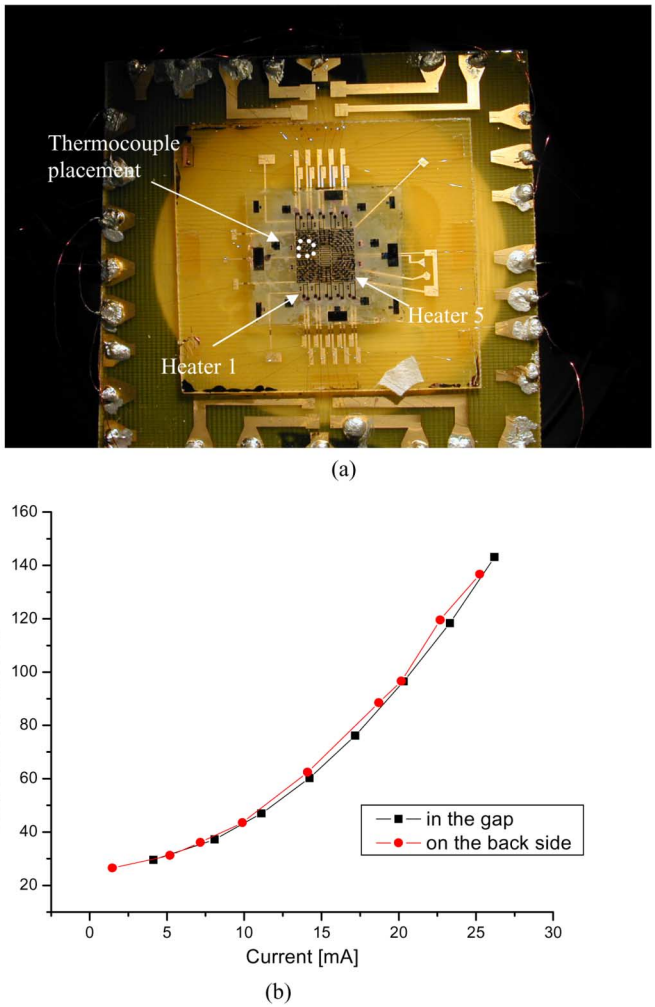


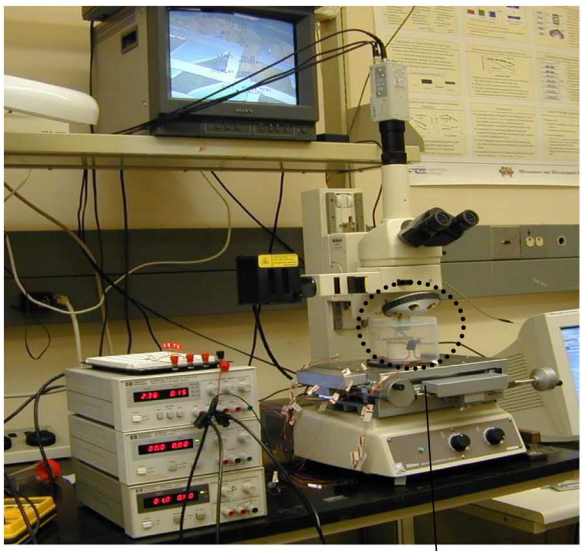
Fig. 6. Microheater characterization: (a) microheater operation setup and (b) comparison of temperature at different location with same applied current.

C. Characterization of Horizontal Movement of the Interconnects

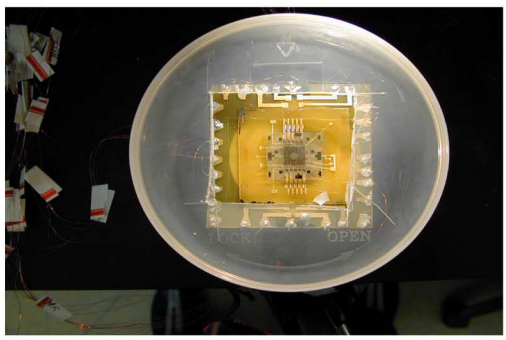
Thermal stress reduction is accomplished by fabricating a horizontally-compliant structure to allow for difference in the thermal expansion of the substrate and chip. The majority of chip packages are comprised of silicon chips and glass-fiber epoxy PWB. The temperature-displacement relation for chip packages can be expressed by (1), [22]

$$\delta = \Delta\mathbf{T}(\alpha_{\mathrm{PWB}} - \alpha_{\mathrm{Si}})\boldsymbol{L} \tag{1}$$

where δ is the displacement of the interconnect; α_{PWB} and α_{Si} are coefficients of thermal expansion in PWB and silicon substrates, respectively; ΔT is the temperature change of the system (i.e., difference between operating temperature and reference temperature, in this case, the reference temperature can be said as room temperature or as initial temperature of operation), and L is the radial distance from the center of the system. If the system is a 1 cm $\times$ 1 cm Si chip, with a 100 °C temperature change, and typical values of $\alpha_{\mathrm{PWB}} = 20$ ppm/°C and $\alpha_{\mathrm{Si}} = 2.62$ ppm/°C are utilized, then the mismatch in system horizontal expansion will be 12.4 μm. To overcome such thermal mismatch, the interconnect structures must move in the lateral direction. Fig. 7 shows the measurement system setup for the horizontal displacement of the S-shape interconnect system thermally actuated by the integral microheater chip. The electrically connected electroplating bonded interconnect system is packaged within a plastic case to reduce the influence of air convection on the system. However, an opening for the objective lens of the microscope is required in order that micron-scale lateral movement of the measurement point could be seen. The packaged interconnect system is then electrically connected to a current source for heater operation and light emitting diode (LED) connections. As described in Section II, the electrical conductivity test lines are designed with 49 interconnect connections per sector to observe the mechanical failure on any sector while heat is applied on the system. This electrical continuity can be monitored by passing current in series through the



(a)



(b)

Fig. 7. The measurement setup for horizontal displacement of S-shape interconnects. (a) measurement setup (b) packaged chip interconnect system.

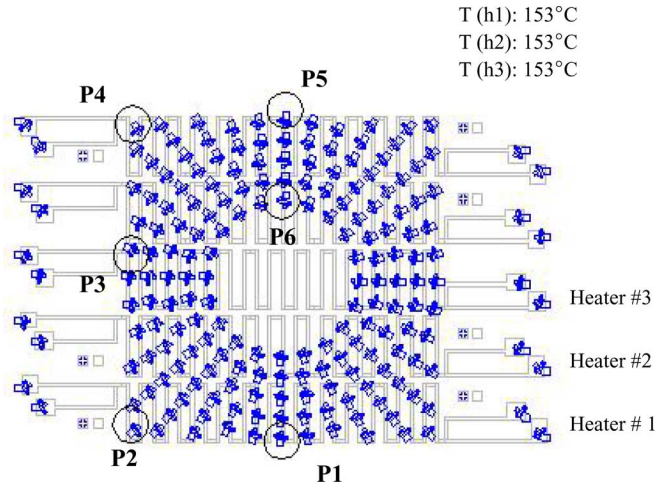


Fig. 8. The measurement positions labeled P1-P6.

TABLE I
COMPARISON OF SIMULATION AND MEASUREMENT VALUE OF DEFLECTION AT VARIOUS POINTS IN THE SYSTEM [UNIT: μm]

		P1	P2	P3	P4	P5	P6
Heater1	Measurement	3.53	12.27	11.81	15.36	13.60	10.2
	Simulation	2.61	10.82	14.4	21.13	19.4	13.8
Heater2	Measurement	6.70	10.52	13.54	15.05	12.16	N/A
	Simulation	5.73	11.30	11.49	16.82	14.16	N/A
Heater3	Measurement	8.10	12.34	8.99	11.54	10.00	N/A
	Simulation	10.41	14.32	10.72	14.24	10.25	N/A

daisy-chained interconnect to power an LED. If any interconnect is disconnected by the thermal expansion or stress, then the LED will no longer remain illuminated. Four LEDs (one for each quadrant) are prepared for observing the electrical connection status of the electroplating bonded chip interconnect system during movement testing. The electrically connected and sealed system is placed on the platform of the microscope that is capable of motion in the x and y direction. The microscope system is connected to a monitor and x, y, z distance reader (QUADRA-CHEK 200). With the measurement setup, the horizontal movement of the chip interconnect is measured during thermal excitation. First, an original point for a spot on an interconnect is chosen before heater operation. Second, movement of the point is traced after heater operation. Third, the comparison between two points is read by the distance reader. The measurement is only carried out on one half of the substrate because the system is designed with symmetric geometry. Fig. 8 describes the measurement locations and energizing heater locations. Heater numbers 1, 2, and 3 are operated to 153 °C individually and the measurement is carried out on six positions on the same interconnect structures. The measurement result i.e., lateral motion of each measurement point, is summarized in Table I.

A thermal simulation for horizontal displacement of chip interconnects is performed with ANSYS 7.0. The purpose of this simulation is to verify the measurement result. The same geometry as in the fabrication mask is exported from AUTOCAD, the mask design tool, to the FEM simulation tool. Using the symmetric geometry of the system, the simulation is executed using only the half area of the substrates. The assumptions for this simulation are that 1) no expansions occurred at the center of the heater and bottom substrate (PWB); 2) heat is uniformly distributed throughout the whole system; 3) the S-shaped interconnects are mechanically well connected to surfaces of the substrates; and 4) the temperature change is 153 °C–25 °C = 128 °C. Fig. 9(a) shows the simulation schematic and a result when the heater number 1 is operating. After thermal simulation, the result is compared with the measurement result as shown in Table I. From Table I, we can recognize that the simulation and measurement value do not agree well on several simulations, especially in the case of P4 and P5 with heater number 1 operating. The difference between the measurement and the simulation of P4 and P5 is 5.77 and 5.8 μm, respectively. However, horizontal displacement of interconnects on P1

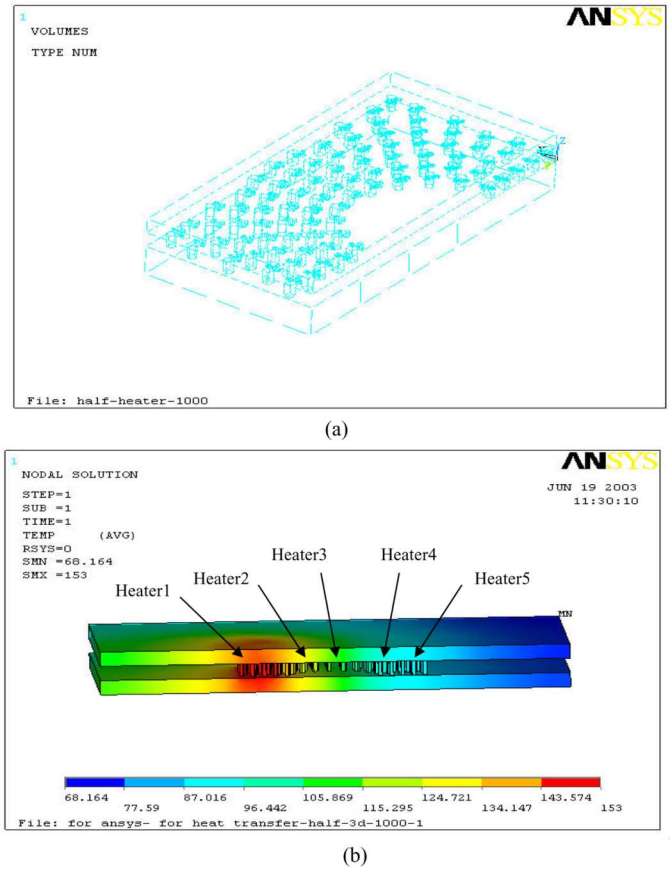


Fig. 9. Finite element calculation for horizontal movement of the interconnects: (a) schematic and (b) the simulation result of heat transfer.

and P2, which are located very close to the energized microheater number 1, agreed very well with the simulation result. A similar correspondence is also obtained from point P2 when heater number 2 is energized and point P3 when heater number 3 is energized. As mentioned before, the thermal expansion of the substrate can be calculated by its CTE, temperature change, and length from center of heater. In those calculation factors, the CTE and length are fixed values for the simulation. On the other hand, the temperature change can be variable during system operation due to heat convection from any external source. If the system is affected by heat convection which is affected by air flow, we can assume that the temperature of the real device is not uniformly distributed. Furthermore, this assumption is likely to be valid because the real measurement system has an opening on the top to accommodate motion of the microscope objective, and the opening can introduce a minor air convection effect to the system. Therefore, the finite element analysis is executed under an environment of heat convection to more accurately reproduce the results of the actual experiment.

From previous comparisons of ANSYS simulation and measurement, the measurement of the real heat distribution is required. The measurement of the heat distribution is performed with a thermocouple and a temperature indicator. Applying the same current, the thermocouple is placed on the glass directly above the heaters in a sequential fashion. That is, while heater number 1 is working, the thermocouple is placed on heater 1, 2, 3, 4, and 5. The same measurement is carried out with heater 2 and heater 3. The measurement results agreed well with any case and the measurement values with heater number 1 working are 153 °C, 145.4 °C, 111.3 °C, 92 °C, 75.9 °C, on heaters numbered 1–5, respectively. The measurement result shows that uniform heat distribution cannot be applied to the simulation in this case. To support this measurement result, an ANSYS heat transfer simulation is performed with the chip interconnect system. The simulation requires a heat transfer coefficient $[h]$ for the system, which will be estimated as described below.

An overall heat transfer coefficient for a generic system placed on a plastic package with air environment is calculated as

$$\frac{1}{h} = \frac{1}{\alpha_1} + \frac{w}{\lambda} + \frac{1}{\alpha_2} \tag{2}$$

where $\lambda[\mathrm{W/m \cdot K}]$ is the thermal conductivity of a model system, α_1 and α_2 are the respective individual heat transfer coefficients, $h\,[\mathrm{W/m^2 \cdot K}]$ is the overall heat transfer coefficient and w is the width of the system.

With (2), the overall heat transfer coefficient can be calculated as

$$\frac{1}{h} = \frac{1}{5} + \frac{2.5 \times 10^{-3}}{385} + \frac{1}{4}$$
$$h = 2.05 \tag{3}$$

where $\lambda = 385[\mathrm{W/m \cdot K}]$ for copper is the thermal conductivity of the interconnect structure with the fact that the heat is well conducted to the PWB substrate by copper interconnect, $\alpha_1 = 5[\mathrm{W/m^2 \cdot K}]$ is the heat transfer coefficient for natural air convection, $\alpha_2 = 4[\mathrm{W/m^2 \cdot K}]$ is selected assuming that the heat transfer coefficient in the plastic package is lower than the air convection environment, and $w = 2.5$ mm [1 mm glass + 1 mm PWB + 500 μm interconnect layer] is the width of the system. This estimation process yields a value of h of approximately 2, which will be used in the ANSYS simulation. The simulation result of heat transfer is shown in Fig. 9(b).

With the result of heat transfer measurement and simulation, the ANSYS simulation of the interconnect movement is performed again. The limitation of the simulation tool makes it necessary to establish a complex simulation step. In the ANSYS simulation, the temperature cannot be assigned to a specific part in the thermal simulation case. So, the simulation is done part by part. Hereafter, the word, "part" will be used for convenience and heater number 1 part is for interconnect system (glass, interconnect and PWB) part which is located on above the heater number 1. The meaning of part by part is that the simulation is first executed on heater number 1 with the measurement temperature to get a displacement value on the edge of the part that is originally connected with the heater number 2 part. Then, the obtained value is inserted in the boundary condition for the simulation of heater part 2. This method assumes that the coefficient of thermal expansion of a material is not changed with any situation. The simulation value with the method is shown in Table II. In the table, simulation I is for uniform heat distribution simulation and simulation II is for the measured heat distribution simulation.

TABLE II
COMPARISON OF HORIZONTAL DISPLACEMENTS OF MEASUREMENT AND SIMULATION [UNIT: μm]

		P1	P2	P3	P4	P5	P6
Heater1	Measurement	3.53	12.27	11.81	15.36	13.60	10.2
	Simulation II	2.52	12.51	12.37	15.91	15.3	12.8
	Simulation I	2.61	10.82	14.4	21.13	19.4	13.8
Heater2	Measurement	6.70	10.52	13.54	15.05	12.16	N/A
	Simulation II	6.95	12.75	12.65	14.4	13.2	N/A
	Simulation I	5.73	11.30	11.49	16.82	14.16	N/A
Heater3	Measurement	8.10	12.34	8.99	11.54	10.00	N/A
	Simulation II	10.28	12.75	12.8	12.86	10.02	N/A
	Simulation I	10.41	14.32	10.72	14.24	10.25	N/A

From the result, the measurement value can be seen to agree very well with the heat transfer simulation result.

D. Characterization of Electrical Properties of the Interconnects

Electrical properties of the beam structures are measured using their electrical characterization elements as seen in Fig. 10(a). Considering the ITRS roadmap, since the operating voltage decreases 20% per technology node (IC technology generation, e.g., 45-nm technology node), increasing noise sensitivity is becoming an important issue in the design of functional devices (e.g., transistors, gates) and products (such as DRAMs or MPUs) [23]. The fabricated chip interconnect has a relatively large length due to its meander type geometry compared to a solder bump. As in wirebonding, the long and round S-shape can produce parasitics such as high resistances and inductances. It is therefore very important to verify the electrical characteristics of the interconnects. The capacitance properties are neglected because the interconnects have a sufficiently large pitch and have overhanging structures that can diminish the electrical effect of the substrate on the structure. Therefore, we can assume that power loss in the chip interconnects is usually due to their resistances and inductances. The electrical characterizations are performed using a network analyzer with two ports. The sweep frequency of the network analyzer is 100 MHz–15 GHz. By using a two-port network analyzer measurement technique, the scattering parameters (S-parameters) are obtained. The S-parameters are then used to extract the impedance parameters by using a Hewlett Packard-Advanced Design System (HP-ADS). From the impedance parameters, the resistances and inductances are calculated as shown in Fig. 10(b). From the graph, the value of the measured inductance is constant (approximately 0.36 nH) up to 15 GHz. It means that resonant frequency occurs over 15 GHz and that the interconnect has good properties for high RF applications. Also, the graph shows the resistance profile of the interconnects. The resistance increases as the frequency increases due in part of the skin effect at higher frequency.

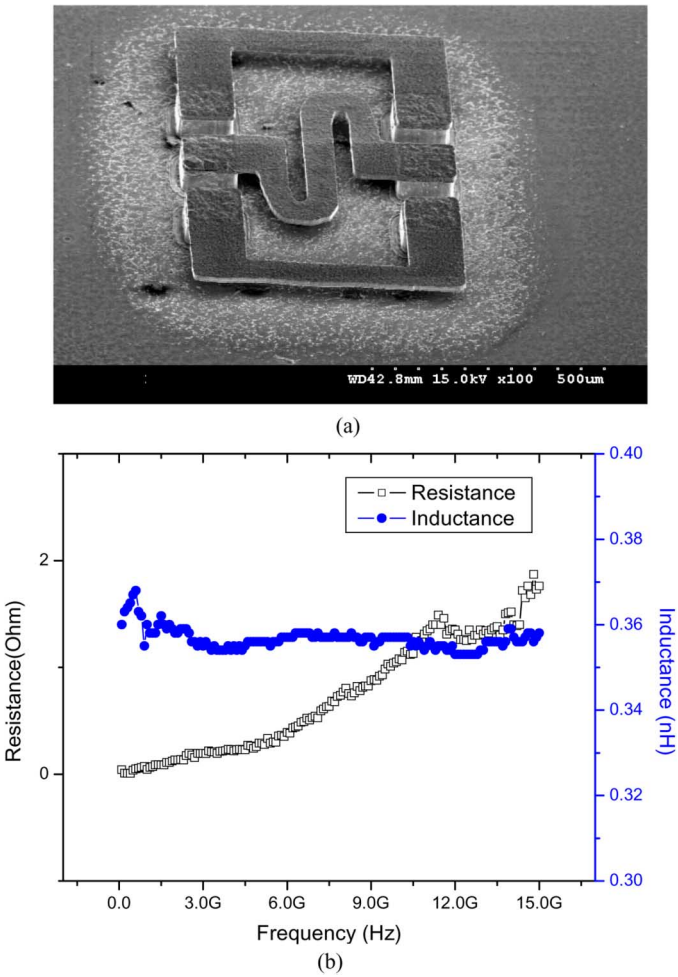


Fig. 10. Electrical characterization of the S-shaped interconnects. (a) a SEM of the measurement structure and (b) a graph for inductance and resistance of the interconnect.

E. Characterization of Thermal Reliability of the Interconnect System

The thermal reliability testing of chip packaging has typically been performed in a thermal chamber. The heat for the chamber is usually provided by convection or radiation. Thermal reliability tests have been carried out for monitoring the anticipated operating environment of the final product and for examining the quality of the product. Thermal reliability testing can be performed with different thermal cycle specifications. For example, a cycle profile specified by MIL-STD-883 for the thermal test of electronic packages is -65 °–150 °C [24]. Alternately, IBM has been using 0 °C–100 °C for flip chip testing [25].

Heaters number 2 and 3 are operated simultaneously for thermal reliability testing to obtain a more uniform temperature distribution of the microheater chamber. Electronic switching circuitry, as shown in Fig. 11(a), is created to achieve thermal cycling with 5 min intervals and working within a temperature range of 40 °C–147 °C. The electronic circuit is composed of a MOSFET (IRF540, Intersil), a function generator, a resistor and power supply.

System characterization of the microheater thermal chamber can be described as a function of temperature and time. By

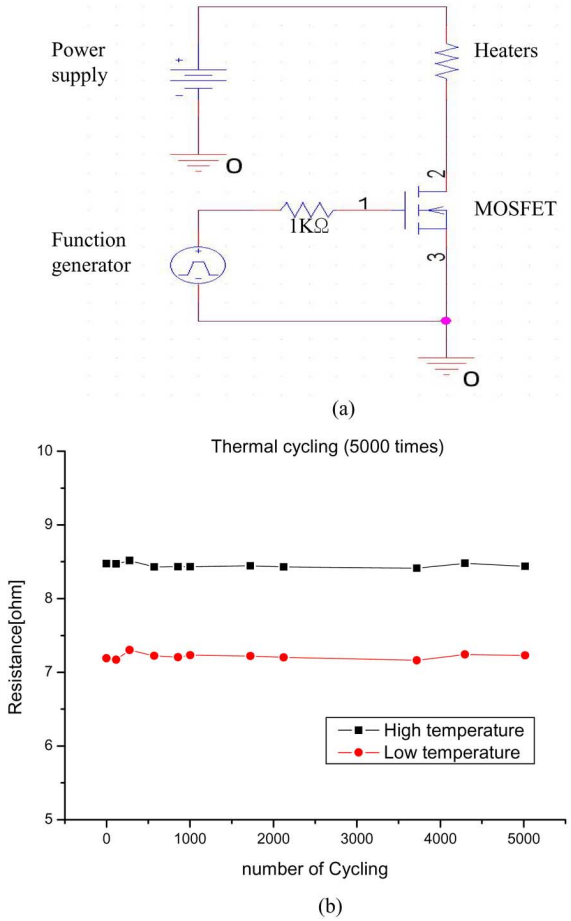


Fig. 11. Thermal reliability test of Cu electroplating bonded chip interconnect system: (a) cycling circuitry and (b) resistance for the 216 structure connection during the cycling.

monitoring the temperature as a function of the time, a system thermal time constant, where the temperature has reached 67% of its steady state value [26], is obtained. The obtained time constant is $\tau = 15$ s and the temperature profile may be described as by following

$$T = T_0 \left(1 - e^{-\frac{t}{\tau}}\right) \tag{4}$$

where T is a temperature as a function of time (t) and T_0 is an final temperature.

The electrical resistance of an electrical conduction line of interconnects is measured while the system is in a high temperature state and a low temperature state. The result is shown in Fig. 11(b). The electrical resistance of the system is changed by variation in temperature. The testing is performed for 5000 cycles and the electrical resistance of electrical connection has almost a constant value as a function of cycle number, predicting excellent reliability for this system.

V. Conclusion

A Cu-electroplating-bonded, S-shape flexible interconnect system for chip-to-board interconnection is fabricated, characterized, and simulated. A mechanical measurement with nanoindenter is performed to show that the interconnect has a sufficient vertical movement for the wafer level electrical and burn-in test. Five microheaters are embedded in the chip to mimic electronic devices such as memory chips or handheld electronic devices and to function as a mini thermal reliability chamber as for real electronic devices. The heater characterization is carried out to show the functionality and the working performance. Thermal reliability tests are performed to verify the thermal performance for 5000 cycles with automatic thermal cycling. The results of the thermal reliability test shows that the chip interconnect system has good thermal reliability and electrical properties.

The 2006 ITRS roadmap expects that chip interconnect systems should endure in high temperature (up to 200 °C) environments in 2016. As mentioned several times before, the CTE mismatch between substrates could be critical issues in the thermal conditions. In the microheater embedded flexible interconnect experiment, the harsh environmental condition (153 °C) is applied to the system with 219 I/O interconnects and 225 mm ^{2} chip size. The electroplating bonded interconnect system has successfully endured the high temperature, harsh environment testing. Considering I/O number, the designed system can be used for memory, handheld, harsh and low cost devices today while meeting ITRS requirements. If the interconnect bonding number is increased with additional research, the technology is expected to be utilized in electronic chip packaging for future ITRS-mandated devices.

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