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A metallic buried interconnect process for through-wafer interconnection

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Abstract

In this paper, we present the design, fabrication process and experimental results of electroplated metal interconnects buried at the bottom of deep silicon trenches with vertical sidewalls. A manual spray-coating process along with a unique trench-formation process has been developed for the electroplating of a metal interconnection structure at the bottom surface of the deep trenches. The silicon etch process combines the isotropic dry etch process and conventional Bosch process to fabricate a deep trench with angled top-side edges and vertical sidewalls. The resulting trench structure, in contrast to the trenches fabricated by wet anisotropic etching, enables spray-coated photoresist patterning with good sidewall and top-side edge coverage while maintaining the ability to form a high-density array of deep trenches without excessive widening of the trench opening. A photoresist spray-coating process was developed and optimized for the formation of electroplating mold at the bottom of 300 μm deep trenches having vertical sidewalls. A diluted positive tone photoresist with relatively high solid content and multiple coating with baking between coating steps has been experimentally proven to provide high quality sidewall and edge coverage. To validate the buried interconnect approach, a three-dimensional daisy chain structure having a buried interconnect as the bottom connector and traces on the wafer surface as the top conductor has been designed and fabricated.

1. Introduction

With the advances in integrated circuit (IC) and microelectromechanical systems (MEMS) technology, the need for a three-dimensional (3D) metallization process is ever increasing. Initiated by the very basic need for metal lines in 3D spaces to overcome the limitations of conventional IC process techniques, the 3D metallization technique has undergone remarkable advances in various fields of application. Die-level stacking of multiple chips and wafer-level packaging are some of the good examples that will benefit from 3D metallization. Among some of the innovative processes developed, two of the widely used are through-wafer interconnection and metallization on a surface with very high topography such as deep cavities [1–8].

Up to the present, research efforts on fabricating patterned metal structures at the bottom of a deep trench have been limited to utilizing wet-etched cavities in general, due to the difficulties in patterning photoresist at the bottom of the trench with good coverage at the top-side edges and sidewalls. Typically, a wet anisotropic etch process using potassium hydroxide (KOH) or Tetramethylammonium hydroxide (TMAH) solution is used, to obtain sloped top-side edges and to improve the step coverage. Kutchoukov *et al* proposed an edge rounding-off technique to further improve the step coverage of wet-etched cavities [5]. Despite the advantages of simple processing and ability to batch process multiple wafers without the aid of costly equipment, the wet anisotropic etch process has certain drawbacks. While providing the angled sidewall suitable for photoresist coating, cavities generated by anisotropic etch process occupy a much larger footprint than the active area at the bottom. The increment of area occupied by the trench opening increases with the cavity depth and makes it difficult to fabricate high-density arrays of cavities. Moreover, dependence on the opening shape and passivation of the front-side structure during the etch process poses another challenge.

Despite these fabrication challenges, several successful approaches to fabricate plated metal structure at the bottom of deep vertical trenches have been demonstrated. Arnold *et al*

fabricated electroplated metal microstructures at the bottom of 75 μm deep trenches using spin-coated thick negative photoresist as the plating mold [6]. However, the step coverage and uniformity of the spin-coated photoresist will deteriorate substantially with the increase of trench depth. Herrault *et al* used conformally deposited and laser-patterned parylene-C as the electroplating mold, to fabricate metal structures at the bottom of 300 μm deep vertical trenches [7]. Although laser micromachining is well suited for patterning on non-planar surfaces and inside the deep cavities, the serial nature of the technique will affect the throughput of the overall process. Electrodeposited photoresist is known to be an effective solution for coating on vertical sidewalls coated with metal seed layers, but the process requires complex setup and thorough maintenance of the bath to have a reproducible result [8]. Also, the relatively short lifetime of the bath will result in increased material cost [9].

In this research, we propose a new type of electrical interconnect using electroplated connectors buried inside the deep trenches formed by dry silicon deep-etch process. Such interconnect has applications in analog or low-density digital circuits, and may be particularly useful in backside MEMS packaging. As high aspect ratio trenches having vertical sidewalls are used, a high-density array of trenches can be formed and more efficient use of substrate backside area can be expected, compared to the processes using wet chemical etching. For the realization of the buried interconnect, we have developed a spray-coating process optimized for coating inside deep vertical trenches up to 300 μm deep. Spray-coated photoresist has been used as the plating mold for metal structures at the bottom of the deep trenches. In combination with the spray-coating process, a unique trench formation process has been developed using conventional inductively coupled plasma reactive ion etch (ICP RIE) and a modified Bosch process [10]. Vertical trenches with angled top-side edges are fabricated for better coverage with the spray-coated photoresist without excessively compromising the efficiency of the surface area usage. By combining the buried interconnect proposed in this research with a through-wafer via technique, a more efficient interconnection scheme can be obtained. Interconnects buried inside the substrate can be used to make electrical connection between the front-side structures through vertical through-wafer vias having reduced height. Moreover, the through-wafer vias connected to the buried interconnect can be fabricated simply by a bottom-up metal plating process. By fabricating the buried interconnect and filling the via holes by electroplating from the bottom, void-free metal filled vias can be fabricated without the need of substrate bonding, hole sealing, or complex electroplating processes [1, 11, 12].

2. Design

For the verification of the proposed buried interconnect fabrication process, an array of electroplated metal connectors is designed and fabricated. Figure 1 shows the designed mask layout for the trench and electroplating mold; the dimensions are summarized in table 1. Figure 2(*a*) shows the perspective and cross-sectional views of the fabricated buried interconnect at the bottom of 300 μm deep (d_{t1}) trenches on a 500 μm thick (t_s) substrate. As compared in figures 2(*a*) and (*b*), an achievable geometry differs significantly depending on the trench formation method. Vertical trenches fabricated with the Bosch process will enable a higher density array of trenches having larger aspect ratio at the cost of difficulties in plating mold formation process due to poor step coverage during the lithography process. Due to the crystallographic axis dependence, a trench formed with anisotropic wet etching will suffer larger opening size and limitations in trench depth (d_{t2}) for array formation (figure 2(*b*)). To maintain the trench bottom surface area (or width w_{t1}) and metal pattern size defined in figure 1, the trench depth will be limited to 212 μm when an anisotropic wet etch process is used.

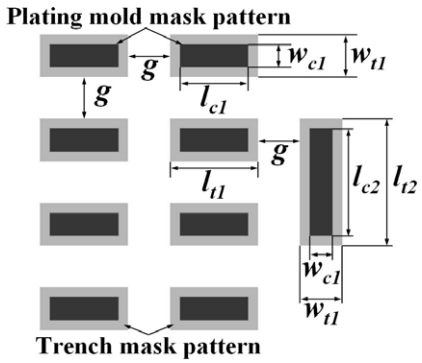
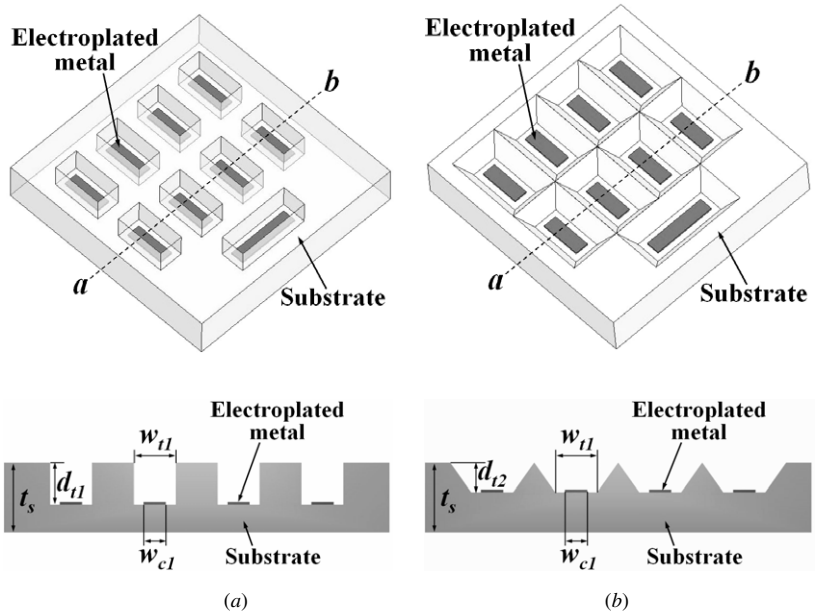


Figure 1. Mask layout for the buried interconnect fabrication.

Table 1. Mask dimensions of the buried interconnect structure (defined in figure 1).

Label	l_{t1}	l_{c1}	w_{t1}	w_{c1}	l_{t2}	l_{c2}	g
Dimension (μm)	620	480	300	160	900	760	300

To combine the advantages of the two processes shown in figure 2, a fabrication process for trenches with vertical sidewalls and rounded-off edges has been developed (figure 3(*a*)). For the electroplating of thick metal structure at the bottom of the deep trenches, the mold fabrication process has been optimized with a spray-coated photoresist. The proposed trench formation process enables a high density array of deep trenches with vertical sidewalls combined with angled top-side edges for better coverage during the subsequent spray-coating process. Due to the dry isotropic etching used in the trench-formation process, the trench width ($w_{t1'}$) increase is unavoidable. However, the amount of trench opening size change is independent of the trench depth. Change in trench width ($w_{t1'}$) due to the etch process used and increase in electroplated metal structure width ($w_{c1'}$) resulting from the proximity effect during lithography process have been characterized. These changes in sizes can be compensated by mask pattern size reduction. As shown in figure 3(*b*), by combining the buried interconnect with metal filled via and front-side metallization process, a 3D interconnection structure with shorter through-wafer interconnection distance can be fabricated. To verify the proposed buried interconnect



(*a*) (*b*)

Figure 2. A buried interconnect structure fabricated with conventional processes: (*a*) perspective and cross-sectional views along line a–b of the buried interconnect fabrication result when the trench is fabricated by the Bosch process, (*b*) perspective and cross-sectional views along line a–b when the trench is etched by wet anisotropic etching.

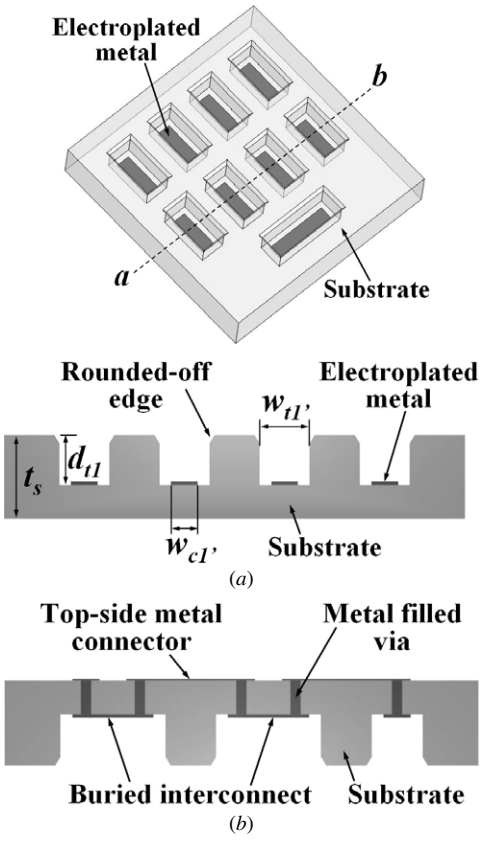


Figure 3. Designed structure: (*a*) perspective view and cross section along line a–b of the buried interconnect fabrication result using the proposed processes, (*b*) cross-sectional view of the daisy chain structure using the buried interconnect as the bottom connector.

scheme, a daisy chain structure using buried interconnect as the bottom connector with fully metal-filled via and top-side connector has been fabricated.

3. Fabrication process

3.1. Combined silicon etch process for backside trench formation

Deep silicon etch using the Bosch process has widely been used in fabricating vertical trenches due to its CMOS-compatibility, high etch rate and ability to form a near vertical structure having hundreds of microns of depth. It is well known that the sidewall slope of the deep-etched trench can be controlled by modifying the etch parameters, such as gas flow rate [10]. Tezcan *et al* tested the sloped via etch process by modifying the Bosch process parameters, and fabricated 100 μm deep trenches having a sloped sidewall where formation of negative corners at the via opening and substantial sidewall roughness were observed [13]. Although the surface roughness was reduced and the negative corners were removed by an additional isotropic etch process, top-side edges were near vertical after the process, and effect of these geometries on later processes, such as insulation and conductive material deposition and patterning, has not been explored. Moreover, the tested process requires increased amount of undercut to obtain a positive-sloped sidewall as the trench depth increases, which negates the advantages of the high-spatial-density Bosch process. For successful coverage of the deep trenches with the spray-coated photoresist, a positive sidewall slope at the opening and a smooth surface are essential. Instead of directly modifying the etch parameters of the Bosch process, we combined a dry isotropic etch of silicon with the Bosch process to fabricate a vertical trench having rounded-off top-side edges, where the slope and depth of the top-side edge can be controlled independent of the trench depth.

The combination of an isotropic etch process with the Bosch process has widely been researched to provide a dry

Table 2. Parameters for the isotropic and vertical silicon etch processes: Dep.: polymer deposition, Etch A: polymer etch step, Etch B: silicon etch step, RF1: coil power, RF2: platen power.

		Isotropic etch			Vertical etch		
Parameters		Dep.	Etch A	Etch B	Dep.	Etch A	Etch B
Duration (s)		2	20	~1200	3	4	5
Pressure (mTorr)		15	15	15	15	20	25
	Ar	30	30	30	40	40	40
Gas flow rate (sccm)	SF_6	0.5	75	100	0.5	100	100
	C_4F_8	75	0.5	0.5	100	0.5	0.5
RF power (W)	RF1	1	15	13	1	12	10
	RF2	825	825	825	825	825	825

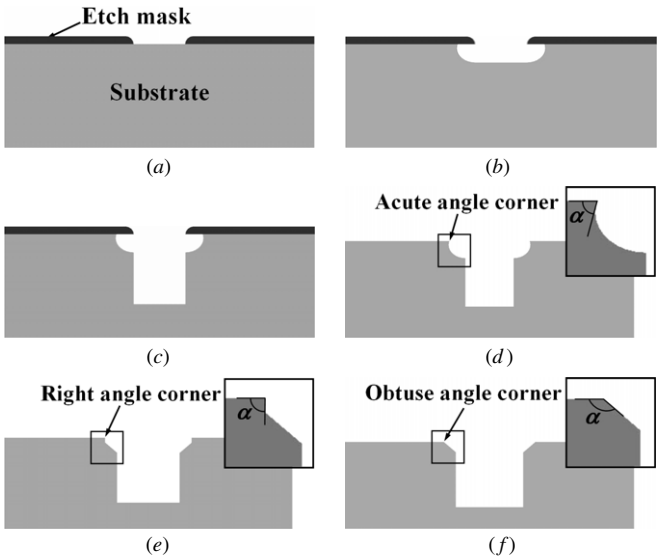


Figure 4. Process sequence of the combined silicon etch process (the inset shows the magnified view of the marked region): (*a*) mask patterning, (*b*) isotropic etch, (*c*) Bosch process, (*d*) mask removal ($\alpha < 90^\circ$), (*e*) short isotropic etch ($\alpha \sim 90^\circ$), (*f*) extended isotropic etch ($\alpha > 90^\circ$).

release technique for a suspended movable structure, where the bottom of the vertical trench has been isotropically etched away [14, 15]. In this research, we performed the isotropic etch at the beginning of the trench fabrication process, followed by the Bosch process. As summarized in table 2, the silicon etch step of the Bosch process was used for the isotropic etch process, so that the two different types of silicon etch can be processed in the same chamber. Any type of dry isotropic silicon etch process, such as a XeF_2 etch, can be combined instead of the process used. Compared to conventional wet etch processes, the increase of trench opening is minimal and is independent of the total trench depth. The depth of the angled edges can be controlled by the amount of initial isotropic etch process. Moreover, the slope of the edges can be controlled by modifying the isotropic etch parameters.

Figure 4 shows a detailed fabrication process flow of the trench formation step. Typically, standard photoresist, oxide or the combination of both can be used as the mask material (figure 4(*a*)), and the use of oxide is known to reduce the vertical striations during the Bosch process [10]. In this experiment, a 10 μm thick positive tone photoresist AZ4620 (Clariant) was used as etch mask. Patterned photoresist is hard baked at 120 °C on a hot plate for 30 min. The wafer is cleaned in piranha after the initial isotropic etch and Bosch process. After the initial isotropic etch and Bosch process, sharp acute angle corners are formed at the adjoining region of the top surface and sloped top-side edge. These apexes are formed due to the negative sidewall formation on the isotropically etched facet at the trench opening (figure 4(*d*)). During the final isotropic etch process, these acute angle corners are gradually transformed into right angle corners (figure 4(*e*)), and then into obtuse angle corners (figure 4(*f*)). Positive or obtuse angled corner formation, and thus sufficient amount of final isotropic etch, is crucial for good step coverage during the subsequent photoresist spray-coating process. The acute and right angle corners, due to their sharpness, make the coverage with spray-coated photoresist very poor.

Table 3. Typical dimensions (defined in figure 5(*b*)) of the trench fabricated with the proposed method.

	a (μm)	b (μm)	h (μm)	θ (°)
Wafer 1	15	25	304	31
Wafer 2	30	50	294	31

Figure 5 shows the scanning electron microscope (SEM) image of the typical trench formation results. The silicon etch process has been performed with ICP RIE system (Plasma-Therm). After initial isotropic etch and deep trench formation process, a sharp acute angle corner resulting from the isotropic etch process remains at the starting point of the sloped top-side edge as shown in figure 5(*c*). By the final isotropic etch process, the acute angle corners are fully removed, and the sidewall smoothness is improved. Also, the slope of the vertical sidewall has become slightly more positive. The dimensions defined in figure 5(*b*) have been measured and the average angle of the sloped edge ($\theta = \tan^{-1}(a/b)$) has been calculated for samples having different amount of initial isotropic and vertical etch amount, using white light interferometry (table 3).

3.2. Spray-coating process

Spray coating of photoresist has been utilized in order to overcome the limitations of the spin-coating process and inherent flow nature of the liquid photoresist on these substrates possessing severe topography. Although a

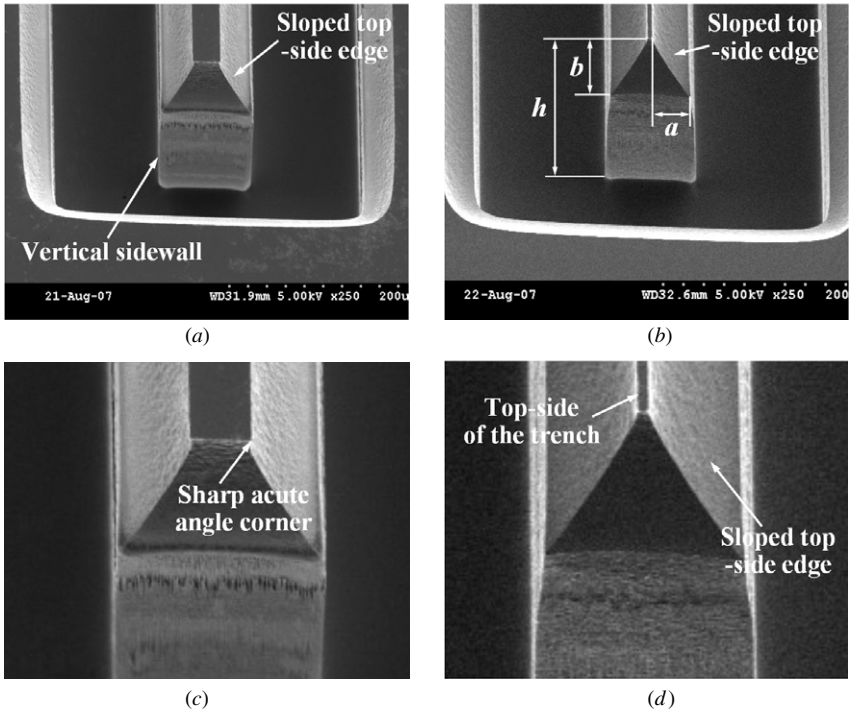


Figure 5. SEM image of the trench formation process: (*a*) after the initial isotropic etch (15 min) and the Bosch process (393 cycles), (*b*) after the additional final isotropic etch process (23 min), (*c*) magnified view of (*a*), (*d*) magnified view of (*b*).

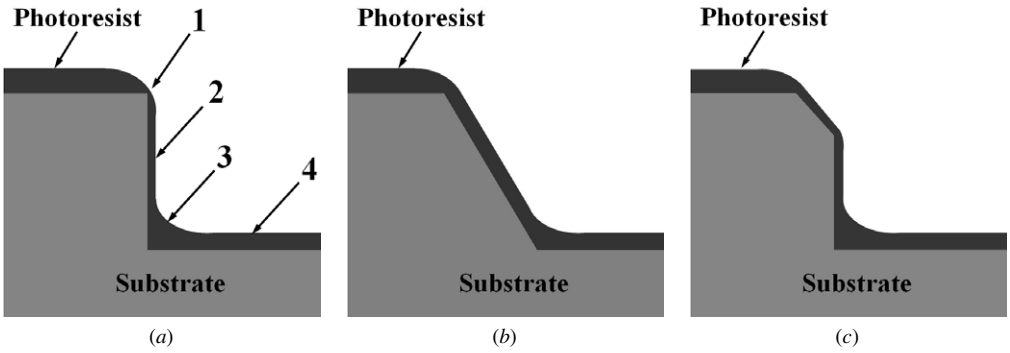


Figure 6. Comparison of the spray-coated cavities: (*a*) cavity with vertical sidewall typically formed by the Bosch process, (*b*) cavity with sloped sidewall typically formed by the anisotropic wet etch process, (*c*) cavity with vertical sidewall having a rounded-off top-side edge proposed in this work.

conformal deposition can be achieved on surfaces with certain amount of topography, uniform coating in a deep cavity is still very challenging even with the aid of spray-coating process. Figure 6 illustrates the typical spray-coating results achievable with different types of cavities. Figure 6(*a*) details the issues related to the photoresist coating on vertical trenches including: 1. poor top-side edge coverage due to photoresist flowing down on the sidewall and receding on the top surface, 2. poor sidewall coverage due to flow, 3. bottom corner over-filling, and 4. the photoresist thickness difference between the top and bottom surfaces. Although some of the coating results have been demonstrated for 100 μm deep vertical trenches [9, 16], most research effort has been focused on coating inside wet anisotropically etched surfaces [8, 9, 17]. Depending on the geometry of the cavity opening and depth, spray-coating conditions vary and have to be optimized even with the use of costly coating equipments. As the cavity depth increases, it is more difficult to have good step and sidewall coverage. As shown in figure 6(*c*), the cavities formed with the combined silicon etch process proposed in this research utilizes the advantages of both the conventional vertical trenches and those of the cavities with angled sidewalls for the spray-coating process.

Before the spray-coating process, the substrate is cleaned in piranha and a 500 nm thick PECVD (plasma enhanced chemical vapor deposition) oxide is deposited for electrical isolation between the copper structure and silicon substrate. Subsequently, titanium–copper–titanium layers having respective thicknesses of 30 nm, 1 μm and 30 nm are deposited. The bottom titanium layer is used as an adhesion layer and diffusion barrier for the copper, and the top titanium layer is used to protect the oxidation of copper seed and to

Table 4. Summary of the spray-coating process.

Step	Process	Method	Incidence angle (θ) (°)/distance (d) (cm)	Baking temperature (°C)/time (s)	Number of times
1	Coating cycle 1	Double coating and 3 min break	90/<5	90/30	1
2	Coating cycle 2	Double coating	45–60/6–10	90/30	6
3	Baking	Final baking		90/60	1

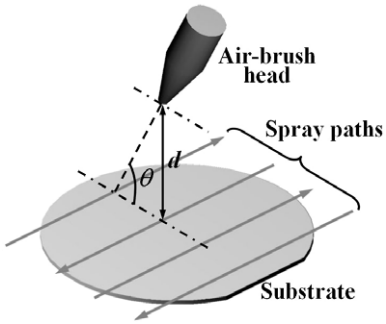


Figure 7. Spray-coating setup and coating method.

promote the adhesion of the photoresist. A 1 μm thick copper seed layer was used in order to guarantee good electrical connection along the severe topographies.

A positive tone photoresist AZ4620 was diluted by 1:1 with propylene glycol methyl ether acetate (PGMEA), which is the generic solvent of the photoresist used, and dispensed with an off-the-shelf air-brush (Paasche Airbrush Company, model H3). Parameters, such as the composition and solid content of the diluted photoresist, dispense rate, spray-on angle, speed of the atomizer movement, spray pressure and temperature of the substrate, affect the quality of the deposited photoresist for spray-coating processes [8, 9, 17]. Due to the limitations in the coating setup used, the spray pressure was set to a constant value of 1.2 bar and the dispense rate was set to its maximum value. Other parameters were optimized to have a void-free coverage of the deep cavities formed by combined silicon etch process. The estimated solid content of the diluted photoresist was 19%, and the measured dispense rate of the air brush was approximately 1.5 ml min^{-1}.

Instead of spinning the substrate during the spraying, the air brush was moved manually to cover the overall surface area of the substrate [8]. For a uniform coating with sufficient photoresist thickness, multiple coatings were performed at different incident angles and directions, and the substrate was baked between each double coating steps. Four different lateral paths were used (figure 7) in each coating step, and the substrate was rotated by 90° for the subsequent coating process to complete a double coating. Since the patterns were formed within 5 × 5 cm^2 area, lateral coating paths were adjusted to have uniform coating on the active region of interest. The number of lateral coating paths can be increased to cover a larger area. Each double coating process is followed by baking at 90 °C on a conventional hot plate to complete a coating cycle. The substrate is then moved to a thermally insulated chuck to maintain the temperature during the subsequent coating process. Table 4 summarizes

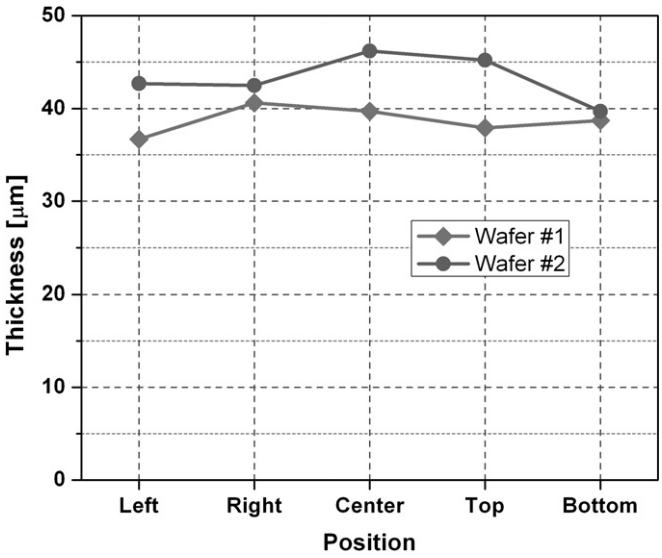
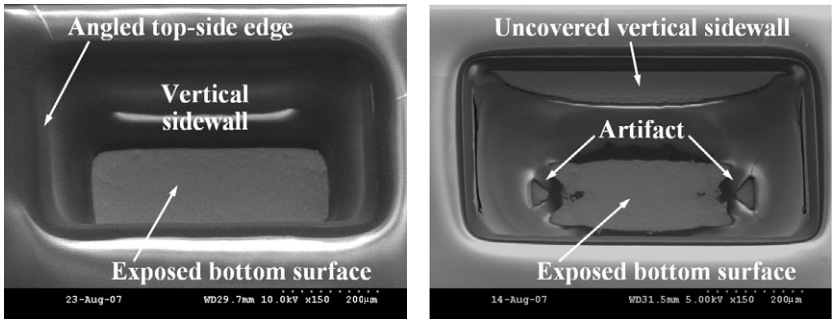


Figure 8. Typical spray-coated photoresist (AZ4620) thickness on the top surface.

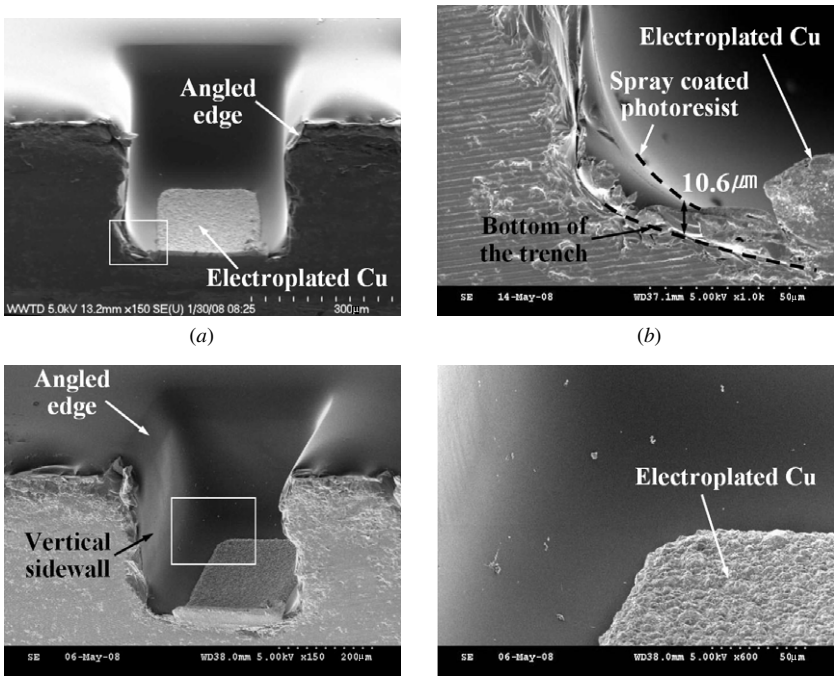
the different coating steps and conditions of the spray-coating process. Singh *et al* reported that the step coverage of the spray-coated photoresist can be improved by controlling the temperature during the coating process [17]. The coating cycle 1 increases the photoresist thickness at the bottom of the trench by direct incidence, whereas coating cycle 2 improves the top-side edge and sidewall coverage. Break time in coating cycle 1, between the double coating and baking, guarantees the self-planarization of the photoresist on the top surface. Together with the rounded-off edge of the deep trench, relatively high solid content and baking between coating cycles improve the step and sidewall coverage. The photoresist-coated substrate was aligned and exposed with a 405 nm source, using an average exposure dose of 1200 mJ cm^{-2}.

The thickness of the spray-coated photoresist inside the 5 × 5 cm^2 active region was measured and analyzed. As shown in figure 8, five point thickness measurements were performed with a stylus profiler (KLA-Tencor P-15 Profilometer) for photoresist on the top surface after the patterning. Photoresist thickness inside the trenches could not be measured precisely due to high aspect ratio and curvature at the bottom surface. Average thicknesses of the spray-coated photoresist on the wafer surface were 38.7 μm and 43.3 μm, and standard deviations were 1.5 μm and 2.5 μm, respectively. The differences between the highest and the lowest points of measurement were 3.9 μm and 6.5 μm, respectively, and these correspond to 10% (±5%) and 15% (±7.5%) of the respective average thicknesses.



(*a*) (*b*)

Figure 9. SEM images of the plating mold formed at the bottom of the deep trench with spray-coated photoresist: (*a*) the pattern defined with positive photoresist, (*b*) the pattern defined with negative photoresist.



(*a*) (*b*)

(*c*) (*d*)

Figure 10. SEM cross-sectional image of the plating mold and electroplated copper: (*a*) front view of the cross-section, (*b*) magnified view of the marked region in (*a*), (*c*) tilted view of the cross section, (*d*) magnified view of the marked region in (*c*); the particles in the image are formed during the sample preparation.

Due to the distance between the mask, which makes contact with the top surface of the substrate, and patterning area (bottom of the trench), some amount of proximity effect is unavoidable. In contrast to the positive photoresist which had a slight pattern size increase due to the proximity effect, a negative tone photoresist suffered from artifact formation due to reflection from trench corners, underexposed vertical sidewalls, and narrow process window for the exposure dose. Figure 9 shows the electroplating mold fabrication result inside 300 μm deep trenches using positive and negative tone photoresists. The same mask pattern with reversed opacity was used in the experiment.

The wafer was developed with AZ400K (Clariant) developer diluted with deionized (DI) water by 1:3. The patterns at the bottom of the trenches were not developed completely by conventional soaking and puddling due to trench depth. To enhance the developer supply to the bottom of the deep trenches, the development was performed in an ultrasonic bath. Use of an air brush for the development was also experimentally proven to be effective.

3.3. Copper plating process

The plating solution consists of 250 g of copper sulfate ($CuSO_4{\cdot}5H_2O$), 25 ml of sulfuric acid (H_2SO_4), and deionized water per liter of plating solution. Before the plating, approximately 7 $\times$ 10 cm^2 sized copper sheet (anode) was thoroughly cleaned with diluted hydrochloric acid (25%). The titanium protective layer in the area to be plated was etched with diluted hydrofluoric acid (2%), and the exposed copper seed layer was cleaned by dipping in diluted hydrochloric acid

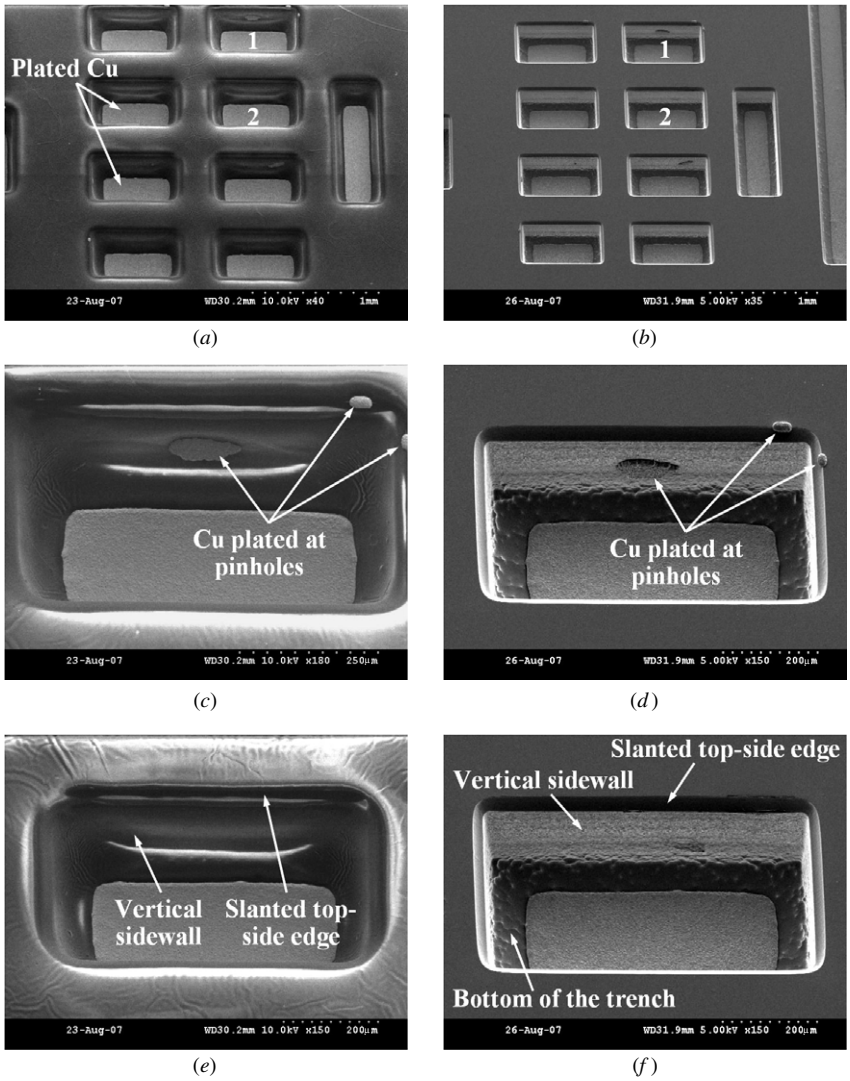


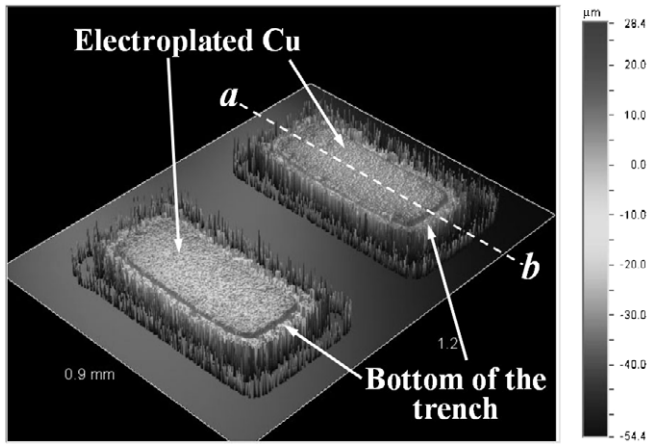
Figure 11. SEM images of the plating mold and electroplated Cu before and after the mold removal: (*a*) bottom side of the buried interconnect structure after the spray-coated mold fabrication process and Cu plating, (*b*) bottom side of the buried interconnect structure after the mold removal process, (*c*) magnified view of area 1 in (*a*), (*d*) magnified view of area 1 in (*b*), (*e*) magnified view of area 2 in (*a*), (*f*) magnified view of area 2 in (*b*).

(25%) for 5 s. A 1000 ml Pyrex beaker was used in the plating and the solution was agitated with the magnetic stirrer during the plating process. A current density of 21 mA cm^{-2} was used, and the plating rate was 0.35 μm min^{-1}. No additional efforts were made to reduce the surface roughness of the plated copper. After the plating process, plating mold was removed with acetone, and the titanium–copper–titanium layer was removed by the subsequent etch in diluted hydrofluoric acid (2%) and copper etchant. Ammonium hydroxide (NH_4OH) saturated with copper sulfate was used as the copper etchant.

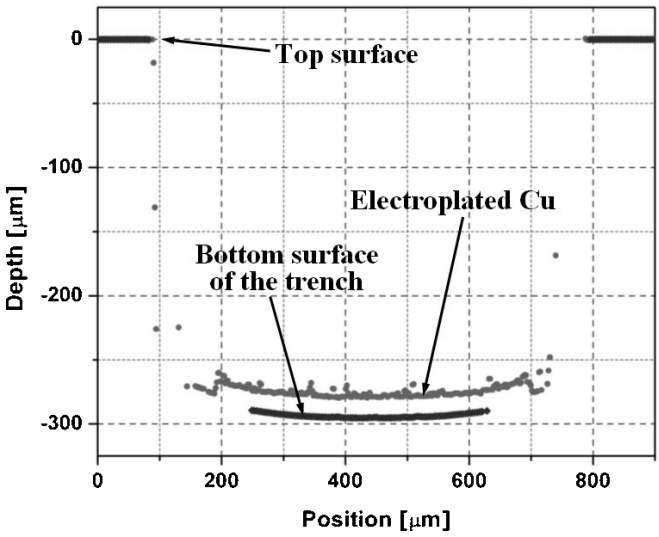
4. Results and discussion

The angled edges of the trench and the step coverage of the spray-coated photoresist are evident in the cross-sectional view in figure 10. Photoresist thickness at the bottom of the trench estimated with the cross-sectional image in figure 10(*b*) was 10.6 μm. As shown in figures 10(*a*) and (*c*), the top-side edges and vertical sidewalls are perfectly sealed with the spray-coated photoresist. Figure 11 shows the SEM image of the electroplated Cu structures at the bottom of 294 μm deep trenches before and after the plating mold removal process. The plating mold is well defined and good coverage of top-side edges and vertical sidewalls was obtained except for some of the pinholes. The unwanted plated copper dots on the sidewall and top-side edges can be removed during the seed layer etch process since the contact area between these electroplated structures and the seed layer is minimal.

The profile and dimensions of the fabricated structure have been measured with white light interferometry. As shown in figure 12, the curvature of the electroplated copper surface is reflected from the bottom surface of the trench, which is an inherent characteristic of the ICP RIE tool used. The thickness of the electroplated copper measured by comparing the profiles in figure 12(*b*) was 15.8 μm.



(*a*)



(*b*)

Figure 12. Profile of the copper plated at the bottom of the trench: (*a*) 3D profile of the bottom surface, (*b*) profile along line a–b in (*a*) before and after the copper plating.

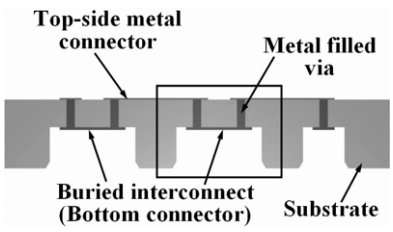
The deviation of planar dimensions of the trench from the mask opening size (300 × 620 μm^2) is mainly attributed to the combined etch process where the dry isotropic etch process is involved. The increase of the opening size (382 × 697 μm^2) is attributed mainly to the initial and final isotropic etch steps, while the bottom area of the trench (327 × 652 μm^2) is increased due to the final isotropic etch process. As the current combined etch process is optimized for patterning inside a 300 μm deep trench, the amount of isotropic etch and resulting trench opening size increase can be reduced depending on the depth and final opening size of the trench.

The increase of bottom connector size (193 × 508 μm^2), compared to the mask dimension (160 × 480 μm^2), is mainly due to the proximity effect during the mold formation process. For a proximity lithography process, the minimum resolvable half grating period ($b_{\min}$) can be approximated as

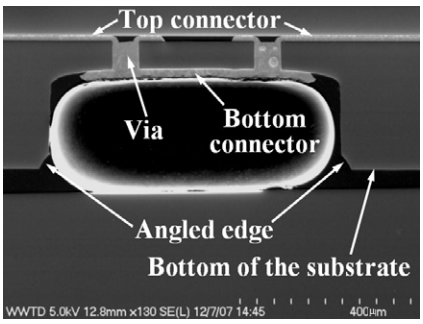
$$2b_{\min} \approx 3\sqrt{\lambda s}, \tag{1}$$

where λ is the wavelength of the exposing radiation and s is the gap between the mask and the photoresist surface [18]. For a 300 μm deep trench, the minimum resolvable half-grating period is 17 μm when a 405 nm source is used, which is in good agreement with the experimentally observed pattern size increase of 14–16.5 μm on each side of the rectangular pattern.

Using the buried interconnect as the bottom connector, a daisy chain structure (figure 3(*b*)) was fabricated. After the buried interconnect fabrication on the backside of the substrate, through-wafer via holes were formed on top of the buried interconnects. Via holes are patterned and etched from the top surface of the substrate, where PECVD oxide deposited on the backside is used as the etch-stop layer. After the etch-stop oxide layer is removed by RIE, PECVD oxide deposition and blank oxide RIE are performed for electrical isolation of the vertical sidewall of the via holes. Via holes are filled by bottom-up electroplating of copper to achieve fully filled vias. Top connectors are then formed on the front side of the substrate to connect vias originating from separate bottom connectors (buried interconnects) to form a daisy chain structure. A partial cross section of the fabricated chain structure is shown in figure 13. As shown in figure 13(*b*), three different layers of electroplated copper structures are well defined and connected as designed, without any void formed in the via. Detailed fabrication process and characterization of the daisy chain structure will be reported separately.



(*a*)



(*b*)

Figure 13. Cross-sectional image of the fabricated daisy chain structure: (*a*) schematic of the fabricated structure and location of the picture on (*b*), (*b*) SEM of the fabricated device (the white circle under the bottom connector is a bubble formed inside the filler).

5. Conclusion

The fabrication process for the buried interconnects has been developed using a combined silicon etch process and an optimized spray-coating process for deep trenches. Deep vertical trenches with angled top-side edges have been fabricated with the combined silicon etch process, and plating mold was defined by spray-coated photoresist inside the deep trenches. The combination of the two processes can be applied to other applications that require the photoresist patterning inside the deep trenches. The fabrication process for the buried interconnect was combined with via filling by metal electroplating to form a daisy chain structure. Such CMOS-compatible interconnect has applications in analog or low-density digital circuits, and can be useful in MEMS packaging which requires backside interconnection.

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