Vertically Laminated Magnetic Cores by Electroplating Ni-Fe Into Micromachined Si

David P. Arnold, *Member, IEEE*, Iulica Zana, *Member, IEEE*, Florent Cros, and Mark G. Allen, *Senior Member, IEEE*

***Abstract*—The fabrication and characterization of vertically laminated, electrodeposited Ni-Fe magnetic cores in micromachined silicon for the low megahertz frequency range is presented. Laminated cores were fabricated by etching vertical trenches (60–180 μm wide and 525 μm deep) through silicon wafers and directly plating Ni-Fe onto the etched sidewalls. The Ni-Fe was plated over a range of thicknesses (3–53 μm) in order to study the influence of eddy currents. The measured impedances in the range 10 kHz–40 MHz confirm the reduction of eddy current losses. This work demonstrates a simple fabrication method for achieving high-aspect-ratio, vertically laminated magnetic cores where the geometry of the structures can be easily tailored for various applications.**

***Index Terms*—Eddy currents, magnetic cores, MEMS, micromachining, nickel alloys, permalloy.**

I. Introduction

ELECTROPLATED, ferromagnetic alloys such as Ni-Fe (80:20 at %) have been widely used for the fabrication of miniaturized electromagnetic devices. One key design consideration for these types of devices is minimization of core losses, which can result from hysteresis effects and/or eddy current effects. The focus of this paper is on the latter. Reduction of eddy current losses is achieved either by using high-resistivity magnetic materials or by laminating the material into thin sheets. For plated soft magnetic materials, the resistivity can only be modestly increased without deteriorating the magnetic properties. Therefore, laminated Ni-Fe cores are preferred, as demonstrated in micro-inductors [1]–[3], power converters [3]–[5], and micro-generators/micro-motors [6].

In macro-scale magnetic devices, low-loss cores are typically achieved by stacking alternating layers of core material and insulating material and laminating the entire stack together. In contrast, incorporating laminations into micro-scale devices poses a significant fabrication challenge, and several approaches have been proposed: mechanical lamination of polymer-coated magnetic foils [1]; repetitive deposition of polymer insulator, seed layer, and electroplated magnetic layers [2]; alternating electrodeposition of magnetic and sacrificial metal layers [3]; alternating sputtering of thin-film magnetic and dielectric layers [4]; and one-step electroplating of high-aspect-ratio vertical structures [5], [6].

Manuscript received October 16, 2003. This work was supported in part by the U.S. Army Research Laboratory under the Collaborative Technology Alliance Program, Cooperative Agreement DAAD19-01-2-0010.

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Digital Object Identifier 10.1109/TMAG.2004.829013

Although these approaches have demonstrated improvement in device performance, processability and scaling remain unaddressed issues. As frequencies increase, lamination thicknesses should be reduced to the order of the magnetic skin depth (micron range) while maintaining total core thicknesses of tens or hundreds of microns to prevent saturation. These requirements dictate large numbers of thin, high-aspect-ratio laminations, which are difficult to achieve using conventional micromolding and electroplating techniques.

This paper presents a batch-fabrication approach for constructing vertically laminated magnetic cores by directly electroplating Ni-Fe into micromachined silicon trenches. This method provides the following advantages over previous approaches:

- cores of large total thickness having micron-scale laminations, achieved in a single electrodeposition step;
- vertically laminated structures, permitting magnetic flux to pass both in-plane and out-of-plane;
- integration of cores with other micro-fabricated structures;
- high-temperature compatible structures.

High-aspect-ratio, bar-type, vertically laminated magnetic cores were micro-fabricated and tested to verify the eddy current reduction.

II. Fabrication

Laminated magnetic cores were built by directly plating Ni-Fe onto the sidewalls of vertical trenches, etched out of low-resistivity (0.001 Ω·cm), 525-μm-thick, n-type silicon wafers. The fabrication process begins by growing a 2000-Å thermal oxide, which prevents electrodeposition on the top and bottom surfaces. Next, AZ4620 photoresist is patterned as a mask for etching trenches in the oxide and silicon using inductively coupled plasma (ICP) etching [7]. The through etch is achieved by etching half way from the top of the wafer and then etching the remainder from the bottom side. The photoresist is then stripped, and the wafer is cleaned in "piranha etch" (3:1 $H_2SO_4 : H_2O_2$, 120 °C) for 10 min. A brief HF dip is used to remove the native oxide on the silicon sidewalls immediately before electroplating. A standard Ni-Fe bath [8] is used with two nickel anodes placed approximately 3 cm from each face of the sample. The low-resistivity silicon provides a conduction path for electrodeposition, and the metal deposits only on the etched silicon sidewalls. The metal is plated to a thickness such that an air gap remains between adjacent laminations, resulting in a structure having a repetitive pattern of Ni-Fe: Si: Ni-Fe: Air.

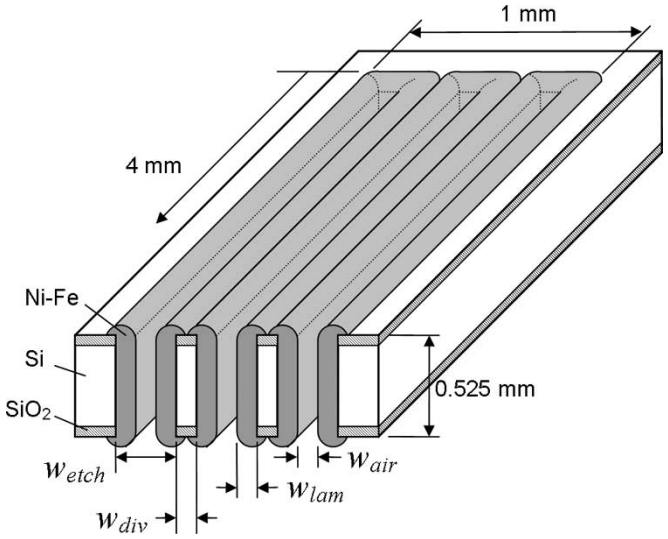

Fig. 1. Schematic of vertically laminated Ni-Fe core. For illustration, $w_{\rm etch} = 3w_{\rm div} = 3w_{\rm lam} = 3w_{\rm air}$, depicting a packing density of 50%.

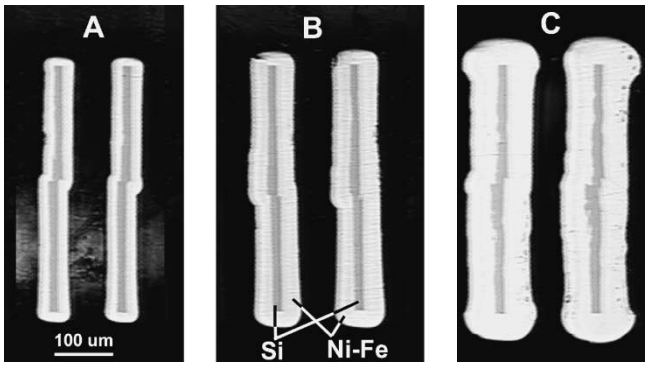

Fig. 2. Optical images showing partial cross-sections of laminated Ni-Fe structures with different $w_{\rm lam}$ (A = 23 μm, B = 38 μm, and C = 53 μm). Some misalignment is noted between the top- and bottom-side etch.

Using this technique, a variety of vertically laminated cores were produced with overall dimensions of 1 mm wide×4 mm thick, as shown in Fig. 1. Fig. 2 shows optical images of cross-sections of several plated Ni-Fe structures. To explore the fabrication limits and the effectiveness of eddy current reduction, the widths of the silicon etch $w_{\rm etch}$ (60–180 μm), silicon divider $w_{\rm div}$ (20–50 μm), lamination $w_{\rm lam}$ (3–53 μm), and resulting air gap $w_{\rm air}$ (53–163 μm) were all varied. The packing density α is defined as the ratio between the magnetic (Ni-Fe) cross-sectional area and the total cross-sectional area of the core

$$\alpha = \frac{A_{Ni-Fe}}{A_{\rm total}} = \frac{2w_{\rm lam}}{w_{\rm etch} + w_{\rm div}} = \frac{2w_{\rm lam}}{2w_{\rm lam} + w_{\rm air} + w_{\rm div}}. \quad (1)$$

The packing density is maximized by reducing the silicon divider and air gap, but fabrication constraints limit the minimum widths of these features.

The silicon divider width is limited by deep silicon etching technology. Structures were created with silicon dividers ranging from 20–50 μm. Reliably creating much smaller dividers presents a substantial fabrication challenge (particularly when front-to-back alignment is used to etch from both sides). No change in plating uniformity was noted for the different silicon divider widths, so only the cores with 20 μm dividers (highest packing density) were used for testing.

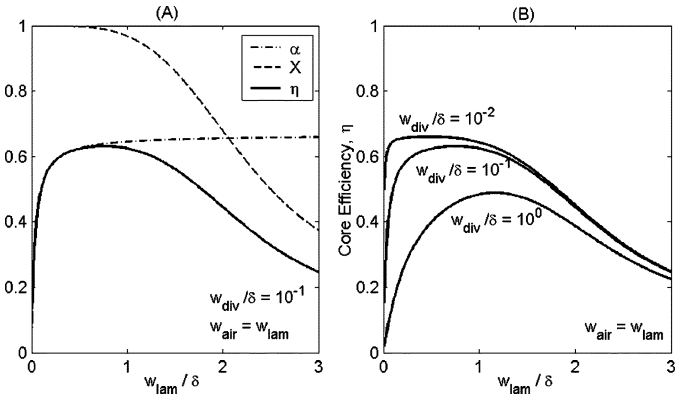

Fig. 3. Core efficiency is limited by packing density and eddy current losses. (a) Overlay of packing density α, magnetic flux efficiency X, and total core efficiency η, showing poor packing density at low $w_{\rm lam}/\delta$ and large eddy current losses at large $w_{\rm lam}/\delta$. (b) Core efficiencies η for various silicon divider widths.

The air gap is limited by electrodeposition nonuniformities caused by current crowding effects and restricted ion transport as the gap between the advancing plated layers is reduced [9]. This results in a deposit that tends to "pinch" or "key-hole," leaving a void in the center region. Pinching was limited by stopping the plating at the onset of nonuniform deposition, as indicated in Fig. 2(c). For silicon trenches of all widths, it was found empirically that the minimum air gap was approximately equal to the lamination thickness ($w_{\rm air} \approx w_{\rm lam}$). Even with these constraints, packing densities in excess of 50% were achieved.

III. Theory

The theoretical frequency dependence of the laminated core due to eddy current losses is given by [10]

$$L(f) = L_0 \mathrm{X}(\xi) = L_0 \frac{1}{\xi} \frac{\sinh\xi + \sin\xi}{\cosh\xi + \cos\xi} \quad (2)$$

where L_0 is the low-frequency (DC) inductance, and $\mathrm{X}(\xi)$ is a shaping function with frequency-dependent argument $\xi = w_{\rm lam}/\delta = w_{\rm lam}\sqrt{\mu_0\mu_r\sigma\pi f}$. Here, $w_{\rm lam}$ is the lamination width, δ is the skin depth, μ_0 is the permeability of free space, μ_r is the relative permeability of Ni-Fe, σ is the conductivity of Ni-Fe (measured 5×10^6 S/m), and f is the frequency. The cutoff frequency f_c is defined as the frequency when $w_{\rm lam} = \delta$. Therefore

$$f_c = \left(w_{\rm lam}^2 \mu_0 \mu_r \sigma \pi\right)^{-1} \quad (3)$$

and $L(f_c) = 0.968\, L_0$.

From an engineering perspective, both packing density and eddy current losses limit the total flux that can be passed through a physical core volume. The combined effect can be captured by defining a total core efficiency η, where $\eta = \alpha \mathrm{X}(\xi)$. The same shaping function $\mathrm{X}(\xi)$ defines the frequency-dependence of the flux (flux is proportional to inductance). The core efficiency can be interpreted as the percentage of "useful" flux-carrying volume within the total space occupied by the laminated, lossy core. As shown in Fig. 3(a), there is an optimal lamination

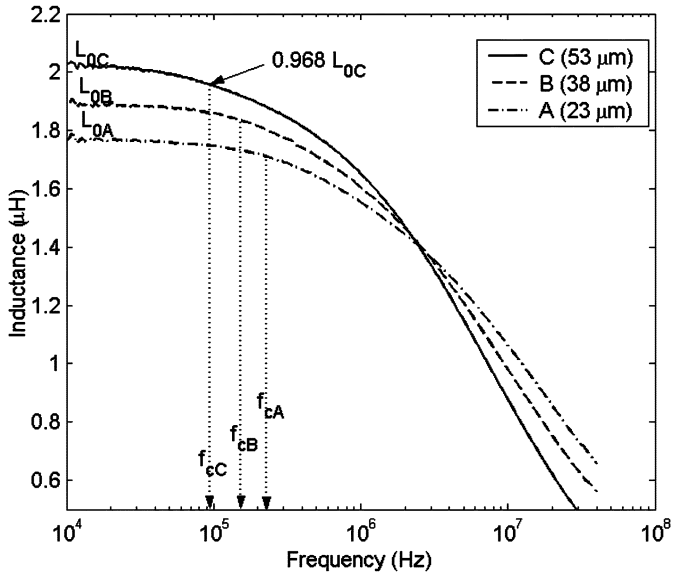

Fig. 4. Inductance versus frequency for three samples of increasing lamination thickness (and increasing packing density). The key parameters for each curve are the low-frequency (DC) inductance L_0 and cutoff frequency f_c (at frequency f_c, $L(f_c) = 0.968\ L_0$).

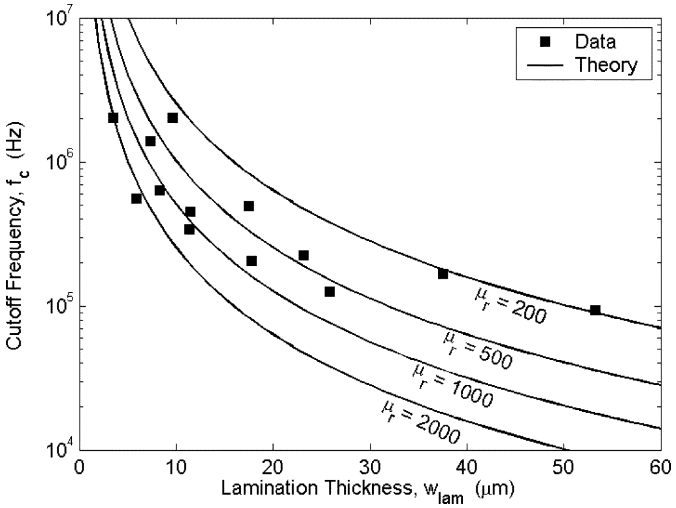

Fig. 5. Measured cutoff frequencies f_c decrease with lamination thickness $w_{\rm lam}$. Theoretical cutoff frequencies (assuming constant relative permeabilities of 200, 500, 1000, and 2000) are shown for reference.

thickness to maximize the core efficiency. Very thin laminations have low packing density, but very thick laminations have large eddy current losses. Fig. 3(b) shows the core efficiencies for various silicon divider widths.

IV. Characterization

To verify that vertically laminated Ni-Fe cores are effective in reducing eddy current losses, the impedances of the various laminated cores were measured from 10 kHz–40 MHz using a 27-turn, 3.5-mm-long, 2-mm-diameter solenoidal coil connected to an HP4194A impedance analyzer. The inductance of the coil with no core present (air core) was subtracted from the inductance of the coil with the magnetic core. This permitted analysis of the inductance contribution from only the magnetic core. The silicon skeleton of the core was assumed to have a permeability of unity and no eddy current losses. This approximation holds, as the dimensions of the silicon were smaller than the skin depth, even at 40 MHz ($\delta_{\rm Si} = 250\ \mu$m).

Fig. 4 shows the inductance of three samples (shown in Fig. 2) with increasing lamination thickness (and increasing packing density). Note the sample with the thickest laminations has the highest low-frequency inductance L_0 but the lowest cutoff frequency f_c. This procedure was repeated to extract the cutoff frequencies for all of the laminated cores.

Fig. 5 shows the cutoff frequencies plotted versus lamination thickness, along with several theoretical curves using (3) (assuming constant permeability). As predicted, the cutoff frequency decreases with increasing lamination thickness, confirming that the laminating scheme is effective in reducing eddy current losses.

V. Conclusion

Vertically laminated magnetic cores were successfully fabricated by plating Ni-Fe into etched Si trenches. Guidelines were developed to maximize the core efficiency within the constraints of fabrication. Inductance measurements showed a reduction of eddy currents for the laminated cores, verifying the fabrication approach. Although core efficiencies were limited to around 60%, this approach is useful when out-of-plane flux is required or for highly integrated or high-temperature devices.

Acknowledgment

Fabrication and testing was performed at the Georgia Tech Microelectronics Research Center (MiRC). The authors thank J.-W. Park for his valuable technical assistance.

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