Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry

C. Camperi-Ginestet, Y. W. Kim, N. M. Jokerst, M. G. Allen, and M. A. Brooke

Abstract—**A three-dimensional integration technology that electrically connects an independently optimized thin-film device layer to a Si circuitry layer is reported in this paper. An epitaxial liftoff GaAs thin-film optical detector is integrated directly on top of Si amplifier circuitry with a planarizing, insulating layer of polyimide between the detector and the circuitry. The detector is vertically connected to the circuitry below through an electrical via in the insulator. This integration technology enables monolithic, massively parallel vertical interconnection between two independently optimized device layers. Systems such as image processing arrays will significantly benefit from this massively parallel integration technology.**

INTRODUCTION

To overcome the interconnection limitation between devices in the plane of integrated circuits, massively parallel interconnection in three dimensions between planes of circuitry is necessary. This three-dimensional integration enables the parallel, simultaneous data transfer and signal processing of all data points in an array, increasing the throughput and speed of computational systems. Optical imaging arrays particularly benefit from such a vertical, parallel connection of each detector to signal processing circuitry since the input image excites all of the detectors in the array in parallel. The data from each pixel can be simultaneously processed by the circuitry directly underneath the detector, increasing the throughput of the detection system. With complex circuitry underneath the detectors, image compression can reduce the pinout of the imaging system.

Excluding chip-substrate-chip hybrid approaches such as multichip modules, there have been several previous methods proposed to accomplish vertical interconnection between devices and circuits for high throughput parallel processing. These methods include solder bump technology [1], in which two wafers are connected both electrically and mechanically by indium bump bonds; diffused aluminum wires which extend from the back to the front of a silicon wafer for interconnection of the wafer front and back side [2]; and amorphous silicon used as a photoconversion layer on top of silicon circuitry [3].

In this letter a new fabrication method for the three-dimensional integration of high-quality compound semiconductor optical detectors directly on top of silicon (Si) circuitry is described. This fabrication technique not only allows monolithic three-dimensional integration to be realized, but also enables integration of independently optimized compound semiconductor devices and silicon circuitry using standard inexpensive microfabrication techniques. Using a modified epitaxial liftoff (ELO) technique [4], a GaAs thin-film optical detector is deposited directly on top of a layer of planarizing, insulating polyimide which lies between the detector and the Si circuitry as shown schematically in Fig. 1. The detector is grown lattice matched to a GaAs substrate, separated from the substrate using selective etches, and aligned and deposited onto the polyimide coated Si circuit. Since the GaAs detector is only on the order of 1 μm thick, standard photolithography and vacuum deposition can be used to connect the detector to the Si circuit through vias in the polyimide. The standard vacuum deposited contacts used between the layers of circuitry have high mechanical and electrical reliability, the short vertical electrical connections are low capacitance, and there is no crosstalk between devices.

This integration technology has several advantages in addition to massively parallel interconnection and data processing. This integration is inexpensive and manufacturable since the Si circuitry is fabricated using standard techniques with the integration added through post processing which does not impact the Si fabrication technology. Also, a variety of different, independently optimized compound semiconductor devices can be deposited onto the same host circuitry with minimal added fabrication complexity. This is in stark contrast to direct growth technologies for three-dimensional integration, which currently require a separate growth for each type of compound semiconductor device, coupled with high growth temperatures for extended periods, which may degrade the performance of the Si circuitry. Systems constructed using this integration technology can be high performance since the circuitry and compound semiconductor devices can be independently optimized, and high yield since the

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The authors are with the School of Electrical Engineering, Microelectronics Research Center, Georgia Institute of Technology, Atlanta, GA 30332.

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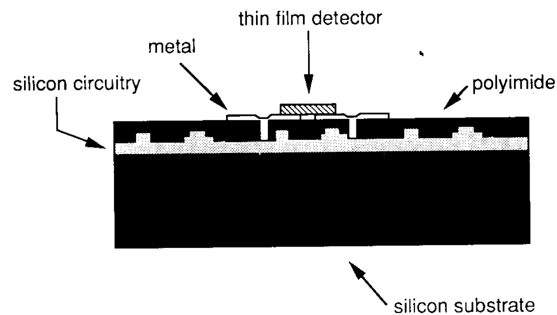

Fig. 1. Schematic of the three-dimensional integrated circuit showing the polyimide planarized silicon circuit with the thin-film detector integrated on top of the insulating polyimide. A metal-filled via in the polyimide provides electrical connection between the detector and the silicon circuit.

circuitry and compound semiconductor devices can be independently tested prior to integration. Using this three-dimensional integration technique coupled with the alignment and deposition of arrays of compound semiconductor devices [4], each device in arrays of thin film devices can be connected to Si circuitry for massively parallel processing. In addition, through the alignment and deposition of subarrays of devices, larger arrays can be formed, thus eliminating the need for the uniform growth of devices on the wafer scale for wafer-scale integration of devices such as detectors for imaging arrays. Finally, for imaging arrays, high detector fill factors are possible since the surface of a detector array fabricated using this vertical integration technology will consist entirely of detectors with the unilluminated Si data processing circuitry located directly underneath the detectors.

Fabrication

To demonstrate a three dimensional integrated circuit, a gallium arsenide (GaAs) metal–semiconductor–metal (MSM) detector was integrated directly on top of a silicon circuit. The silicon circuit is a simple transresistance amplifier consisting of three MOS inverters operating in the subthreshold regime [5]. This type of low power circuit is adequate for many image processing tasks which require highly parallel processing without high individual pixel processing speed. No attempt was made to optimize either the circuit or the detector; the point of this reported effort was the first demonstration of this new three dimensional integration technology.

To integrate the circuit and detector, the fully fabricated circuit was spin coated with 5 μm of polyimide (DuPont PI-2611), baked at 130°C in air for 20 min, and cured at 300°C in nitrogen for 1 h. This polyimide deposition and thermal processing is standardly performed on Si circuitry for multilevel interconnect and has been shown not to affect the performance of the Si circuit. A titanium mask 150 nm thick was then vacuum deposited onto the polyimide. Using standard photolithography, 100×100 μm vias were defined in this mask. The vias were transferred to the polyimide using a parallel plate reactive ion etcher using 100% oxygen as the etch gas, which fully exposed the underlying Al pads on the circuit. The titanium was removed with a wet etch of $HF:HNO_3:H_2O$ 1:2:7. Gold (150 nm) was vacuum deposited on the etched substrate to electrically interconnect the underlying circuit to the top of the polyimide. The gold was then patterned into 2 μm wide interdigitated "fingers" for subsequent connection to the MSM.

To obtain the high-quality, single-crystal thin-film GaAs devices necessary for this three-dimensional integration, epitaxial liftoff (ELO) was employed. This technique utilizes the high etch selectivity between high Al concentration $Al_xGa_{1-x}As$ materials and low Al concentration alloys [7] to separate single crystal epitaxial material and devices from the lattice matched growth substrate. For this letter, a 200 nm lattice matched sacrificial etch layer of AlAs followed by a 1 μm layer of the GaAs (used to form the MSM detector) were grown lattice matched to a GaAs substrate. A mesa etch was used to define an array of GaAs epitaxial devices which were then separated from the substrate through a sacrificial etch of the AlAs in $HF:H_2O$ (1:10). The array of 100×100 μm GaAs devices was then transferred to a transparent polyimide diaphragm for alignable and selective deposition [4] onto the polyimide-planarized Si circuit. Note that these thin film devices can be deposited onto any smooth host substrate without the lattice-matching condition required for direct growth. When the GaAs was deposited onto the host substrate, it was van der Waals bonded onto the Au fingers on the polyimide to form the MSM detector. The Schottky barrier electrical contact and a stable mechanical bond between the Au and the GaAs was formed through contact bonding [6], completing the three-dimensional structure.

Tests conducted on the quality of thin-film devices fabricated using epitaxial lift-off demonstrate that this process does not affect the performance of the devices. These tests include measurements of minority carrier lifetime [7], semiconductor laser threshold current [8], and photoluminescence [9], [10]. An increase in the dark current of ELO InGaAs/InP p-i-n photodetectors has been reported [11]. This may be due to increased surface recombination at the back side of the device exposed after liftoff. The transfer diaphragm process utilized herein for ELO detectors enables coating on both sides of the devices, so back passivation can be applied to these photodetectors, thereby reducing the dark current to the on-wafer value [12].

Although a single device from the array on the transfer diaphragm was selectively deposited onto the host Si circuit, we have also simultaneously deposited an entire array of devices from the diaphragm onto Si using this transfer technique. For imaging array applications, wafer-scale (six inch) integration is often desirable. Using the integration techniques described herein, arrays of detectors can be aligned and deposited (currently to within 1 μm accuracy) with respect to one another to create large

arrays, thus eliminating the need for highly uniform material growth over the entire substrate surface area, which is very difficult with current growth technology.

Results

Fig. 2 shows two photomicrographs of the fabricated structure. Fig. 2(a) shows the planarized and metallized circuit prior to the MSM deposition with a closeup of the finger region, and illustrates the excellent planarizing properties of the polyimide. Fig. 2(b) is a photomicrograph of the fully fabricated device, with the GaAs on top of the metal fingers shown in Fig. 2(a). No difficulty in alignment, deposition, or bonding of the MSM was observed. The magnitude and durability of both the mechanical bond strength as well as the electrical connection of the MSM is the subject of current study, although no device failures have been noted in our limited testing.

The response of the three dimensional integrated circuit was tested using pulsed (square wave) 850 nm laser light from a Hewlett Packard HP8153A lightwave multimeter delivered through an optical fiber directly to the MSM. No illumination of the surrounding circuit occurred during this test. The measured response to a 1 kHz input optical square wave is shown in Fig. 3. The output of the amplifier circuit closely followed the input light signal. This performance is typical for these types of low power subthreshold amplifier circuits.

Several tests were performed in order to verify that the output of the circuit was due exclusively to the response of the MSM detector. Deliberate improper biasing of the electrical circuit produced no output signal. Likewise, when the input optical signal was moved from MSM to the adjacent Si circuitry, no output signal was observed. These results indicate that only optical signals detected by the MSM were amplified and appeared at the output, and that the amplifier circuit, interconnections, and MSM are all operating properly, thus demonstrating this new vertical three dimensional integration technology.

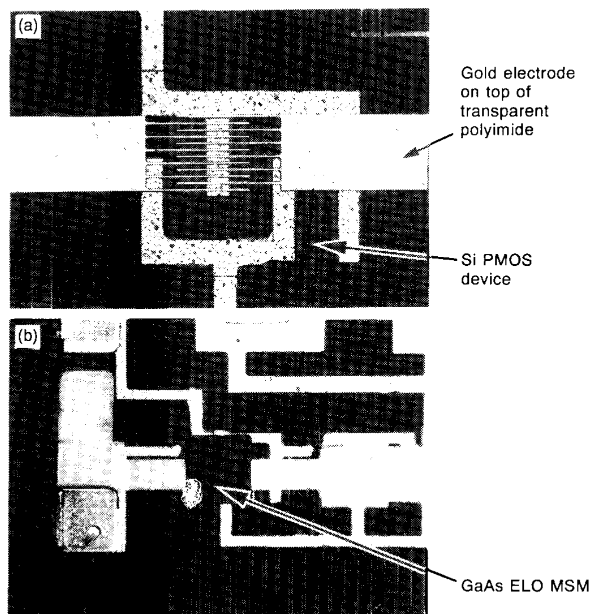

Fig. 2. Photographs of the fabricated three-dimensional vertical integration. The Si amplifier circuit has been planarized with insulating polyimide. Vias 100 × 100 μm have been etched in the polyimide over the bonding pads in the Si circuit. Gold contacts have been deposited on top of this polyimide to form the MSM fingers and to connect the Si circuit to the MSM through the vias in the polyimide. (a) A close-up view of the MSM metal fingers which lie directly above the Si circuitry with a layer of polyimide between the fingers and the Si circuitry. (b) The final three-dimensional vertically integrated device. The GaAs ELO material has been contact bonded to the Au MSM fingers shown in (a), resulting in an MSM photodetector.

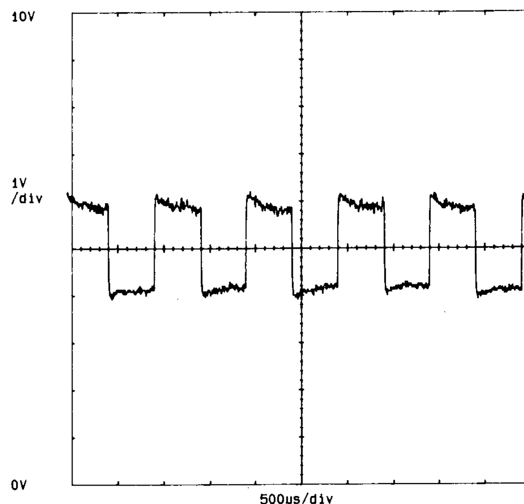

Fig. 3. Measured output voltage of the three-dimensional vertically integrated circuit to a square wave 1 kHz optical input.

Conclusions

In this letter we report the three-dimensional integration and test of a GaAs epitaxial liftoff thin-film MSM detector directly on top of silicon amplifier circuitry with a planarizing, insulating layer of polyimide between the detector and the circuitry. The detector is vertically interconnected to the circuit below through a via in the polyimide. The underlying circuit is a transresistance amplifier which shows output swings on the order of volts in response to optical excitation of the MSM. This work demonstrates parallel, vertical interconnection between planes of devices, which may lead to massive parallel processing of data and images from vertically connected device arrays such as image processing systems.

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Extremely Large Band Gap Shifts for MQW Structures by Selective Epitaxy on SiO_2 Masked Substrates

C. H. Joyner, S. Chandrasekhar, J. W. Sulhoff, and A. G. Dentai

***Abstract*—We investigate selective epitaxy through SiO_2 masks of varied geometry with the goal of making planar photonic integrated circuits. The InGaAs / InP, InGaAsP / InP, and InGaAs / InGaAsP MQW material systems are studied with atmospheric and 100 torr MOVPE. Extremely large band gap shifts (136 meV) may be achieved, more than enough to allow construction of lasers, modulators, and low loss waveguides in a single plane.**

In order to reduce cost and improve optical functionality per unit surface area on semiconductor substrates, photonic integrated circuits (PIC's) are being studied. Recently, growth over masked substrates has been proposed as a possible solution to the problems of photonic integration [1]–[4] because it allows variation of the band gap of multiquantum well (MQW) material in the same plane with a single growth. Previously, researchers have reported the effects of varying mask width for a single gap [1] or for very wide mask openings where the band shifting effect is small [2], [5], [6]. The limits to which the technique can be pushed to produce a wide variety of integrated waveguide devices in the same plane had yet to be determined. In this letter we will present an evaluation of this technique for a wide variety of mask widths and gaps using both atmospheric and low pressure metalorganic vapor phase epitaxy (MOVPE) for the InGaAs/InP, InGaAsP/InP, and InGaAs/InGaAsP material systems on InP substrates masked with SiO_2.

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The authors are with AT & T Bell Laboratories, Crawford Hill Labs., Holmdel, NJ 07733.
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The concept of band gap control by selective area growth of quantum wells (QW's) through masks is straightforward. Source material arriving from the gas phase will grow epitaxially in regions where the mask is open. Where source material lands on SiO_2 it will not readily nucleate. If the growth temperature is high enough and the mask width is narrow enough most of the source species deposited on the mask will reenter the gas phase and diffuse, due to the local concentration gradient, to find an unmasked region [7]. Compared to a completely unmasked substrate, the QW growth which occurs through a mask for both InGaAs and InGaAsP epilayers will be thicker [8] and richer in In [6], [9] due to the relative diffusion coefficients of In and Ga under typical MOVPE growth conditions. Thus, from both the quantum-size effect and the change in alloy composition, the QW's in the gap are shifted to lower energy band gaps than regions far from the mask.

Fig. 1 gives the geometry and dimensional variations of our mask. The patterns were spaced 250 μm apart. We find that by keeping the mask width under 20 μm and the amount of masked area on the substrate to a minimum, no polycrystalline growth on the SiO_2 for any growth