Tunable Ferroelectric Capacitor with Low-Loss Electrodes Fabricated Using Reverse Side Exposure

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Abstract

This work describes the fabrication of a highly-tunable capacitor based on barium strontium titanate (BST:$Ba_XSr_{1-X}TiO_3$) ferroelectric thin films which have been deposited and/or epitaxially grown on transparent sapphire substrates. The fabrication of the capacitor relies on same-surface interdigitated electrodes. A critical challenge in the fabrication of these devices is maintaining narrow gaps for high tunability, while simultaneously forming thick electrodes to minimize RF loss. In this paper, a single mask process and a repeatable self-alignment technique using reverse side exposure through the transparent substrate are employed to achieve both of these goals. A single-finger test capacitor with an electrode gap of 1.2μm and an electrode thickness of 2.2 μm was fabricated using this process. Tunability ($T=100\times(C_0-C_{bias})/C_0$) of 33% at 10V and 54% at 30V has been achieved at 100kHz. To demonstrate the scalability of this process, an 102-finger interdigitated capacitor is fabricated and characterized at 100kHz and 1GHz. The structure is finally embedded in a 25μm thick polymer (SU-8) for passivation. Quality factor decrease of 15~25%, tunability decrease of 2~3%, and capacitance increase of 6% are observed due to SU-8 passivation. The capacitor shows 15.9pF of capacitance, 28.1% of tunability at 10V, and quality factor of 16 (at 10 V bias) at 1GHz.

Introduction

Tunable capacitors using high dielectric constant ferroelectric materials have been utilized in many microwave devices for several years, such as, phase shifters, filters, phased array antennas, etc. [1-5]. For practical usage of ferroelectric varactors, it is desirable to have large tunability as well as low device losses. One capacitor architeture that could achieve these goals is to fabricate interdigitated electrodes on deposited or epitaxially-grown high dielectric constant ferroelectric layers such as, strontium titanate (STO) or barium strontium titanate (BST). As for the ferroelectric material deposition, there are several methods reported (RF sputtering, MOCVD, CCVD, sol-gel, or pulsed laser ablation etc.) [6-10] and the electrical properties of tunable devices are known to vary with each method.

Metallization and subsequent patterning by photolithography is a key step in the fabrication of gap capacitors (i.e., capacitors formed by deposition of metal on a single side of a BST film). Thus, the electrical performance

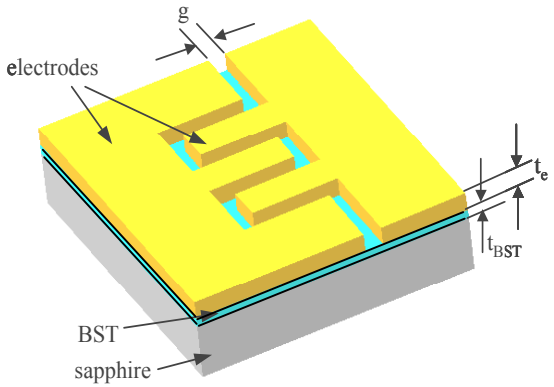


Fig. 1 *Structural schematic of an interdigitated gap capacitor on barium strontium titanate (BST) on sapphire substrate.*

of an interdigitated gap capacitor is also dependent on the electrode patterning and its geometry. Because the dielectric tunability of a ferroelectric capacitor depends on electric field, small gaps between electrodes are necessary for high tunability for a given bias voltage. A thick electrode compared to the skin depth at the frequency of interest is also preferred for reducing RF conductor loss. However, in general it is difficult to fabricate tall and narrow gap electrodes due to the difficulty of forming high aspect ratio photoresist molds with the required pattern resolution. Therefore, a critical challenge in the fabrication of these same-surface interdigitated electrodes is maintaining narrow gaps for high tunability, while simultaneously forming thick electrodes to minimize RF loss.

In this paper, we describe the fabrication of a highly-tunable capacitor based on barium strontium titanate (BST:$Ba_xSr_{1-x}TiO_3$) ferroelectric thin films which have been epitaxially grown on transparent sapphire substrates. A single mask process and a repeatable self-alignment technique using reverse side exposure through the transparent substrate are employed to achieve both narrow gaps and thick electrodes. An additional benefit of the process is that the BST is passivated from aggressive processing conditions, thereby maintaining its properties.

Theory

Figure 1 shows a structural schematic of an interdigitated gap capacitor architecture. Two electrodes with thickness t_e and gap g are formed on top of high dielectric constant ferroelectric BST which has been epitaxially grown on a sapphire substrate.

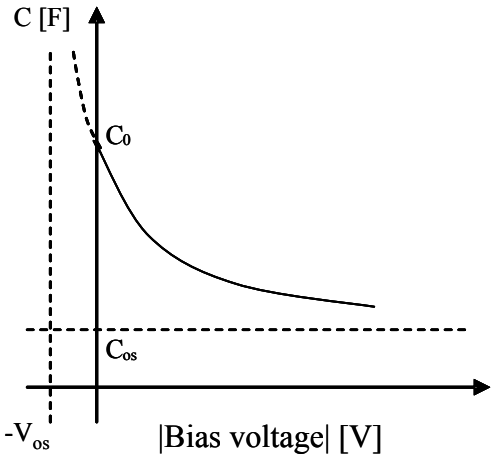


Fig. 2 *Schematic of capacitance as a function of bias voltage.*

Capacitance as a function of bias voltage – Over some portions of its range, the capacitance of the ferroelectric gap capacitor typically decreases with bias voltage with a hyperbolic curve dependence ($C \propto 1/V$) as shown in Figure 2. Since the capacitance of the gap capacitor is insensitive to the polarity of the bias voltage, it is axisymmetrically plotted with respect to the y-axis. The voltage-dependent capacitance $C(V)$ and tunability $T(V)$ ($T=100\times(C_0-C_{bias})/C_0$) can be defined as Equations (1) and (2), respectively.

$$C(V) = C_{os} + \frac{k}{|V| + V_{os}} \tag{1}$$

$$T(V) = \left| \frac{C(0) - C(V)}{C(0)} \right| \times 100 = \left| 1 - \frac{C_{os}}{C(0)} - \frac{k / C(0)}{|V| + V_{os}} \right| \times 100 \tag{2}$$

where C_{os} is non-voltage dependent offset capacitance, k is a coefficient of the hyperbolic function, $|V|$ is the magnitude of the biasing voltage, and V_{os} an offset voltage to give a finite capacitance value at zero bias voltage. The coefficients (C_{os}, k, and V_{os}) can be empirically determined.

Capacitance as a function of gap - Since a gap capacitor fabricated on a high dielectric constant layer is storing electric energy mostly in the dielectric underneath the gap area, its capacitance is greatly affected by the fringing field between the electrodes through the dielectric. Unlike the case of the parallel plate capacitor, the dependence of the capacitance on geometry and dielectric constant is not analytically straightforward. The capacitance for the gap capacitor, however, might be postulated over some range as shown in Equation (3):

$$C(g) = \varepsilon_0 \varepsilon_r \frac{\alpha \cdot t}{g^{\beta}} \tag{3}$$

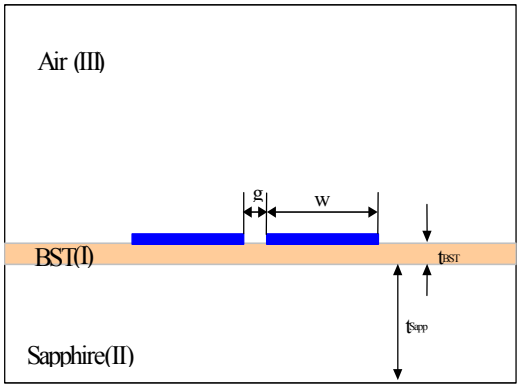


Fig. 3 *Capacitor geometry for 2D electric analysis.*

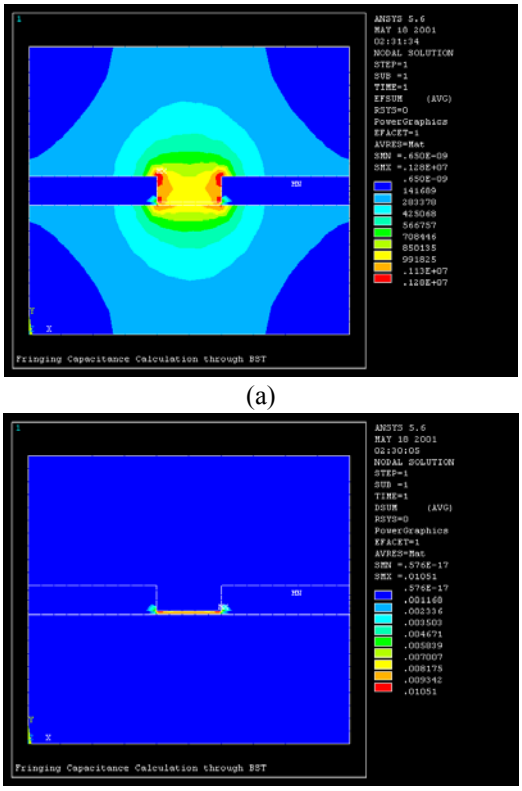


Fig. 4 *Magnified view of electric field and electric displacement distribution in gap area with 5μm gap; (a) electric field ($|\bar{E}|$), (b) electric displacement ($\varepsilon|\bar{E}|$) (ANSYS 5.6).*

where α is an effective coupling length, t the thickness of the dielectric layer, g the gap between the electrodes, and β an effective power factor.

Finite element analysis (ANSYS 5.6) is used in order to numercally determine α and β for a given capacitor geometry. The geometry used for two-dimensional electrostatic simulation is shown in Fig. 3 with the following parameters:

Relative permittivity of air ε_{air} : 1
Relative permittivity of sapphire ε_{sapp} : 10
Relative permittivity of BST ε_{BST}: 500~1000
Thickness of BST t_{BST} : 0.5μm
Width of electrode w : 500μm
Gap g : 0.5μm ~ 20μm

Electric field and electric displacement in the gap area are shown in Figure 4. While a strong electric field is concentrated on the gap area symmetrically between electrodes regardless of the upper air region and underlying substrate region as shown in Figure 4a, strong electric displacement is displayed only in the high dielectric BST layer of the gap area in Figure 4b. More than 80% of the total strored electric energy in the capacitor is attributed to that area alone when the relative permittivity of BST ε_{BST} is 800 and the gap g is 2μm.

When the upper region is covered with a dielectric material (e.g., as might happen during passivation and subsequent packaging, resulting in an embedded capacitor), the capacitance increases due to the contribution of the dielctric material. Figure 5 shows the capacitance as a function of gap in two cases; one without passivation (air ambient) and with passivation (SU-8 embedded, ε_{SU-8} ~3.5). The capacitance with dielectric passivation shows a 2~10% increase with a 2~20μm gap.

Quality factor - In general, practical passive components (e.g., R, L, and C) are not ideal, and can be modeled with a combination of complex impedance with unwanted parasitics. Specifically, a practical capacitor includes unwanted inductance, resistance, and dielectric absorption and can be schematically drawn as shown in Figure 6, where C is ideal capacitance, R_p parallel resistance representing dielectric loss, R_{esr} equivalent series resistance, and L_s series parasitic inductance.

The total impedance is written in Equation (4)

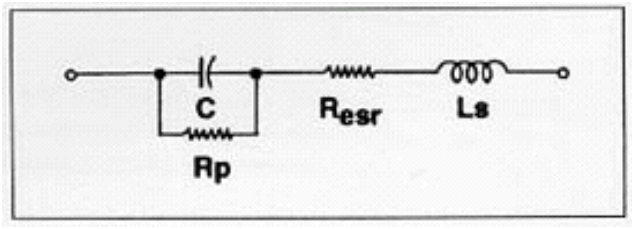


Fig. 6 *Equivalent circuit for a gap capacitor.*

$$Z = \mathrm{Re}(Z) + j\,\mathrm{Im}(Z) \tag{4}$$

where

$$\mathrm{Re}(Z) = \frac{R_p + R_{esr} + \omega^2 C^2 R_p{}^2 R_{esr}}{1 + \omega^2 C^2 R_p{}^2},$$
$$\mathrm{Im}(Z) = \frac{-\omega C R_p{}^2 + \omega L_s + \omega^3 L_s C^2 R_p{}^2}{1 + \omega^2 C^2 R_p{}^2} \tag{5}$$

The quality factor Q is defined as the ratio of the energy stored in the device to energy dissipated per cycle. It is easily calculated for passive components in Equation (6) if the complex impedances are known:

$$Q = -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{6}$$

In the high frequency region, the real part of impedance *Re(Z)* is dominated by R_{esr} while the imaginary part *Im(Z)* is approximated as $-1/\omega C$ as long as the operating frequency is below its resonant frequency and series inductance L_s is very small. Therefore, high Q-factor can be achieved by surpressing the equivalent series resistance R_{esr} existing in the frequency range of interest.

Equivalent series resistance R_{esr} in the RF range consists of DC resistance, RF resistance, and contact resistance, etc.. DC resistance and metal contact resistance are independent of frequency whereas RF resistance is a frequency-dependent function due to the skin effect at high frequency. In order to minimize RF resistance, the conductors for RF devices should be designed to be on the order of the skin depth at the frequency of interest. Thicker conductors do not yield much additional benefit, and have the additional cost of difficult fabrication for thick conductor structure.

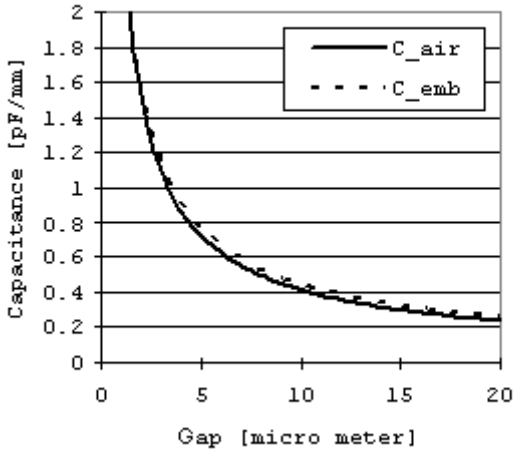


Fig. 5 *Capacitance as a function of gap; solid line shows without embedding and dashed line shows the effect of embedding of SU-8*

Fabrication

In order to reduce RF conductor loss, the electrode thickness t_e is targeted to be 2μm, which is about one skin depth of copper at 1GHz. For high tunability at a given bias voltage, the gap g should be small, and is targeted to 1~2μm in width. The fabrication process is shown in Figure 7. This process is based on back-side exposure (which is enabled by the substrates and deposition method for the BST), and allows for the fabrication of thick metal electrodes while simultaneously maintaining small electrode gaps. BST is epitaxially grown to a thickness of 0.5μm on single-crystal alumina sapphire substrates using combustion chemical vapor deposition (CCVD). This technique allows epitaxial growth of BST in non-vacuum conditions. Negative tone photoresist

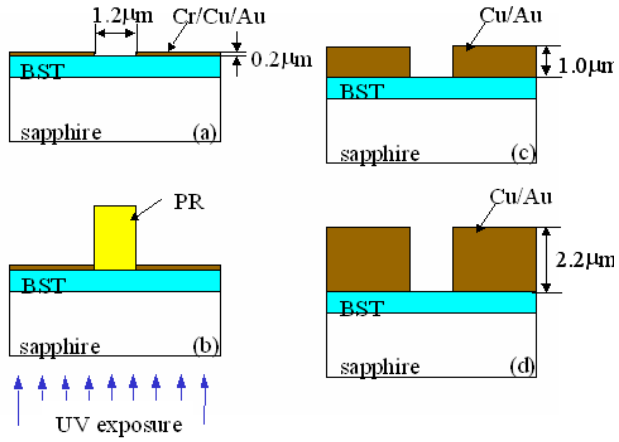


Fig. 7 *Fabrication process.*

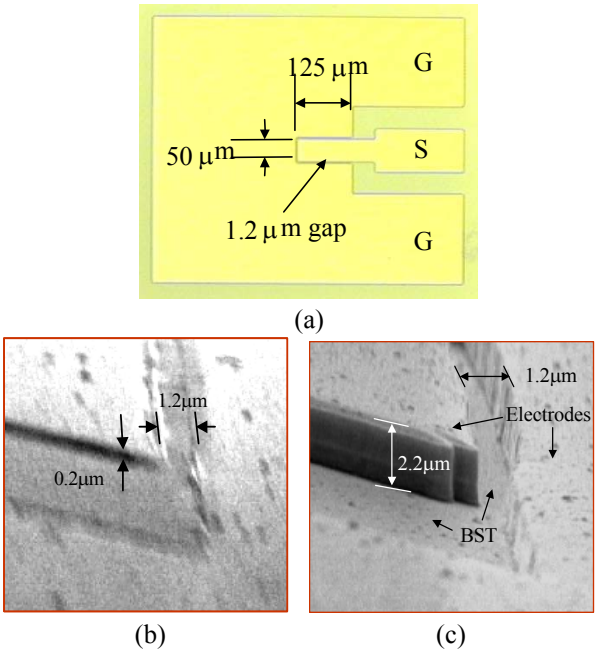


Fig. 8 *A fabricated single digit gap capacitor; (a) 1.2μm gap and 300μm coupling length, (b) SEM picture of gap area after the first lift-off (0.2μm thick metal), (c) after the third lift-off (2.2μm thick metal).*

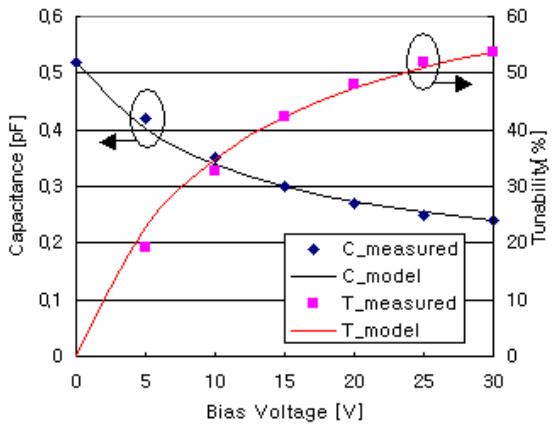


Fig. 9 *Capacitance and tunability of single digit gap capacitor (1.2μm gap and 300μm coupling length) structure.*

(NR9_1000PY, Futurrex, Inc.) is spin-coated on the BST film and patterned. In a lift-off process, first metal layers (Cr/Cu/Au, 20nm/200nm/30nm) are deposited and the photoresist removed (7a). Chromium is used as an adhesion layer between the substrate and the subsequent copper layer, and the top gold layer is employed for oxidation protection. A second negative photoresist (NR9_1500, Futurrex, Inc.) is then spin-coated and baked. The photoresist is then exposed from the reverse side. Since the sapphire substrate is transparent, and the first metal layer is opaque, a self-aligned mold is opened in the negative photoresist over the first deposited metal layer (7b). This mold can then be filled either using electroplating or subsequent lift-off steps to create thick, self-aligned electrodes. In this work, multiple lift-off processes are employed. Ti/Cu/Au (20nm/800nm/30nm) is deposited using a standard lift-off process followed by photoresist removal (7c). A third metallization of Ti/Cu/Au (20nm/1μm/200nm) and lift-off has been done to further increase metal thickness and the fabrication is complete (7d).

A fabricated single digit gap capacitor with 300μm coupling length is shown in Figure 8a, yielding 1.2μm gap and 0.2μm thickness after the first lift-off (Figure 8b), and 1.2μm gap and 2.2 μm thickness (1.8:1 gap aspect ratio) after the third lift-off process (Figure 8c).

Measurement and characterization of single digit capacitor

The impedance of the fabricated gap capacitors is measured with a Keithley 3322 LCZ meter at 100kHz. The capacitance and its tunability as a function of dc bias voltage for the capactitor of Figure 8a (2.2μm thickness) are plotted in Figure 9. The coefficients (C_{os}, k, and V_{os}) are empirically determined with the measurement data from at least three different voltages. Capacitance and tunability from Equation (1) and (2) for the Figure 8a device are plotted also in Figure 9. Modeling curves show good agreement with the measurement data throughout the voltage range (0~30V). The coefficients used for the plot are summarized in Table 1.

Table 1. *Coefficients for capacitance and tunability curves*

	C_{os} [pF]	k [pF• V]	V_{os} [V]
Capacitor in Fig. 3a	0.135	4.33	11.24

Also, several capacitors with various gaps (1.2μm, 2.5μm, 5μm, 10μm, and 20μm) have been fabricated and their impedence is measured at zero and 30 volts. Figure 10 shows the capacitance and tunability as a function of the gap. A solid line, square marks, and diamond marks represent the simulated capacitance with zero bias voltage, measured capacitance with zero bias, and measured capacitance at 30V bias, respectively. Note that the fabricated samples have their capacitance converted to capacitance per unit length (pF/mm) in order to compare with simulation results. The solid curve in

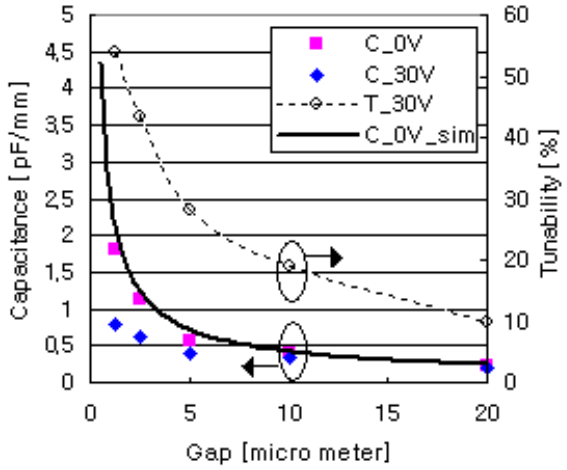


Fig. 10 *Capacitance and tunability according to gap; filled squares and diamonds show measured capacitance, a solid line does simulated capacitance, and a dashed line with empty circles does tunability at 30V.*

Figure 10 is the best fit from Equation (7):

$$C(g) = \frac{2.531}{g^{0.782}} \text{ [pF/mm]} \qquad (7)$$

where g is in μm. By comparison of Equation (3) and (7) with proper unit conversion, α and β are determined to be 0.714m and 0.782, respectively.

It is observed that a capacitor with a narrower gap shows a larger capacitance value than wider gap devices, and that its percentage capacitance changes for a given bias voltage show a similar trend as well. Tunability benefits from a narrow gap as expected.

The skin depth of copper at 1GHz is about 2μm thick and the copper electrodes for the test gap capacitors are 2.2μm thick. Two gap capacitors (one with 0.2μm thick electrodes in Figure 8b and the other with 2.2μm thick electrodes in Figure 8c) have been tested in the frequency range between 100MHz and 5GHz to investigate the effect of electrode thickness on Q-factor.

One-port scattering parameters are taken using an HP 8510 Vector Network Analyzer and Cascode G-S-G probe systems after standard calibration. S-parameters are converted to Z- parameters and the Q-factors are calculated using Equation (6). The resultant data are plotted in Figure 11, where the square marks and the diamond marks represent Q-factors of the 0.2μm and 2.2μm thick electrode capacitors, respectively.

By fitting Q values from Equation (5) and (6) to those from measurement in the frequency range 1GHz through 5GHz (solid lines in Figure 11), the lumped parameters in Figure 6 are determined and summarized in Table 2. The equivalent series resistance R_{esr} for the 2.2μm device is smaller than that of the 0.2μm device, resulting in Q-factor improvement.

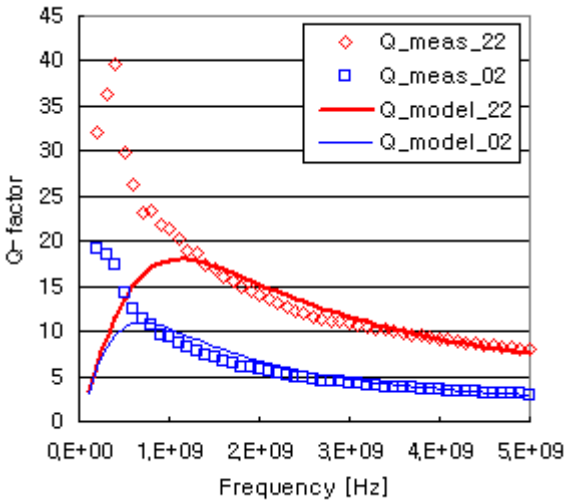


Fig. 11 *Quality factor of gap capacitors with two different metal thicknesses; diamonds and squares represent Q-factors for 2.2μm thick capacitor and 0.2μm thick one, respectively.*

Table 2. *Lumped parameters used for Q-factor calculation*

	C[pF]	R_p[Ω]	L_s[nH]	R_{esr} [Ω]	Qmeasured at 1GHz
0.2μm device	0.52	10^4	0.02	20.5	9.32
2.2μm device	0.52	10^4	0.02	7.7	21.5

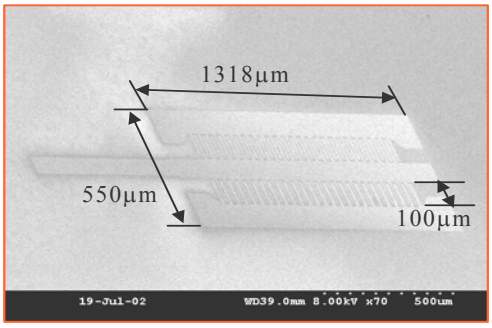
Multi-interdigitated capacitor

Based on the initial test structures above, a 102-finger interdigitated capacitor has been fabricated to demonstrate the scalability of the proposed process to large capacitance. This sturucture is finally embedded in SU-8 epoxy for passivation.

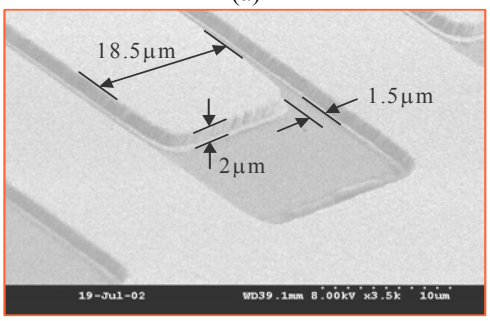
Since the thick conductor process is using a self-alignment technique, increasing to a multiple interdigitated structure does not increase process complexity. The capacitor is a

coplanar waveguide type gap capacitor having 51-finger electrodes 100μm long, 18.5μm wide, and 2μm thick between signal conductors and each ground conductor. Figure 12 shows SEM pictures of the capacitor prior to its embedding in SU-8). The overall dimension of the capacitor is 1318μm x 550μm and the gap is 1.5μm.

Capacitance, tunability, and Q-factor as a function of bias voltage of the non-embedded capacitor and the passivated, embedded capacitor are shown in Figure 13. Before passivation, the capacitor shows 17.8pF of capacitance at 0V bias, 33% tunability at 10V bias, and a quality factor of 46 at 10V bias. The voltage dependence of the capacitor can be expressed as in Equation (1) with the coefficients in Table 3.



(a)



(b)

Fig. 12 *SEM picture for a 102-finger interdigitated capacitor before embedding; (a) overall view, (b) magnified view.*

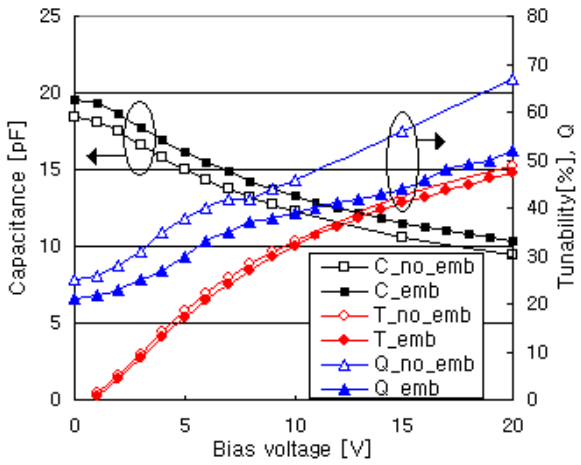


Fig. 13 *Capacitance, tunability, and Q-factor vs. bias voltage for a 102-finger interdigitated capacitor at 100kHz.*

Table 3. *Coefficients for capacitance and tunability of 102-finger interdigitated capacitor*

	C_{os} [pF]	k [pF• V]	V_{os} [V]
Capacitor in Fig. 12	0.45	350	19.52

Tunability at 10V using Equation (2) and the coefficients in Table 3 is about 31%, in good agreement with measurement. Also, the capacitance using Equation (7) for a gap of 1.5μm is 1.84pF/mm. If this result is multiplied by total coupling length (≅10mm), it is equal to approximately 18.4pF, which is also in good agreement with measurement.

The structure is embedded in a 25μm thick SU-8 epoxy

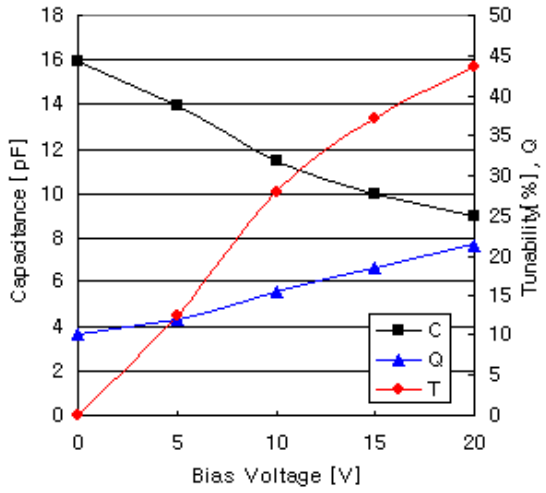


Fig. 14 *Capacitance, tunability, and Q-factor vs. bias voltage for a 102-interdigited capacitor at 1GHz.*

layer for passivation with pad openings for probing. After embedding, a slight degradation in Q-factor and tunability is observed, resulting from additional dielectric loss due to the SU-8 layer and non-tuning SU-8 material between the electrodes, while the overall capacitance is slightly increased due to additional dielectric contribution from the SU-8. The capacitor demonstrates a capacitance of 18.9pF, tunability of 32% at 10V, and a quality factor of 39 (at 10 V bias). In the range of 0~20V bias voltage, a quality factor decrease of 15~25%, tunability decrease of 2~3%, and capacitance increase of 6% are observed due to SU-8 passivation in Figure 13. In the previous theory section, we have shown the presence of SU-8 increases the capacitance by 2~10% in Figure 5, which shows an appropriate trend of capacitance increase due to dielectric passivation. All measurements in Figure 13 were performed at a frequency of 100 kHz.

Also the embedded structure has been characterized at 1GHz for RF application. It shows 15.9pF of capacitance, 28.1% of tunability at 10V, and quality factor of 16 (at 10 V bias) in Figure 14.

Conclusions

Interdigitated gap capacitors with thick low-loss electrodes fabricated using reverse side exposure on a transparent BST/sapphire substrate are demonstrated and tested at both low frequency and high frequency. A single-finger test capacitor with an electrode gap of 1.2μm and an electrode thickness of 2.2 μm was fabricated using this process. Tunability ($T=100\times(C_0-C_{bias})/C_0$) of 33% at 10V and 54% at 30V has been achieved at 100kHz

Capacitance and Q-factor as functions of voltage and gap have been characterized for the fabricated interdigited gap capacitors. A hyperbolic curve model for voltage dependent capacitance is used and it represents the capacitance trend well. Gap dependence of capacitance for interdigitated capacitors differs from that of the parallel gap and its dependence has been determined using numerical analysis (ANSYS) and measurement data. Q-factors for two capacitors with different thickness (0.2μm and 2.2μm) have been calculated from S-parameter measurement between 100MHz and 5GHz. The Q-factors at 1GHz are 21.5 and 9.32 for the 2.2μm thick device and 0.2μm thick one, respectively. The capacitor with thick electrode fabricated from the proposed fabrication process shows Q-factor improvement from its RF loss reduction.

A 102-finger interdigitated capacitor has been fabricated, embedded in SU-8 epoxy for passivation, and tested. After embedding, a slight degradation in properties is observed. The embedded structure has been characterized at 100kHz and at 1GHz for RF application.

Acknowledgments

Deposition of epitaxially-grown BST on sapphire was carried out at Microcoating Technologies, Inc. (MCT), Chamblee, GA (http://www.microcoating.com). Valuable technical discussions with Professor J. Steveson Kenney of Georgia Tech are acknowledged.

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