THIN FILM PROGRAMMABLE INTERCONNECT ARRAYS

by

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ABSTRACT

A new low cost material is presented for the realization of thin film programmable interconnect arrays for selective switching of chip to substrate interconnects from a high impedance state to a low impedance state. The programmable interconnect arrays are realized using a tri-level graphite-filled polyimide system as an interlayer material between metallic electrodes. The interconnects are switched from a high impedance to a low impedance state using an activation current to heat the material between the electrodes. This current causes an irreversible change of material resistivity which persists even after the current is removed. The graphite loading of the individual layers is varied in order to obtain the optimal interconnect characteristics. The characteristics of interest at this time are the dc levels of the interconnect initial resistance and the final resistance as well as the magnitude of the change in resistance between the initial and final states. Results of various layer combinations including 5/30/30, 0/18/0 and 3/3/3 wt% graphite are presented.

INTRODUCTION

A new technique is presented for the realization of thin film programmable interconnect arrays. Programmable interconnect arrays (PIAs) can be defined as an array of potential interconnect vias that can be selectively switched from a high impedance state to a low impedance state. Programmable interconnect arrays are of interest to the semiconductor industry as a means of significantly reducing the cost associated with the packaging of integrated circuits. There are several important features associated with programmable interconnect arrays. First, PIAs are of interest as a means of standardizing the packaging of integrated circuits. Package standardization is accomplished by establishing a suitable electrode array pattern which satifies the spatial requirements for the pad layouts of a particular class of integrated circuits. For each integrated circuit pad layout generated for a programmable interconnect array, only selected interconnect vias are activated based on the location of the pads on the die. The location of the electrically activated interconnect vias in the array is dependent on the particular integrated circuit being packaged. Even though only particular interconnects are utilized to provide functionality to the integrated circuit, the standard array pattern on the surface of the PIA matches the same array configuration located on the package, thus allowing for mating between the die and package. A second feature is the elimination of the wire bonding process required for conventional packaging techniques. Since the integrated circuit is electrically connected to the package through the programmable array, wire bonding is not required.

The approach investigated in this paper to realize programmable interconnect arrays involves the use of a tri-layer multi-coat thin film of graphite-filled polyimide material as an interlayer material between metallic electrodes. The graphite loading of the individual layers is varied in order to obtain the optimal interconnect characteristics. The characteristics of interest at

this time are the initial resistance and the final resistance of the interconnect vias as well as the magnitude of the change in resistance between the initial and final state. The graphite / polyimide interconnect system has several advantages. First, the programmable arrays can be realized as a post-processing step to the fabrication of the integrated circuit. Therefore, the design and performance of the device does not have to be compromised for this interconnect array technology. The fabrication process used to create the programmable arrays is simply added to the end of the existing procedure used to create the integrated circuit. Second, the PIAs are a low cost alternative in which the materials are readily available and the equipment is standard for microelectronic manufacturing facilities. The materials used for the technology are polyimide, graphite, and standard metallic electrode materials. The equipment needed includes spinning stations, low temperature ovens for polyimide curing, metallization systems, and exposure systems for patterning electrodes. The third advantage of this approach for the realization of programmable arrays is the possibility of improving device performance in the presence of electromagnetic fields. The conductive layers of the structure act as shielding layers from external fields. Similar films using metallic fillers suspended in polymer films have been investigated for use in electromagnetic shielding applications [1].

This paper presents a generic programmable interconnect array based on thin films of graphite / polyimide material. In the following sections, a brief description of the fabrication process used to create the programmable arrays is given. Also, results of testing on several tri-level system compositions is presented, where the graphite loading of the individual layers is statistically varied.

EXPERIMENTAL DEVELOPMENT

The graphite / polyimide material is composed of submicron graphite particles obtained from Johnson Matthey Electronics and DuPont PI-2555 polymide (a benzophenone tetracarboxylic dianhydride-oxydianiline / metaphenylene diamine formulation). The composite is formed by introducing various quantities (loadings) of the graphite particles into the as-received PI-2555 polyamic acid solution in N-methylpyrollidone (NMP). The materials are mixed using a ball mill rotating at 4-5 rpm. The mixing period is held for at least 72 hours at room temperature in order to insure homogeneity of the mixed composite solution. The composition of the films is based upon the weight percentages of the two constituents in the fully cured film. The weight of the polyimide in the cured film is calculated using the average percent solids of the polyimide solution. Mechanical and piezoresistive characterization of the graphite / polyimide thin films for a graphite loading range of 15 wt% to 25 wt% is described in references [2,3].

As mentioned earlier, the procedure required to realize the programmable interconnect array structures utilizes standard cleanroom equipment and materials. First, a suitable substrate is needed for the array. In this work silicon substrates are used as a test vehicle, but extension of the process to other substrates such as gallium arsenide, ceramics or other planar materials can be envisioned. Next, the bottom electrode of the structure is deposited and patterned into the desired configuration. In this work, aluminum is used as the bottom electrode material. The aluminum is patterned into a circular electrode to minimize the fringing effects of the electric field used to activate the interconnect via. The radius of the electrodes are 500 μm. After patterning of the bottom electrode, the tri-level graphite / polyimide structure is deposited on the surface of the electrodes. The graphite / polyimide material is deposited using a multicoat spin procedure. The individual layers of the tri-level system have varying amounts of graphite loading. The different loading percentages of the layers result in unique characteristics for the interconnect system. To deposit the graphite / polyimide material, a standard adhesion promoter is spun on the surface of the substrate and bottom electrode. Next, the first graphite / polyimide layer is spun at 3000 rpm

for 30 seconds using standard spin casting equipment. The first layer is then partially cured for 20 minutes at 150 °C in a conventional oven. The second and third layers of the structure are similarly deposited and soft baked. After the partial cure of the third layer is complete, the multilayer graphite / polyimide structure is fully cured at 400 °C for 45 minutes to remove the remaining solvent in the thin film. The top electrode material is then deposited and patterned into the same circular configuration as the bottom electrodes of the array. The complete planarized thin film programmable interconnect array structure is shown in Figure 1. For the test performed, aluminum is used as the top electrode material. The multilevel system will be described using the notation L1 / L2 / L3, where L1, L2, and L3 are the weight percentages of graphite in the cured film.

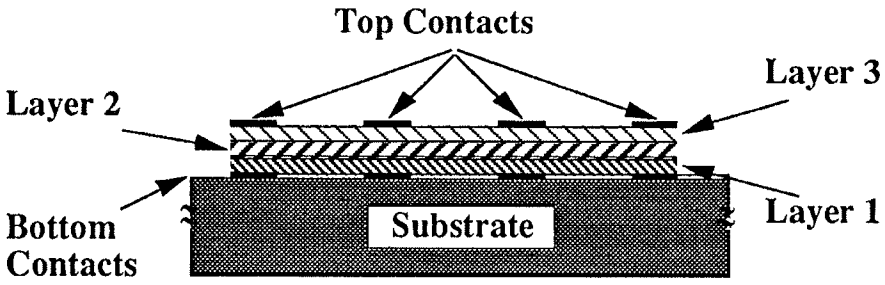

Figure 1. Cross-sectional view of the complete thin film programmable interconnect array structure. The structure consists of three layers of graphite / polyimide material with graphite loading percentages from 0 wt% to 30 wt%. The metallic electrodes were deposited on the top and bottom of the structure.

RESULTS

There were several parameters used in the characterization of the interconnect vias. The parameters of interest at this time included the graphite loading percentages for each layer of the structure, the current density used to activate the interconnect vias, the amount of time at which the current was applied to the interconnect via, and the temperature at which the test were performed. Each of these parameters were systematically varied in order to study the induced effects. Various multilevel combinations were tested with the results of the most interesting presented below.

One relevant experimental parameter which was varied during testing was the current density through the interconnect via. Variation of the applied current density during activation of the via yields information concerning the origin of the resistivity changing effect. All currents applied during testing were dc currents. The square of the current density magnitude is linearly related to the amount of heat generated through resistance losses. Therefore, if changes in the current density affect the final resistivity of the interconnect via, then there is a strong indication that the origin of the resistivity changes is dominated or at least strongly assisted by localized heating of the thermoplastic polyimide material and simultaneous translation of the graphite particles due to the radial electrodynamic force induced by the electric field through the material between the via contacts. In order to test the effect of current density on the change in the interconnect resistivity (or graphite particle mobility), two seperate current densities were used to close the via connection. Current densities of 6.4 mA/mm^2 (5 mA for a 1.0 mm circular electrode) and 127.3 mA/mm^2 (100 mA for a 1.0 mm circular electrode) were applied to the vias from the

same array for a period of 5 seconds. Several multilevel interconnect system were tested with similar results. For example, results of testing on a sample with a composition of 5/30/30 is shown in Figure 2. As can be seen from Figure 2, the change in resisitivity encountered during activation of the interconnect via is dependent of the amount of current applied. This implies that localized resistive heating of the composite material is one of the main effects leading to the lowering of the via resistivity.

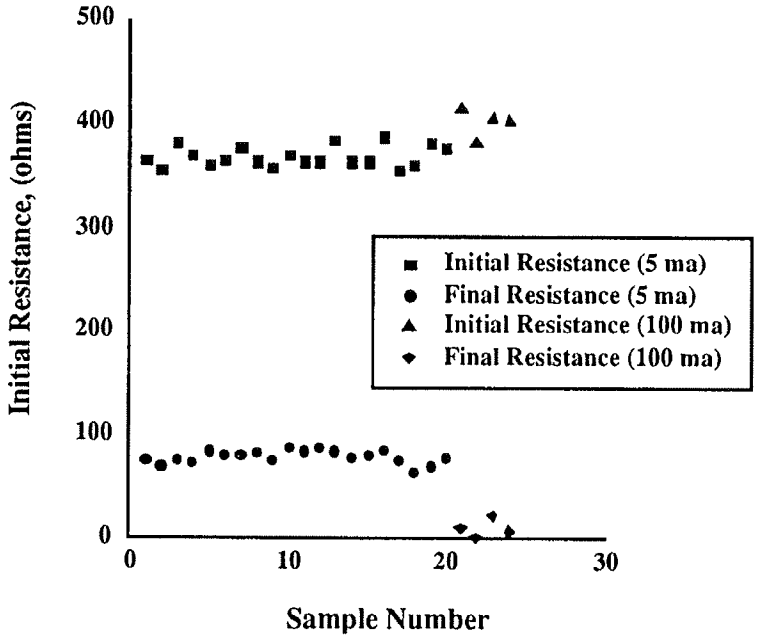

Figure 2. Change in resistance after the activation current was applied to an interconnect structure with layer compositions of 5/30/30. As the current was increased, the change in resistance also increased.

Another relevant parameter in the via activation process is the duration of the applied current density. Several different time intervals were tested for a current density of 6.4 mA/mm^2. The activation times included single periods of 3 seconds, 5 seconds, 10 seconds, and 60 seconds. Results of these tests concluded that the final resistivity of the via connection was independent of the activation time period for the times tested. There was negligible change in the final resistivity of the interconnect for samples with varying activation periods. Periods shorter than 3 seconds were not investigated.

Another important parameter in the design of the trilevel interonnect system is the graphite loading of the individual layers. Many of the trilevel layer combinations possible using graphite loadings of 0%, 5%, 18%, and 30% were tested. Several general observations were noted about the tri-level interconnect system. In general, the change in the initial resistance and final resistance of the via was maximized for layer combinations that contained at least two layers with low graphite loading (0%, 5%). For multilevel combinations where heavily loaded layers (18%, 30%) were used exclusively, there was minimal change in the initial and final resistance. Also, in general, the higher the graphite loading in the layers, the smaller the standard deviation of the via resistances across the array. This is due to the fact that for heavily loaded layers the initial resistance of the vias is several orders of magnitude less than that for lightly loaded films.

In Figure 2, the initial resistances and final resistances of a 5/30/30 layer are shown. As mentioned previously, the change in resistance due to activation of the interconnects is small compared to multilevel systems with 2 or more layers with low graphite loading. The vias were formed using a current density of 6.4 mA/mm^2 applied for a 5 second period. The initial resistances have an average value of 368 ohms. The final resistances have an average value of 81 ohms. The average change in resistance for the interconnects is 287 ohms. Figure 3 shows results of an array with a composition of 0/18/0. As can be seen from Figure 3, the initial resistances of

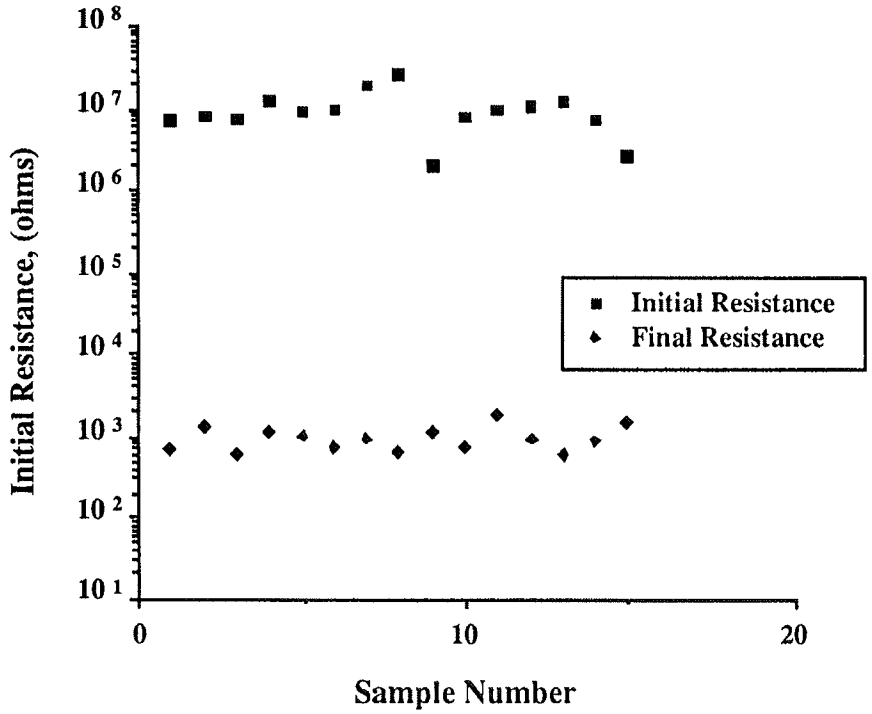

Figure 3. The change in resistance between the intial and final resistances of an interconnect structure with a layer combination of 0/18/0 wt% graphite.

the vias are well into the megaohms range. The average initial resistance is 9.3 Mohms. After formation of the interconnects the via resistance values drop several orders of magnitude. The average final resistance value is 950 ohms. The drop in resistance is significant enough to use the high resistance state as a disconnected via and the low resistance state as a conductive path. Another layer combination which displayed a significant drop in resistance is 3/3/3. A combination of three layers with a low weight percentage of graphite resulted in a initial resistance in the megaohm range. Figure 4 shows the initial resistance and final resistance of several interconnects. For this sample, the duration of the applied current is varied. Periods of 5 seconds and 10 seconds are used during testing. The average initial resistance of the vias is 7.0 Mohms. The average final resistance is 2.8 Kohms.

CONCLUSION

A thin film programmable interconnect array has been demonstrated. The interconnects were realized using multicoats of graphite / polyimide thin films with variable graphite loading.

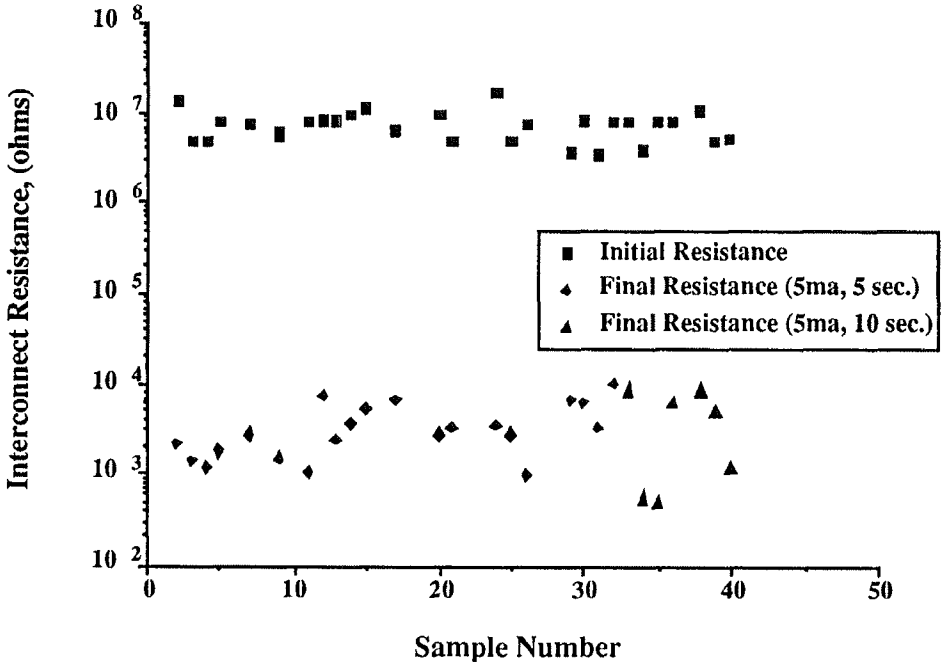

Figure 4. The change in resistance between the intial and final resistances of an interconnect structure with a layer combination of 3/3/3.

The process used to create the interconnect arrays is compatible with integrated circuit technology and uses commercially available cleanroom equipment and materials. The key advantages to the PIA are the standardization of integrated circuit packaging and the elimination of wire bonding during the packaging process. Interconnect arrays have been fabricated and tested for various tri-level systems. The layer combinations of 0/18/0 and 3/3/3 proved to yield the best result for the sample space chosen for investigation. Initial via resistances in the megaohm range were recorded. Final interconnect resistances in the 100 ohm to 10 Kohm range were achieved. Maximum changes in resistance between the initial and final states of the interconnect were in the megaohm range. Isolation between interconnects can be achieved either by plasma etching of the material between the interconnects or by using high resistivity layers (low graphite loadings) in the multilayer structure.

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