

Surface Micromachined Solenoid Inductors for High Frequency Applications

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Abstract—As operation frequencies and performance requirements of wireless devices increase, the resultant demands on the performance of passive components also increase. Miniaturization of inductive components for high frequency has been a key research area to address this issue; however, in general, miniaturized integrated inductors can suffer from low Q factors and/or self-resonant frequencies when compared to their discrete counterparts. In this research, a modified geometry of a solenoid type inductor using a surface micromachining technique is proposed. This inductor has an air core and an electroplated copper coil to reduce the series resistance, and its low temperature process is suitable for various packaging applications. An important feature of the proposed inductor geometry is the introduction of an air gap between the substrate and the conductor coil in order to reduce the effects of the substrate dielectric constant. This air gap can be realized using a polyimide sacrificial layer and a surface micromachining technique. Therefore, the resulting inductor can have less substrate-dependent magnetic properties, less stray capacitance, and higher Q -factor. The measurement result shows that this inductor has high Q -factor and stable inductance over a wide range of operating frequency. Also, various effects of geometrical factors have been investigated. Various inductors with the inductance varying from 1 to 20 nH and maximum Q -factor from 7 to 60 have been fabricated and measured.

Index Terms—Integrated inductor, Q -factor, solenoid, stray capacitance, surface micromachining.

I. INTRODUCTION

MODERN mobile communication requires compact and high frequency equipment. As this technology advances, the focus will be on smaller size, lower power consumption, higher frequency, and lower noise level systems. There has been much research to satisfy these requirements, and the miniaturization of an inductive component has been one of the key research areas [1]–[4].

One approach is to make an active inductive component [8] which simulates the electrical properties of an inductor is by using active circuitry, and it is possible to achieve very high Q -factor and inductance in a relatively small size with this approach. However, this approach may suffer from

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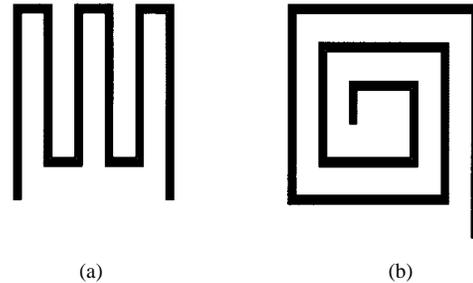


Fig. 1. Simplified schematic of a meander-type inductor (a) and a spiral-type inductor (b).

high power consumption and high noise levels. An alternative approach is the fabrication of integrated inductors, in which lithographic techniques are used to pattern an inductor directly on a substrate. However, in general, an integrated inductor suffers from low Q -factor and high parasitic effects. To expand the applications of integrated inductors, these characteristics must be improved.

Most of the conventional geometries for integrated inductors have been meander-types or spiral-types [1], [5], whereas most of the macro-scale inductors are solenoid-types. The main reason for not using a solenoid-type geometry for integrated inductors is a limitation of microfabrication techniques. Fabrication of a coil wrapped around a core has been more difficult using conventional IC processes than the fabrication of meander or spiral-types. Fig. 1 is a simplified schematic that shows a meander-type inductor Fig. 1(a) and a spiral-type inductor Fig. 1(b). A meander-type inductor is simple to fabricate but, because of negative turn-to-turn mutual inductance, it suffers from low overall inductance. A spiral-type inductor has a relatively high inductance, but has several other drawbacks. First, it requires a lead wire to connect from the inside end of the coil to the outside, which introduces an unnecessary capacitance between the conductor and the lead wire, and this capacitance is one of the dominant stray capacitances of this geometry [5]. Second, its size is large compared with other inductor types with the same number of turns. Third, the direction of flux is perpendicular to the substrate, which can interfere with the underlying circuit in multichip modules. This can be a problem for some vertically integrated devices.

Some of these issues associated with spiral-type inductors can be addressed by using solenoid-type inductors. Recent advances in micromachining technology have provided alternative processes for fabricating integrated solenoid-type

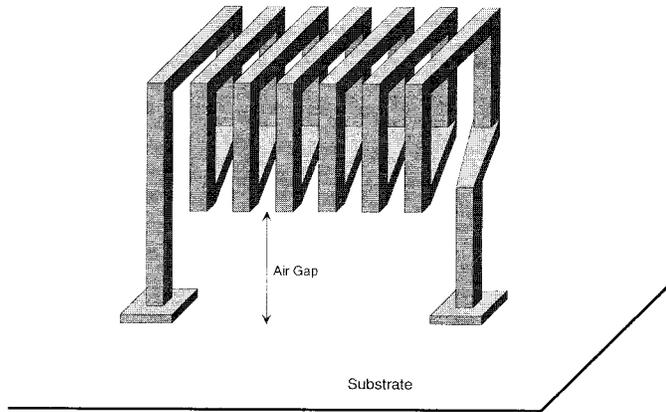


Fig. 2. A schematic of an integrated solenoid-type inductor with an air gap.

inductors. Previously, a solenoid bar type inductor, fabricated using various micromachining techniques, has been reported [6]. This inductor, which was intended for lower frequency use, had an electroplated Ni-Fe core, and electroplated copper layers which were used as conductors to reduce the coil resistance. In the work described in the present paper, an integrated inductor for high frequency applications based on solenoid geometries was designed and fabricated using polymer/metal multilayer processing and surface micromachining techniques. This inductor uses an air core and introduces an air gap between the substrate and the conductor by use of a surface micromachining technique and an organic sacrificial layer. This inductor can be fabricated using low-temperature fabrication processes, allowing the possibility of fabrication on either ceramic or organic (laminate) substrates.

II. DESIGN CONSIDERATIONS

For a solenoid-type inductor, neglecting the substrate and fringing, the inductance L can be represented with

$$L = \frac{N^2 \mu A_c}{l_c} \quad (1)$$

where A_c is the cross-section area of the core, l_c is the total length of the core, μ is the permeability of the core, and N is the number of coil turns. In order to increase the L in a given two-dimensional (2-D) area, the area of the core A_c can be increased, which requires a tall via structure. Therefore, a high aspect-ratio, i.e., height-to-width ratio, metal structure must be used to achieve the highest L and Q -factor for a given total inductor area.

A conductor layer composed of low resistivity metal is critical to maintain a high inductor Q -factor at very high frequencies. This is due to the skin effect whereby high frequency currents flow only in a surface layer of the conductor. Since the metals of lowest resistivity ρ are silver, copper, and gold, these are proper material choices for the conductor coil. Electroplated copper was chosen for the conductor coil.

In terms of fabrication complexity, the solenoid-type inductor is more complex than the spiral-type inductor. Fig. 3 shows the cross-sections of a spiral-type and a solenoid-type inductor. Since solenoid-type inductors require a gap between

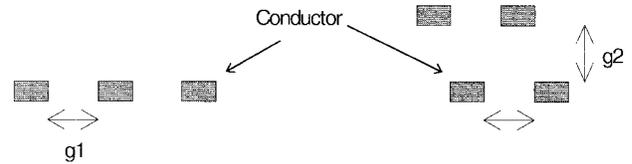


Fig. 3. Simplified cross section of a spiral-type and solenoid-type inductor.

the bottom and top conductors (unlike spiral-types, which have only gaps between underlying conductors), additional stray capacitance components between the top and bottom conductors must be considered in the design stage. Large gaps between top and bottom conductors, i.e., tall vias, will increase the inductance and decrease the stray capacitance. Since most current microfabrication techniques are based on 2-D geometry, achieving a very high aspect ratio metallic structure is often difficult. In addition, very precise dimensional control is required to control the characteristics of these microinductors. Since this device includes no magnetic materials, its inductance value strictly depends on its geometry. Since high aspect ratio vias and tight geometry control are required simultaneously, understanding of geometric tolerances of available photolithographic methods and plating profiles is critical in the design stage.

As mentioned before, stray capacitance determines the self resonant frequency (SRF), hence the inductor operation range and Q -factor of the inductor. Thus, controlling this capacitance is very important in the design stage and actual fabrication stage. Yamaguchi *et al.* [5] have reported calculated results for the stray capacitance of various parts of thin film inductors employing meander and spiral-type coils. It was reported that the capacitance between conductor lines was very small compared with the substrate-to-conductor capacitance. In an air-core inductor, where the only stray capacitances are conductor-to-conductor and conductor-to-substrate, reducing the conductor-to-substrate stray capacitance by introducing an air gap between the substrate and the coil (as currently done for integrated spiral inductors in some microwave circuits) can significantly lower the total stray capacitance. This air gap can be achieved with a surface micromachining technique using a polyimide sacrificial layer. To further reduce the winding capacitance, a coil geometry which minimizes stray capacitance between conductors by minimizing overlaps between the top and bottom conductor lines as shown in Fig. 4 can be utilized.

In order to estimate the stray capacitance characteristics of the inductor as a function of geometry, a simple equivalent circuit model (Fig. 5) is introduced. In this model only conductor-to-conductor capacitances were considered. Also this model is built on the assumption that the inductor coil is suspended in air and the via conductors have no effect on the total stray capacitance. C_t is the capacitance between two top conductor lines, C_b between two bottom conductor lines, C_{bt} between the top and the bottom conductor lines, and C_x between two diagonally placed conductor lines (Fig. 5). Neglecting fringing, these capacitances can be represented as

$$C_t = C_b = \frac{\epsilon A}{d} = \frac{\epsilon(w \cdot b)}{s} \quad (2)$$

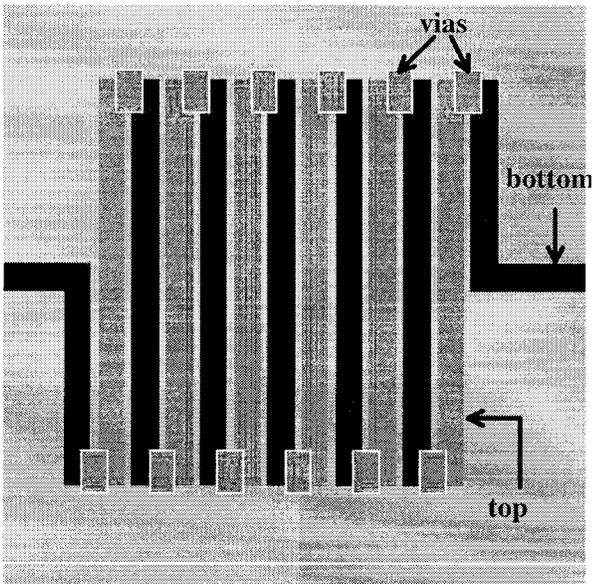


Fig. 4. A coil geometry to reduce the stray capacitance caused by conductor lines.

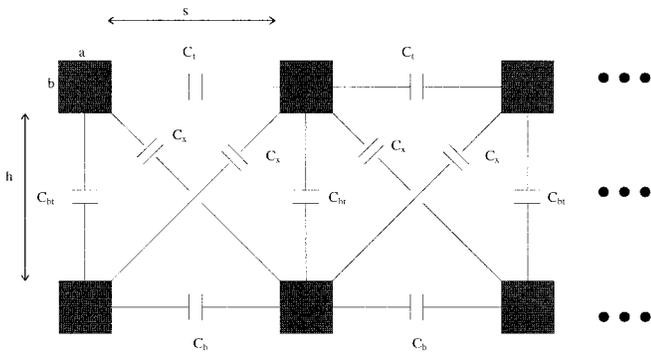


Fig. 5. Equivalent circuit for calculation of the stray capacitance between conductor lines. The cross-sectional area of the conductor lines and the capacitances between these conductor lines are shown.

$$C_{bt} = \frac{\varepsilon(w \cdot a)}{h} \quad (3)$$

$$C_x = \frac{\varepsilon(w \cdot \sqrt{a^2 + b^2})}{\sqrt{s^2 + h^2}} \quad (4)$$

where ε is the dielectric constant of air, a is the width of a conductor line, b is the height of the conductor line, w is the length of each conductor line, s is the horizontal spacing between each conductor line, and h is the vertical spacing (via) between the top and the bottom conductor lines. After calculating each of the capacitances between conductor lines, these calculated values have been substituted in the circuit model in Fig. 5. The total capacitance of the model is then calculated using a circuit simulation program.

Fig. 6 shows the effect of the core height, the vertical spacing between the top and the bottom conductor (h). Obviously, the highest possible value of h is desired since this will increase the inductance and decrease the stray capacitance. Fig. 7 shows the effect of the line spacing between two adjacent conductor lines (s). The total stray capacitance

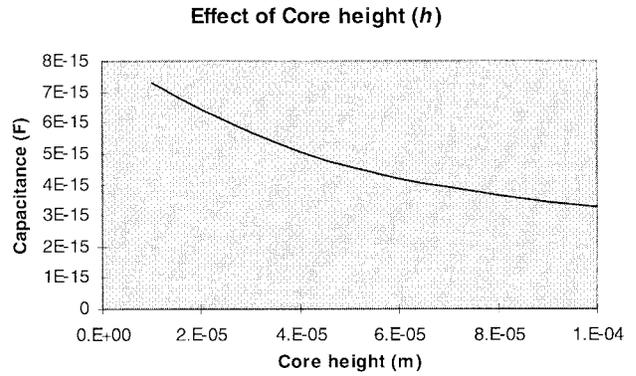


Fig. 6. The stray capacitance change with various core height (h), assuming constant line spacing (s) and conductor thickness (b).

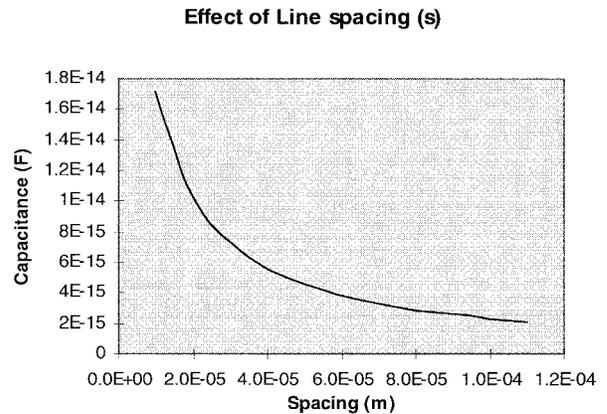


Fig. 7. The stray capacitance change with various line spacing (s), assuming constant h and b .

decreases sharply when the line spacing changes from 10 to 30 μm and continues to decrease with increasing line spacing. Even though the increased line spacing helps to reduce the stray capacitance, it also increases the required inductor size and decreases the inductance. The effect of the conductor line thickness (b) is shown in Fig. 8. The total stray capacitance is linearly increasing with the conductor line thickness. Even though the increased conductor thickness can reduce the series resistance, it also increases the stray capacitance and lowers the self resonant frequency. Due to the skin effect, the required thickness of the conductor lines, generally, reduces with increasing frequency, and a conductor thickness of several times the skin depth can be a proper choice. Therefore, the choice of the conductor thickness must be based on the desired Q -factor and operating frequency range. Although the assumptions inherent in these models do not allow quantitative calculation of stray capacitance, the qualitative trends of the models are useful for inductor design.

III. FABRICATION

Fig. 9 shows a brief description of the fabrication process. The fabrication starts with an unpolished 2 in \times 2 in alumina substrate coated with 30 μm planarization layer of DuPont PI-2611 polyimide. A seed layer of Cr/Cu/Cr (500 \AA /3000 \AA /500

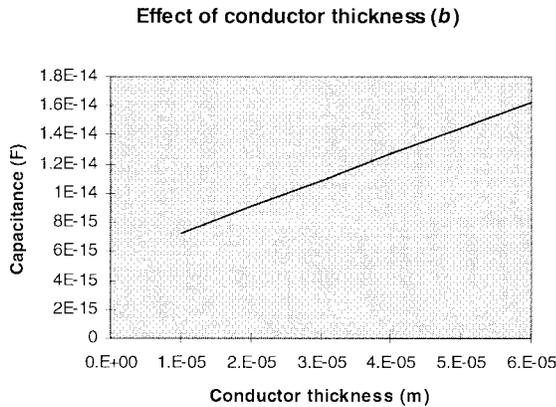


Fig. 8. The stray capacitance change with various conductor line thickness (b), assuming constant h and s .

Å) is deposited on top of the polyimide layer. Multiple coating of DuPont PI-2611 on the seed layer and curing in N_2 for one hour at $350^\circ C$ produces a $20\ \mu m$ thick PI layer. A $1500\ \text{Å}$ Al layer, which will act as a hard mask for subsequent polyimide etching, is deposited using DC sputtering (this approach is commonly used in RIE patterning of polyimide in plasmas which contain only oxygen and/or fluorine chemistries). A support pattern to sustain an air gap between the substrate and the coil is defined using conventional photolithography and wet etching techniques in a standard PAN (phosphoric, acetic, and nitric acid) etching solution. The PI layer is etched with 100% O_2 RIE, which generates a very steep side wall profile with very little under-etching (at the expense of etch rate), which is particularly useful in fabricating posts and via holes. The Al layer is removed using wet etching (e.g., PAN or a dilute hydrofluoric acid solution), and the etched polyimide is used as a mold for the deposition of electroplated Cu (a).

After depositing a seed layer of Cr/Cu/Cr, another layer of PI is deposited. As previously mentioned, this PI layer is patterned and a bottom conductor layer is deposited (b). A $30\ \mu m$ thick PI layer is deposited and via hole patterns are defined on an Al mask. The via holes are formed with 100% O_2 RIE and Cu vias are electroplated through these via holes (c). To reduce the via contact resistance, the copper oxide film is removed in a dilute sulfuric acid solution.

A new PI layer for the top conductor layer is deposited, and etched using 100% O_2 reactive ion etching (RIE). The top conductor is deposited using Cu plating (d). A combination of gases, 20% CHF_3 and 80% O_2 , RIE is used to remove the PI layer. Unlike 100% O_2 , a gas mixture of 20% CHF_3 and 80% O_2 RIE has a strong tendency to under-etch the polyimide beneath the metal structure, and is thus very useful in forming the air core and the air gap between the substrate and the copper coil. After removing all of the PI layers, the seed layer is removed using wet etching with standard etchants (e).

Fig. 10 shows a top-view of an integrated inductor with a ten turn coil fabricated on an alumina substrate. Fig. 11 shows an open-pad without an inductor. Later, the measured S -parameters of this open-pad will be used for de-embedding. Fig. 12 shows two scanning electron microscope (SEM) pic-

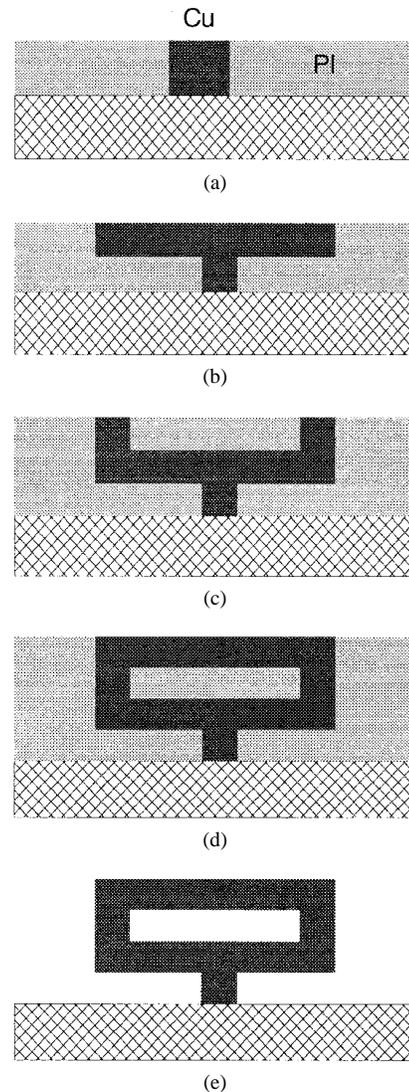


Fig. 9. Simplified fabrication process.

tures of fabricated inductors suspended over the substrate. These pictures clearly show the air gap and the air core. The height of the air gap from the substrate are $50\ \mu m$ and $20\ \mu m$, respectively. High aspect ratio vias were used to increase the inductance and to decrease the stray capacitance between the top and the bottom conductor lines. Up to 1.5:1 aspect-ratio vias have been fabricated using a polymer/metal multilayer and high aspect-ratio via formation, as shown in Fig. 13.

Since this inductor has an air core, its magnetic properties are determined only by its geometry. Therefore, controlling the error margin in each photolithography and etching stage is very important to maintain good magnetic properties. For example, poor planarization or over-etching of a metal mask or a PI layer can cause widened conductor patterns. These widened conductor patterns will reduce the distance between each conductor pattern, hence increase the total stray capacitance. Special care is needed to achieve good planarization and accurate etching. Also, thermal processes (for example, a thermal curing of PI or photoresists) can cause a thin oxide film formation on copper conductors. In order to keep the lowest

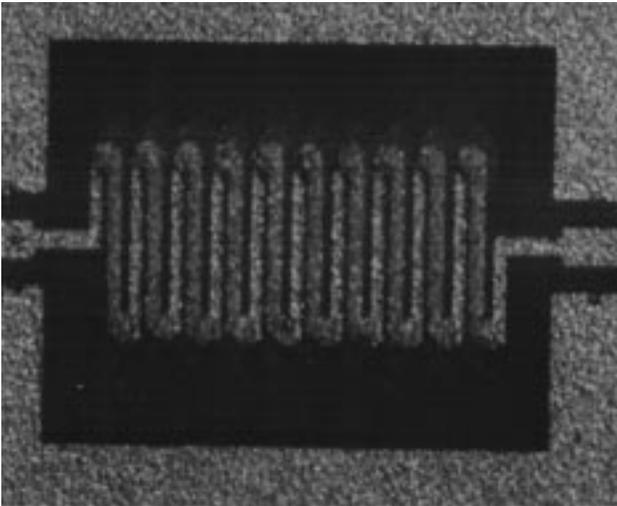


Fig. 10. A top-view of an integrated solenoid-type inductor.

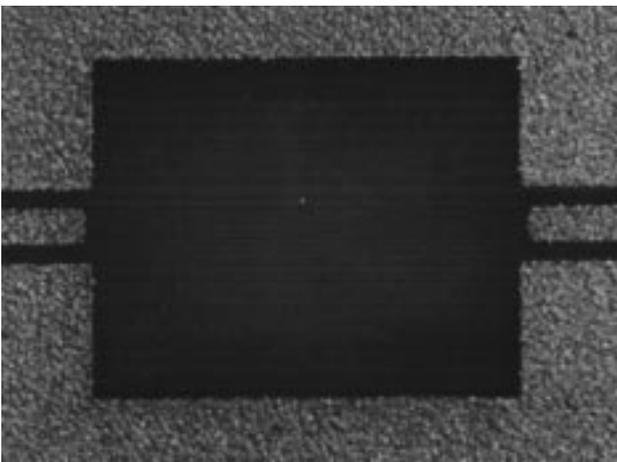


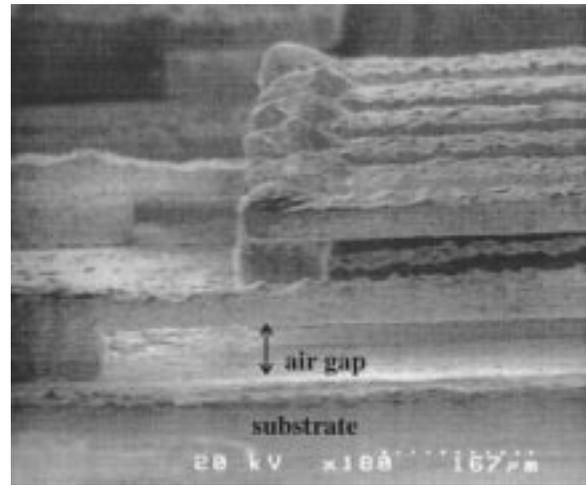
Fig. 11. A top-view of an open-pad fabricated on the same substrate with the inductors for contact pad de-embedding.

resistivity possible, these oxide films were removed using wet etching techniques after every thermal processes.

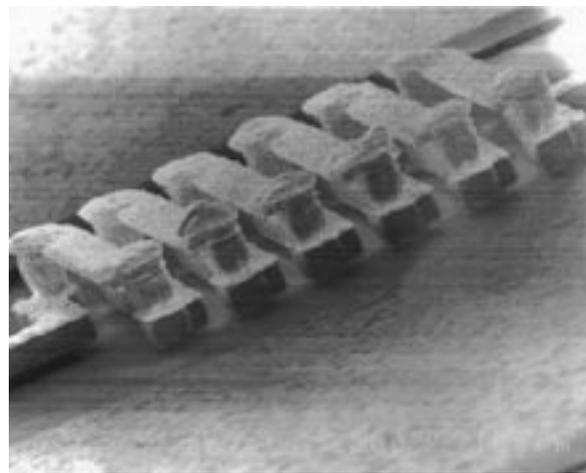
IV. MEASUREMENTS AND RESULTS

Various integrated inductors with different geometries, such as the number of turns and core sizes were fabricated. Fig. 14 is a equivalent circuit model of the inductor [7]. In this model, the combination of R_1 , R_2 , L_1 , and L_2 represents the resistance change with frequency due to the skin effect, and the capacitor C is the effective total capacitance across the inductor.

The samples have been measured using an HP 8510C vector network analyzer and CASCADE MICROTECH ground-signal-ground high frequency coplanar probes with 100 μm pitch size. The inductors were designed to have two-ports surrounded by a ground plane. The two-port s -parameter measurements were averaged and then a π -network was generated according to the measured s -parameters. The unloaded input impedance was computed and the unloaded Q -factor was determined by dividing the imaginary part (inductive



(a)



(b)

Fig. 12. Scanning electron micrographs of the solenoid-type inductors suspended over the substrate by (a) 50 μm and (b) 20 μm .

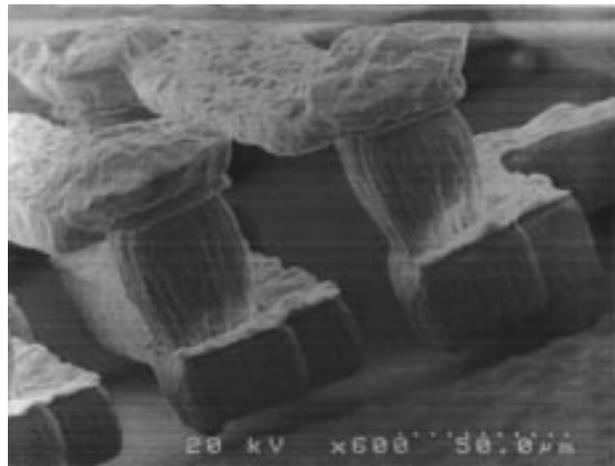


Fig. 13. Scanning electron micrograph showing high aspect-ratio (1:1.5) vias.

stored energy) by the real part (dissipated energy) of the input impedance.

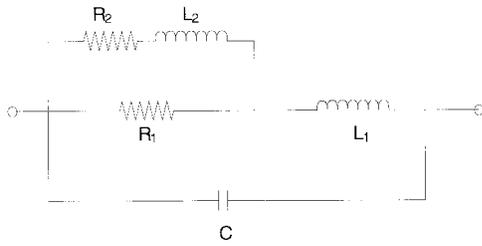


Fig. 14. Equivalent circuit model of the inductor.

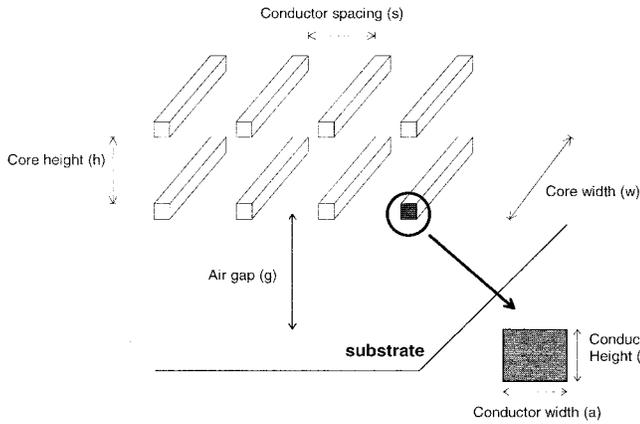
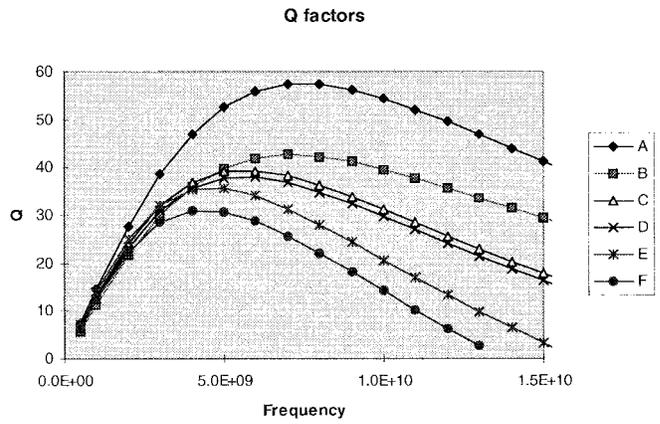


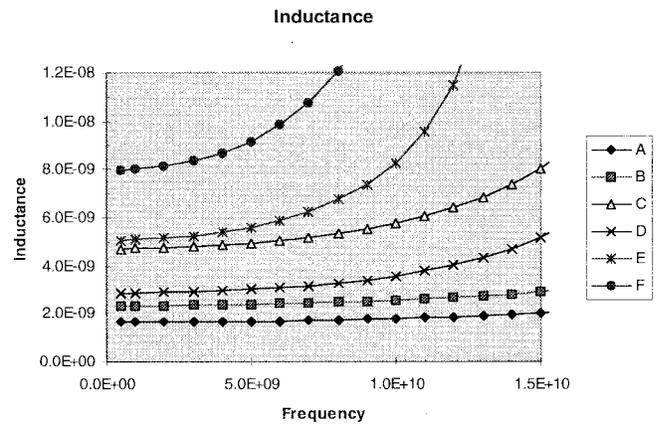
Fig. 15. Geometrical parameters for solenoid-type inductors.

To remove the effect of the measurement parasitics, open-pads without inductors were designed and fabricated on the same substrate with the inductors. The measured s -parameters of the open-pad were interpreted as a series R and C circuit, and the R and C values were used to de-embed the open-pad from the inductor. The de-embedding and lumped parameter extraction has been performed by using an HP microwave and RF design system (MDS). The lumped parameter extraction has been accomplished with a nonlinear optimization algorithm that employs a hybrid-optimization in MDS.

Geometrical parameters of a solenoid-type inductor have been illustrated in Fig. 15. Table I shows a list of the fabricated inductors with different number of turns (N) and core width (w). These inductors have $20\ \mu\text{m}$ wide (a) and $20\ \mu\text{m}$ thick (b) electroplated copper conductor lines, and the spacing (s) between each of the turns is $50\ \mu\text{m}$. The vias have $33\ \mu\text{m}$ height (h), and the cross-sectional area of the vias is $30\ \mu\text{m}$ by $60\ \mu\text{m}$. All inductors have $20\ \mu\text{m}$ air gaps (g). Since the conductor width (a) and the spacing (s) are constant, the total inductor length (core length) is proportional to the number of coil turns (N), and this can be represented as, $\text{Core Length} = 2(s + a)N$. The core length varies with the number of turns and they are 400 , 720 , and $1520\ \mu\text{m}$ for 6 , 10 , and 20 turn inductors, respectively. The measured results, Q -factor and inductance, of the inductors are shown in Fig. 16. Typical dc resistance value varies from 0.32 to $1\ \Omega$, inductance from 1 to $8\ \text{nH}$ and stray capacitance from 13 to $30\ \text{fF}$. The smallest inductor, A, has a self resonant frequency of $25\ \text{GHz}$.



(a)



(b)

Fig. 16. Measured results of various inductors, (a) Q -factor and (b) inductance.

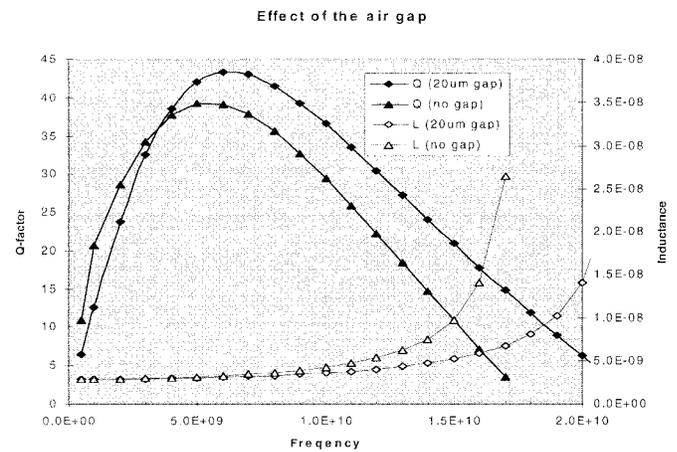


Fig. 17. Effect of the air gap. The stray capacitance has been reduced from $25.1\ \text{fF}$, with no air gap, to $17.7\ \text{fF}$, with an $20\ \mu\text{m}$ air gap.

Fig. 17 shows the effect of a $20\ \mu\text{m}$ air gap, which shows the improvement of the electrical properties of the inductor. The stray capacitance has been reduced from $25.1\ \text{fF}$, with no air gap, to $17.7\ \text{fF}$, with a $20\ \mu\text{m}$ air gap. It is shown that the inductor with an air gap has higher Q -factors and SRF than the one without an air gap. Also, the inductor with an

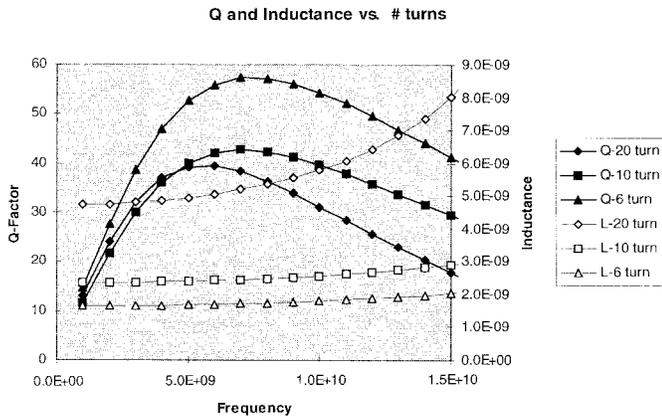


Fig. 18. Q and inductance of inductors with different number of turns.

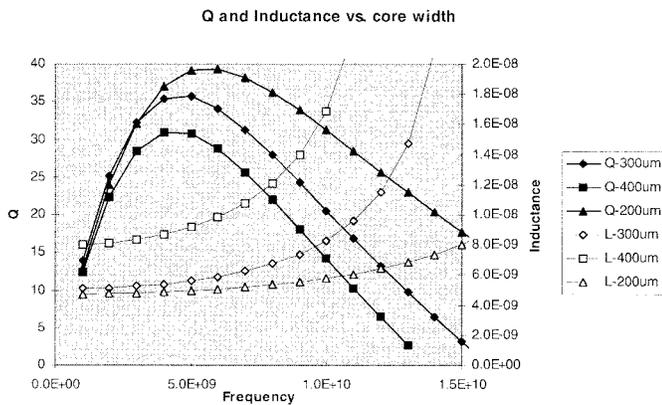


Fig. 19. Q and inductance of inductors with different core sizes.

TABLE I
INDUCTORS WITH DIFFERENT NUMBER OF TURNS (N) AND AIR CORE WIDTH (w)

	A	B	C	D	E	F
turns	6	10	20	10	20	20
core width (μm)	200	200	200	400	300	400

air gap has better inductance stability. Fig. 18 represents the effect of the number of turns on the Q -factor and inductance. Obviously, increasing the turns increases the inductance, as can be expected from (1). But this increases the resistance and the stray capacitance of the inductor, which lowers the SRF and Q -factors. Fig. 19 shows the effect of the core size by varying the core width (w). These inductors have the same number of turns (N), therefore all have the same core length. The increase in the core width (w) increases the inductance, because it increases the core cross-sectional area, as shown in (3)–(11). But the increase in w also increases the stray capacitance between the top and bottom conductor lines and the series resistance due to the increased overall coil length, resulting in lower Q -factor and lower self resonant frequency.

V. CONCLUSION

A packaging compatible integrated solenoid-type inductor for high frequency applications has been proposed and fab-

ricated using polymer/metal multilayer processing techniques and surface micromachining techniques. To achieve high Q -factor, this inductor has solenoid-type geometry with an air core and introduces an air gap between the substrate and the conductor, which reduces stray capacitance contributed by the high dielectric constant of the substrate. This air gap was realized by using an organic sacrificial layer and releasing with a dry etching technique. The metal support maintaining the air gap can be an extension of the connection between underlying circuitry and the inductor.

Also, the effect of inductor geometry has been investigated by designing and fabricating several inductors with varying geometry. A large air core generated with increased core width (w) can help to increase the inductance, but this also contributes to the stray capacitance increase. This stray capacitance increase reduces the resonant frequency and the Q -factor. Therefore highest aspect-ratio vias (h), as tall as current fabrication processes permit, is needed to achieve maximum inductance and Q -factor. In addition, the effect of the air gap to the inductor characteristics has been demonstrated.

Even though these solenoid-type inductors have the drawback of increased fabrication complexity, they have very good electrical properties such as high inductance and high Q -factors for a given 2-D inductor area. Therefore, these inductors can find applications where inductors of compact size and good electrical properties are required.

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