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Planarization techniques for vertically integrated metallic MEMS on silicon foundry circuits

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Abstract. Various micromachining techniques exist to realize integrated microelectromechanical systems (MEMS), which include sensors, signal processing and/or driving circuits, and/or actuators in one small die. Post-processing techniques performed on foundry-fabricated circuits (e.g., MOSIS) are attractive since such an approach eliminates the need for an in-house integrated circuit fabrication line to produce integrated MEMS. A method based on the combination of metallic (e.g., electroplating) micromachining techniques with multichip module deposited (MCM-D) processes is a possible candidate to realize vertically-stacked integrated MEMS using the post-processing of integrated circuits (post-IC) approach. In order to realize such devices, planarization of the surface of foundry-fabricated circuit chips or wafers is often required. In such planarization layers, mechanical and chemical stability, as well as adhesion between the circuit-containing substrate and the micromachined devices, should be addressed. A PI/BCB/PI sandwich interlayer system, which utilizes both advantages of DuPont polyimide PI 2611 and Dow benzocyclobutene (BCB) Cyclotene 3022 series, was developed as a planarization interlayer for vertically integrated MEMS. The PI/BCB/PI interlayer system shows an over 95% degree of planarization (DOP) as well as passes the Method 107G Thermal Shock from the military standard MIL-STD-202F. A SiO_2/BCB/SiO_2 interlayer system was also developed as an alternative to the PI/BCB/PI system.

1. Introduction

Integrated MEMS offer many advantages over conventional macroscopic sensor/actuator systems, such as high reliability, high functionality in a small space, low weight, low energy consumption, and the potential for low-cost manufacturing. Previously, several integration techniques have been proposed to realize integrated MEMS. Those investigations can be divided into two categories. The first category includes modification of the integrated circuit fabrication process (including complementary metal oxide semiconductor (CMOS), bipolar IC, BiCMOS, etc) to produce MEMS structures during the circuit fabrication [1, 2]. The second category involves post-processing of foundry-fabricated circuits either using packaging techniques [3], a single-crystal reactive etching and metallization (SCREAM) process [4, 5], or anisotropic wet etching techniques [6, 7].

In the modified circuit fabrication approach [1, 2], circuits and micromachined devices are batch fabricated using, for example, standard CMOS or modified CMOS processes. In this approach, a commonly used technique is polysilicon-based micromachining, which uses polysilicon as a structural material and phosphosilicate (PSG) or borophosphosilicate (BPSG) glass as a sacrificial material. The structural polysilicon is normally deposited using low-pressure chemical vapor deposition (LPCVD), followed by an annealing process, which is normally performed at approximately 900 °C, well over the 660 °C melting point of aluminum (Al) [8]. In order to overcome this limitation, either the micromachined devices are fabricated prior to the deposition of Al, or the standard CMOS process is modified to use higher melting point metals, such as tungsten [1] (with a melting point of 3410 °C [8]). Using either method, circuits and micromachined devices are batch fabricated and inherently merged in one die, so realization of integrated MEMS is feasible. However, an in-house or otherwise modifiable integrated circuit fabrication facility is required to realize integrated MEMS.

One of the simplest approaches for realizing integrated MEMS without the necessity of modifying an IC process is

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based on multichip packaging using, for example, printed circuit boards (PCB) [3], multichip modules, or similar packaging techniques. In this approach, micromachined devices and circuits are fabricated separately and integrated in one package using an external (chip-to-chip) wire interconnection, such as wire bonds, ribbon cables, or solder bumps. Since the packaging integration process is a separate process, circuits can be produced using a standard IC fabrication process and micromachined devices can be fabricated using virtually any micromachining technique. However, since the printed circuit board packaging integration process requires external wire interconnection, it is expected that in some applications the reliability and the signal-to-noise ratio of the integrated package may be limited in comparison with other integration techniques.

Another approach for realizing integrated MEMS is the post-IC approach using the SCREAM process [4]. The SCREAM process defines microstructures using single-crystal silicon (SCS) as a structural material. The micromachining processes performed after the completed circuit fabrication are all low temperature, such as oxide deposition using plasma enhanced chemical vapor deposition (PECVD), oxide and single-crystal silicon etching using reactive ion etching (RIE), and aluminum deposition using sputtering. This technology can realize relatively high aspect ratio microstructures and has also been used to show the feasibility of using single-crystal gallium arsenide (SC-GaAs) as a structural material [5].

Another attractive post-IC approach is anisotropic etching of MEMS structures on foundry-fabricated circuits, using, for example, an ethylene-diamine-pyrocatechol (EDP)-based process [6] or, a potassium hydroxide (KOH)-based process [7]. In these processes, appropriate passivation layers serve as etching masks for the silicon substrate as well as protective layers for other wafer features if required. The exposed silicon is subsequently etched by EDP or KOH. Micromachined devices are usually formed using polysilicon and/or aluminum. This technology has been used to realize various types of integrated sensors [6, 7] by this simple post-processing etching step of foundry-fabricated IC chips.

Summarizing the two distinct approaches discussed above, the modified IC process is a good approach to flexibly realize high-performance integrated MEMS. However, access to and potentially modification of an IC fabrication facility is required; such access may not be available in many research laboratories and small businesses. In contrast, the post-IC approaches use already-fabricated foundry circuit chips, thus eliminating the need for an in-house IC fabrication line. Although the SCREAM and the EDP etching processes are attractive post-IC processes, since both processes are subtractive (i.e. dry or wet etching is used to selectively remove sections of the foundry-fabricated circuit to form MEMS devices), designs and material selections for such devices fabricated using these technologies are limited to those achievable using subtractive processing.

Additive post-processing offers an attractive alternative for the realization of integrated MEMS. In additive post-processing, microstructures are built on top of

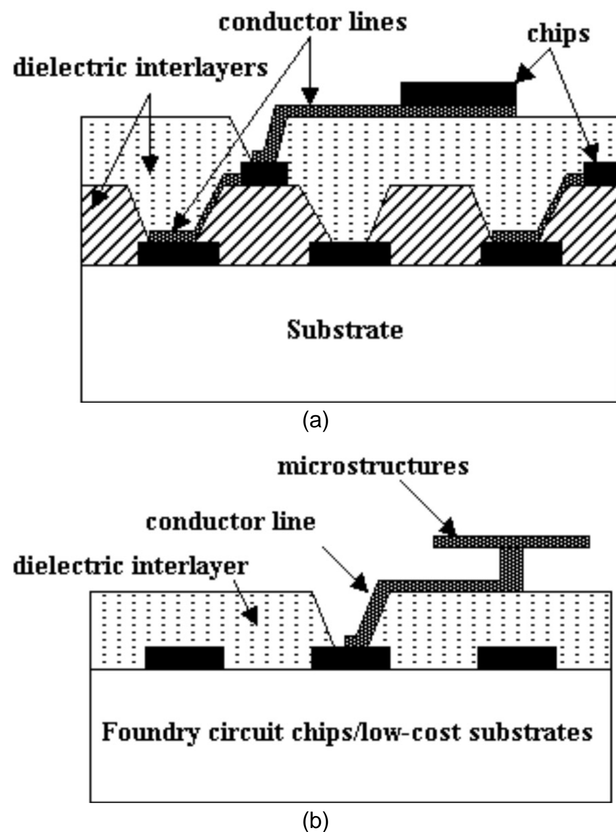


Figure 1. Schematic representation of (a) a common MCM-D structure; (b) a vertically integrated metallic MEMS.

already-fabricated circuit chips to form a vertically-stacked integrated MEMS. Electroplating-based metallic MEMS technologies [9–11] are good candidates to realize integrated MEMS using this additive post-processing approach, due to the ability to realize high aspect ratio structures, and the low deposition temperatures required. To build microstructures on top of already-fabricated circuit chips, the surface of the circuit chips should be coated with an interlayer material which has the following attributes: it is planarizing to make subsequent photolithography easier, provides electrically insulating layers between the MEMS devices and the underlying circuitry, and enhances adhesion between the chip and the microstructures. In this paper, several polymeric combinations have been studied, tested, and characterized as candidates for this interlayer between foundry-fabricated circuit chips and micromachined devices/systems. Polymeric combinations could be used not only as interlayers, but also as electroplating molds to fabricate microstructures. The purpose of this paper is to investigate a variety of interlayer materials and assess their performance for application in the realization of additive, integrated MEMS, with particular emphasis on planarization, reliability, and fabrication compatibility with electroplated metallic MEMS.

The determining factors for whether or not an integrated MEMS can be produced using post-IC techniques are process temperatures and the chemical processes involved. Process temperatures of the post-IC process should not exceed a certain temperature (normally, in the range

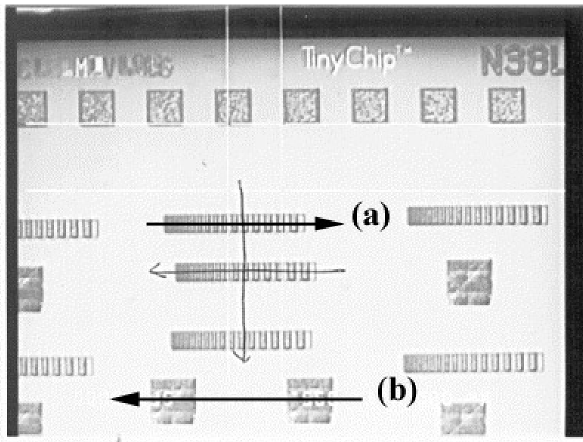
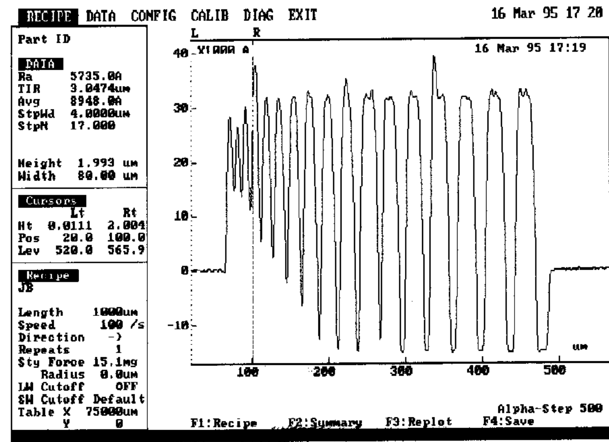


Figure 2. An optical micrograph of the top view of the test chip. Tested features are labeled (a) and (b) and are measured in figure 3.

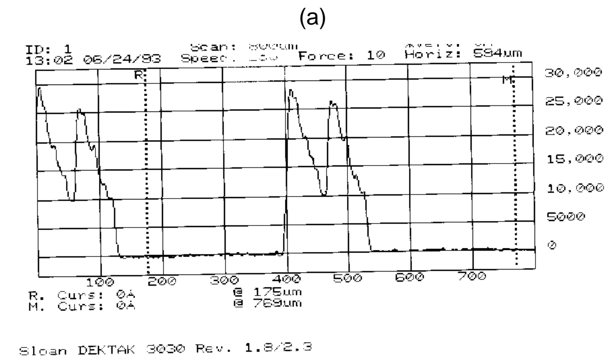
of 400–500 °C [12]) so as not to damage or alter the performance of already-fabricated foundry IC. In multichip module deposited (MCM-D) applications [13], interlayer dielectrics separate and insulate metal conductors to form a vertical interconnection structure. Since the physical interlayer structure of the MCM-D is similar to that required for vertically integrated MEMS, a combination of electroplating-based micromachining techniques with MCM-D processing technology could provide the means for realizing a vertically integrated MEMS. Figure 1 shows schematic diagrams that compare a common MCM-D structure with a vertically-stacked integrated MEMS. Previously, researchers at Texas Instruments [14] investigated vertically integrated MEMS for spatial light modulators which utilized sputtered metals and an organic spacer on top of static random access memory (SRAM) circuits. Electroplating-based metallic MEMS technology is also a good candidate to build metallic microstructures on top of circuit chips/wafers.

2. Test chip design and measurement methodology

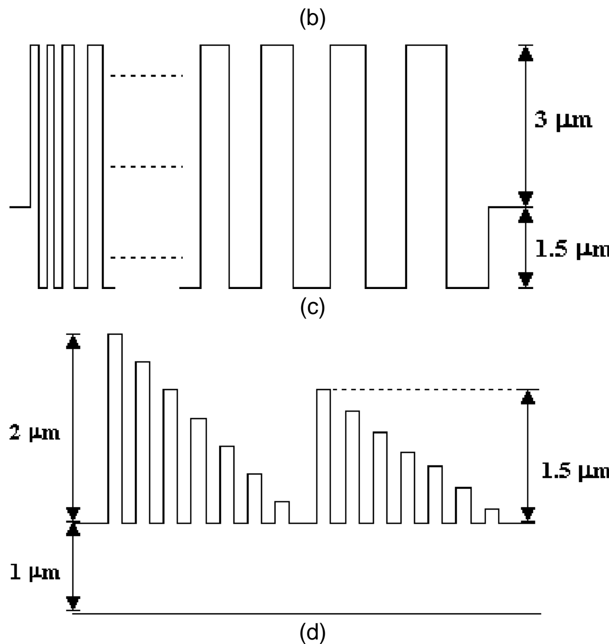
Test foundry chips were fabricated using the conventional CMOS foundry service, MOSIS [15]. The test chip contains various features that simulate the vertical and horizontal structures of a typical foundry-fabricated IC. Figure 2 shows the photomicrograph of the top view of the test chip. Figure 3 shows the surface profile measurement data ((a) and (b)) and schematic diagrams ((c) and (d) corresponding to (a) and (b), respectively) of two test structures which correspond to the scanning directions labeled (a) and (b) on figure 2. The test chip has 17 of the first test structure (figure 3(a)) and 14 of the second test structure (figure 3(b)). The first test structure has a total of 17 vertical features which have the same height (3 μm above the surface of the chip) and depth (1.5 μm below the surface of the chip) with variations of lateral dimensions. The lateral dimensions are in the range 4–20 μm line/spacing. Beginning with 4 μm lines and spaces,



(a)



(b)



(c)

(d)

Figure 3. (a, b) Surface profile data for and (c, d) schematic diagrams of surface test structures on the test foundry chip.

each line and space is incremented by 1 μm until the 20 μm lines and spaces are reached. The second test structure has a total of 16 line/spacing (4 μm line/spacing) features with variations of vertical height from 1 to 3 μm. The size of the test chip is 3 mm on a side. The interlayers developed and tested will be deposited onto this test chip. Two important parameters will be assessed: the degree of planarization (DOP) of the interlayers, and the mechanical robustness

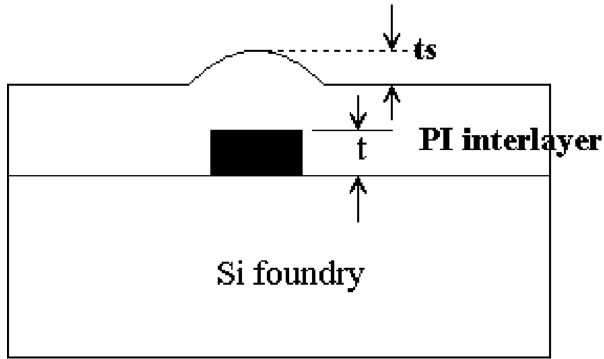


Figure 4. Schematic representation of planarization.

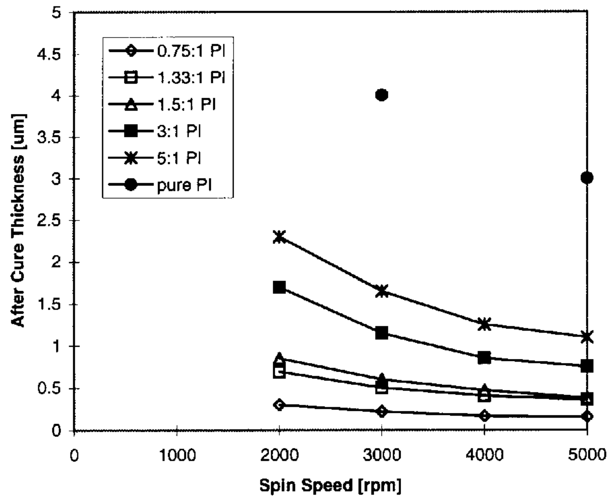


Figure 5. The measured achievable after-cure thickness as a function of spin-casting speed for various thinned DuPont PI 2611 formulations.

of the interlayer to thermal cycling and thermal shock. In addition, processing parameters for the etching of via holes through the interlayers will be investigated.

The planarity of the interlayer is defined using the DOP, which is given by

$$\mathrm{DOP} = \left(1 - \frac{t_s}{t}\right) \times 100\% \quad (1)$$

where t is the height of the bump of the structure before the planarization and t_s is the height of the bump after the planarization as shown in figure 4. As the DOP increases (approaching 100%), the surface of the structure becomes more planar. As discussed above, various interlayer systems have been studied with respect to the DOP, total thickness achieved, and mechanical and chemical stability for each system.

3. Study on PI 2611-based interlayer systems

DuPont polyimide PI 2611 is widely used in microelectronic packaging applications. In particular, this material has a well matched coefficient of thermal expansion (CTE) of 3 ppm/°C [16] to silicon (CTE of 2.3 ppm/°C) [17]. This

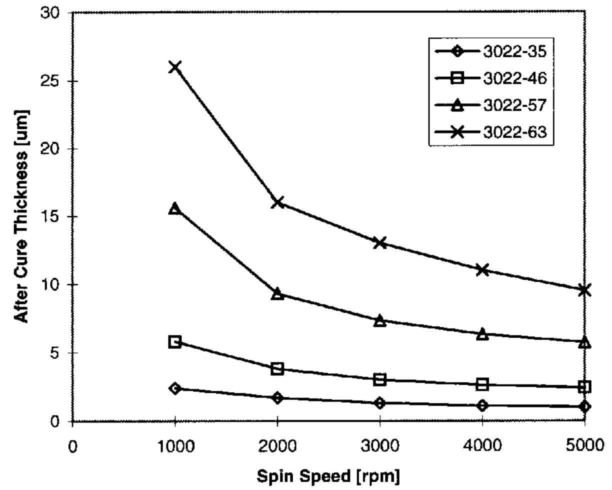


Figure 6. The measured achievable after-cure thickness as a function of spin-casting speed with 30 s spin-casting for the Dow Cyclotene 3022 series.

well matched CTE makes it suitable as an interlayer for applications where temperature changes/cycling have the potential to induce structural failures. DuPont polyimide PI 2611 was investigated as the interlayer for vertically integrated MEMS. It was desirable to investigate multiple coats of thinned polyimide instead of unthinned polyimide for two reasons. First, higher DOP can be achieved at constant thickness by multiple coats of thin material than by fewer coats of thick material. Second, since via connections for electrical signals must be made through the thickness of the interlayer, it is desirable to maintain as low an overall interlayer thickness (consistent with an acceptable degree of planarization) as possible. A polyimide thinner (DuPont T-9038) was used to dilute the PI 2611 and make multiple coats to achieve higher DOP. Figure 5 shows the measured achievable after-cure thickness as a function of spin-casting speed for various diluted PI 2611 formulations (in figure 5, 0.75:1 PI means 0.75 parts of PI 2611 with 1 part of thinner by volume, etc).

Prior to the first layer of organic coating, an adhesion promoter (95 ml of methanol, 5 ml of deionized water, two drops of adhesion promoter DuPont VM-651) was applied. Multiple coats of various PI 2611 formulations (both diluted and undiluted) were spin-cast on the test chip and soft cured at 120 °C in a convection oven for 10 min for each layer and finally fully cured at 300 °C for 1 h in nitrogen ambient. The maximum achievable DOP (approximately 75%) using multiple coats of diluted polyimide PI 2611 with the same overall thickness was much improved over that of undiluted polyimide (DOP approximately 50%). Although the achieved planarity is good, there may be applications where even higher DOPs are required.

4. Study on BCB-based interlayer systems

To achieve higher DOPs, it was desirable to investigate other organic materials that have excellent planarization

Table 1. Typical properties of the Dow BCB Cyclotene 3022 series [17].

	3022-35	3022-46	3022-57	3022-63
Resins content (%)	35	46	57	63
Viscosity (cSt @ 25 °C)	14	52	259	870
Density (g/cc @ 25 °C)	0.93	0.95	0.97	0.99
Thickness range (μm)	1 ∼ 2.5	2.5 ∼ 6	5.5 ∼ 16	9 ∼ 25

Table 2. 5.6 μm thick PI/BCB/PI on a test chip.

	Spin-casting speed (rpm) /time (s)	Total thickness (μm)	Thickness of feature (μm)	DOP (%)
Before PI coating		0	4.5	0
Bottom 5-to-1 PI 2611	5000/30	1.4	3.8	15.6
Middle BCB 3022-46	5000/30	4.9	0.3	93.3
Top 1.5-to-1 PI 2611	5000/30	5.6	0.2	95.6

Table 3. 15 μm thick PI/BCB/PI on a test chip.

	Spin-casting speed (rpm) /times (s)	Total thickness (μm)	Thickness of feature (μm)	DOP (%)
Before PI coating		0	4.5	0
Bottom PI 2611	5000/30	3.0	2.2	51.1
Middle BCB 3022-57	2000/30	12.3	0.1	97.8
Top PI 2611	5000/30	15.3	0.08	98.2

Table 4. 19 μm thick PI/BCB/PI on a test chip.

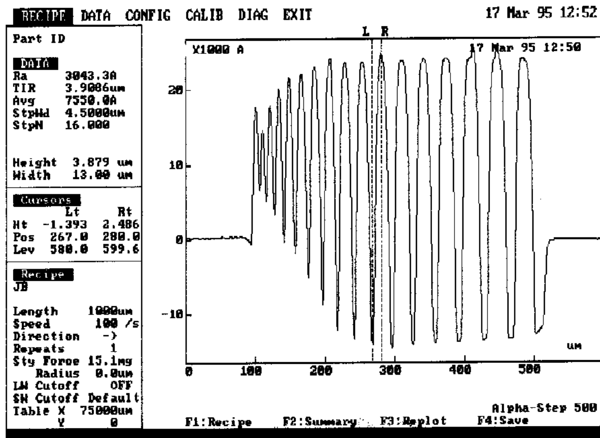
	Spin-casting speed (rpm) /time (s)	Total thickness (μm)	Thickness of feature (μm)	DOP (%)
Before PI coating		0	4.5	0
Bottom PI 2611	5000/30	3.0	2.2	51.1
Middle BCB 3022-63	3000/30	16.0	0.07	98.4
Top PI 2611	5000/30	19.0	0.06	98.7

properties. One of these materials, known as benzocyclobutene (BCB), is a commercially available, thermosetting, crosslinked aromatic polymer that has been developed by Dow Chemical Company (Midland, MI, USA). It is widely used in multichip module applications because it has several superior properties such as minimal metal migration and a flexible thermal cure capability (low-temperature hard cure, ∼200–250 °C in nitrogen ambient) [18]. Typical properties of BCB are shown in table 1.

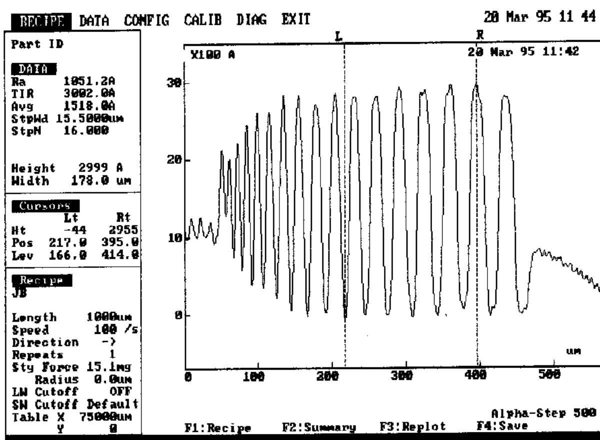
Figure 6 shows the after-cure thickness versus spin-casting speed with 30 s spin-casting of the Cyclotene 3022 series BCB. As expected, the maximum achievable DOP using BCB was over 95%. Even though the BCB has excellent planarization properties, the cured BCB is chemically and mechanically less stable than DuPont PI 2611. For example, stress-related cracking has been observed in mechanically and thermally shocked BCB films. This phenomenon may be due to the CTE mismatch between silicon (CTE of 2.3 ppm/°C) [17] and BCB (CTE of about 60 ppm/°C) [19, 20]. This susceptibility to cracking does not allow BCB alone to meet the requirements of the organic interlayer for vertically intergrated MEMS.

5. Study on PI/BCB/PI interlayer systems

Several polymer combinations have been investigated to achieve higher DOP and simultaneously address the reliability issue. A triple-layer coating, consisting of a bottom layer of DuPont PI 2611, a middle layer of Dow BCB, and a top layer of DuPont PI 2611, has been developed. This PI/BCB/PI triple-layer interlayer system has several advantages. First, it shows a DOP of over 90% because of the planarization property of BCB. Second, it exhibits the desirable mechanical properties of PI because of the top and bottom layers of PI 2611. The PI/BCB/PI interlayer system combines the advantages of both of



(a)



(b)

Figure 7. Surface profile data for the 5.6 μm thick PI/BCB/PI interlayer on a test chip: (a) after the first layer (5:1 PI 2611); (b) after the second layer (BCB 3022-46).

DuPont PI 2611 and Dow BCB. A total thickness of 5.6, 15, and 19 μm PI/BCB/PI interlayer systems were developed.

A 5.6 μm thick PI/BCB/PI interlayer system uses Dow BCB Cyclotene 3022-46, and thinned DuPont PI 2611. The bottom layer is 5-to-1 thinned PI (5 parts of PI 2611 with 1 part of thinner by volume), the middle layer is Cyclotene 3022-46, and the top layer is 1.5-to-1 thinned PI 2611. Each layer was fully cured at 300 °C for 1 h in nitrogen ambient. The spin-casting speed, after cure thickness, and DOP for the 5.6 μm thick PI/BCB/PI on the test chip are shown in table 2. The surface profiles were measured using the alpha-step surface profile measurement system after hard curing of each layer. Figure 7 shows the surface profile data after the first layer coat (5:1 PI 2611) and after the second layer coat (BCB 3022-46), which were scanned through the direction given in figure 2(a). Prior to deposition of any interlayer, the test feature thickness was 4.5 μm as stated (figure 3). The thickness of the test feature after the first layer coating (5:1 PI 2611) decreased from 4.5 to 3.8 μm (figure 7(a), DOP of 15.6%). Subsequently, it decreased from 3.8 to 0.3 μm (3 000 Å in figure 7(b), DOP of 93.3%) after the second BCB coat. As seen in figure 7, there is no significant difference between the DOP of the widest line/spacing (20 μm each) and the smallest line/spacing (4 μm each), meaning that the DOP does not depend on the lateral dimension in our test cases. However, it should be noted that in our test case and measurement methodology there is no capability to measure the exact depth and profile for narrow line/spacing test features (test features narrower than 10 μm) due to the large size of stylus used (stylus radius of 5 μm) in the surface profile meter. Similarly, 15 μm thick and 19 μm thick PI/BCB/PI interlayer systems were also developed using BCB Cyclotene 3022-57 and 3022-63, respectively, with undiluted PI 2611. The spin-casting speed, after-cure thickness, and DOP for the 15 μm thick and 19 μm thick PI/BCB/PI systems are shown in table 3 and table 4, respectively. The PI/BCB/PI interlayer system could be realized from 3 μm to as thick as 55 μm with various combinations of thinned/pure PI 2611 and BCB. When the total thickness of the system is decreased (thinner than 3 μm), pin-hole-like defects are observed after high-speed, spin-casting of the thinned PI 2611.

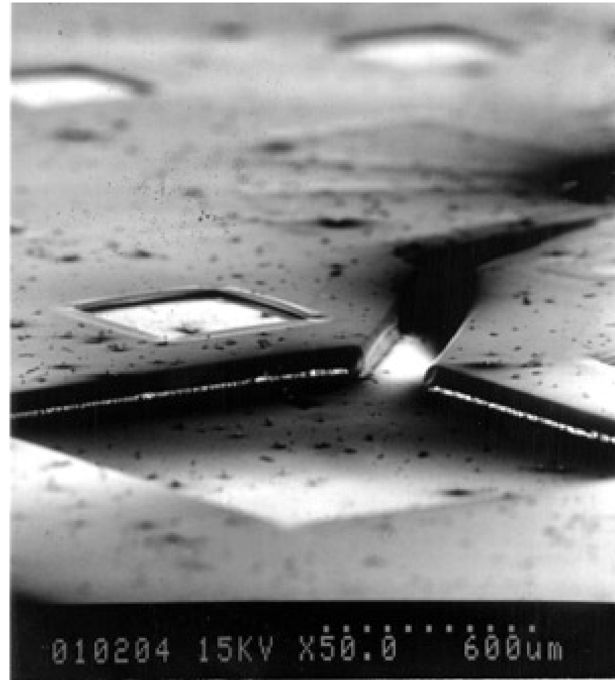


Figure 8. Scanning electron micrograph for a micropump consisting of the PI/BCB/PI interlayer system that shows straight sidewall fluidic channels.

In actual applications of these interlayers to vertically integrated MEMS, interconnection between micromachined devices and the underlying silicon circuitry will be required. To test this, RIE was used to define via holes in the interlayers deposited on the test chip. Various gas mixtures, powers, and pressures were investigated to develop two different via hole shapes; one for a nearly straight sidewall, and the other for a sloped sidewall (in the range of ~45–80°). The former could be useful in the application of vertically-stacked integrated MEMS using electroplated metallic MEMS techniques, while the latter could be useful in the application of general MCM-D. When straight sidewalls are needed (e.g., a vertically integrated micropump [21], figure 8), pure oxygen plasma (50 sccm) was used with a pressure of 300 mTorr and a power of

Table 5. Summary of the test parameters of the thermal cycling tests.

	Test						
	A		B		C		D
Number of cycles	1	5	1	5	1	5	5
Low extreme	−70 °C		−70 °C		−70 °C		−70 °C
High extreme	85 °C		125 °C		200 °C		350 °C
Time at each extreme	15 min		15 min		15 min		15 min
Max time from low to high extreme	1 min		1 min		1 min		1 min
5 μm PI 2611 on test chip	Pass	Fail	Fail	Fail	Fail	Fail	Fail
5.6 μm PI/BCB/PI system on test chip	Pass	Pass	Pass	Pass	Pass	Pass	Fail

300 W. A gas mixture of 47.5 sccm of oxygen (O_2) and 2.5 sccm of trifluoromethane (CHF_3), pressure 450 mTorr and power 300 W, was used to define an approximate 45°–55° sidewall slope for a PI/BCB/PI interlayer system. Scanning electron microscopy (SEM) photomicrographs for via holes of the PI/BCB/PI interlayer system on test chips are shown in figure 9.

6. Thermal shock and thermal cycling tests

Thermal shock and thermal cycling tests were performed to investigate the reliability of the PI/BCB/PI interlayer system as well as a single layer of PI 2611, which were spin-cast and cured on test foundry chips. Detailed test steps were taken from the military standard MIL-STD- 202F entitled Method 107G Thermal Shock [22].

A multichamber test apparatus, consisting of a cooling chamber and a heating chamber, was used to perform the thermal shock/thermal cycling tests. The cooling apparatus consisted of a stainless-steel cylindrical chamber surrounded by an insulating material and capped by an aluminum covered insulated lid. An aluminum-coated Pyrex beaker was placed in the bottom of the chamber and filled with dry ice. A Teflon tube ran from the center of the Pyrex beaker to the outside of the chamber. The tubing was connected to a siphoning system of acetone reagent. Acetone was siphoned into the beaker over the dry ice causing the dry ice to sublimate, creating a temperature of approximately −70 °C. A low-temperature thermometer monitored the chamber atmosphere temperature. Two heating chambers were used to create the necessary high-temperature atmospheres. A Cole–Parmer laboratory oven was used to perform all tests below 200 °C. For temperatures above 200 °C, a Thermolyne hotplate was used. To isolate the samples in the heated atmosphere, a Pyrex petri dish was placed over them. After the minimun temperature was reached in the cooling chamber, the samples were placed on a glass slide and cooled for 15 min. The samples were taken out of the cooling chamber and placed immediately in the high-temperature oven or on the hotplate. The maximum time delay was less than 1 min. The samples were heated for 15 min and then transferred back to the cooling chamber and the test repeated. As shown in table 5, a cycle is defined as 15 min in the cooling chamber and 15 min in the heating chamber. After each test was performed, the samples were examined under a microscope for defects. The criterion for the failure of the thermal shock/cycling tests was whether there was any mechanical failure (such as cracks) observed using optical or electron microscopy on the surface of the tested interlayers.

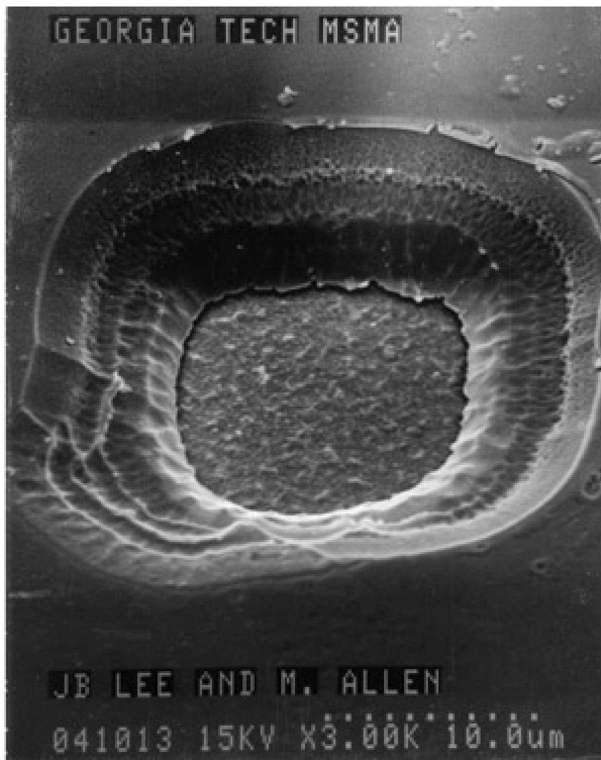
Samples used for thermal shock/cycling tests were a 5 μm thick PI 2611-coated test chip and a 5.6 μm thick PI/BCB/PI coated test chip. The 5 μm thick PI 2611-coated test chip failed the thermal cycling tests after test A-5. Figure 10 shows the photomicrograph of the top view of the 5 μm thick PI 2611-coated test chip after the A-5 cycle. The defects increased across the sample during the subsequent thermal cycling tests. During test D-5, the defects started to turn black and charred. In contrast, the 5.6 μm thick PI/BCB/PI interlayer system on the test chip did not show signs of failure until test D-5. Figure 11 shows the photomicrographs of the top view of the 5.6 μm thick PI/BCB/PI system coated test chip after the C-5 and D-5 cycles. As can be seen in figure 11(b), cracks on the PI/BCB/PI interlayer were observed after cycle D-5. An SEM picture was taken and it shows the side view of the crack at the surface of the PI/BCB/PI interlayer at one corner of the test chip. Table 5 shows a summary of the test parameters of Method 107G Thermal Shock and test results on both systems tested.

7. Study on $SiO_2/BCB/SiO_2$ interlayer systems—an alternative to the PI/BCB/PI system

In some applications it may be desirable to have inorganic coatings comprise the outermost layer of an interlayer dielectric system. In this case, the multilayer system discussed above can be substituted with a BCB/SiO_2 interlayer system or an $SiO_2/BCB/SiO_2$ system. Such a system combines the planarizing properties of BCB with the mechanical properties of inorganic SiO_2.

These interlayer systems consist of spin-cast, cured BCB, and a thin SiO_2 layer (approximately 2000 Å), which is deposited using PECVD. The BCB (Cyclotene 3022 series) is spin-cast and cured and the SiO_2 layer is deposited using 400 sccm of silane (SiH_4) and 900 sccm of nitrous oxide (N_2O) with a power of 20 W and a pressure of

(a)



(b)

Figure 9. Scanning electron micrographs for via holes of the PI/BCB/PI interlayer system that shows sloped sidewalls at etched via holes: (a) array of via holes; (b) a close-up view of a via.

0.9 Torr on a 200 °C heated substrate. Since SiO_2 has a well matched coefficient of thermal expansion (CTE) of 3.9 ppm/°C [8] to silicon (CTE of 2.3 ppm/°C) [18], it is expected that the $SiO_2/BCB/SiO_2$ system is also suitable as an interlayer for applications where temperature changes/cycling have the potential to induce structural failures, although such cycling experiments were not performed on this system. This system also shows high DOP (over 95%) that is suitable as an alternative to the PI/BCB/PI system.

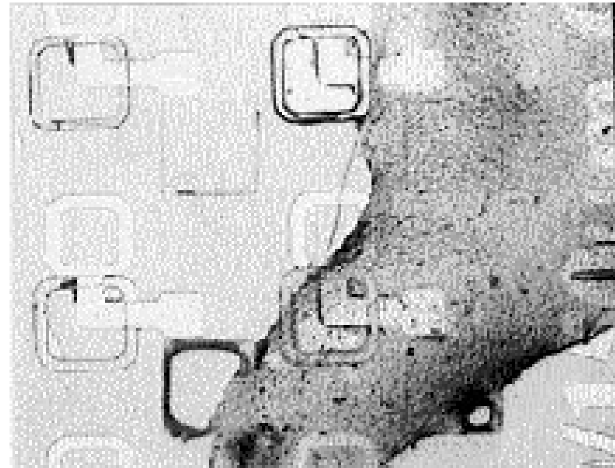
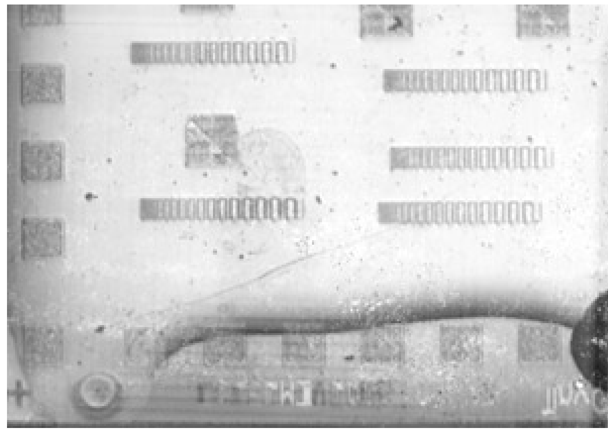


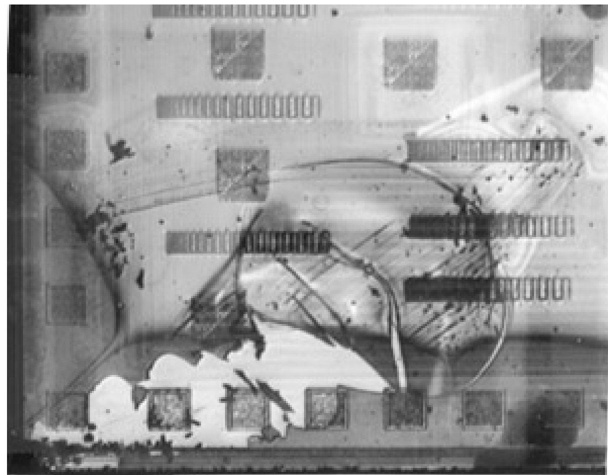
Figure 10. A photomicrograph of the top view of the 5 μm thick PI 2611-coated test chip after the thermal cycle A-5.

8. Special considerations on small chip processing

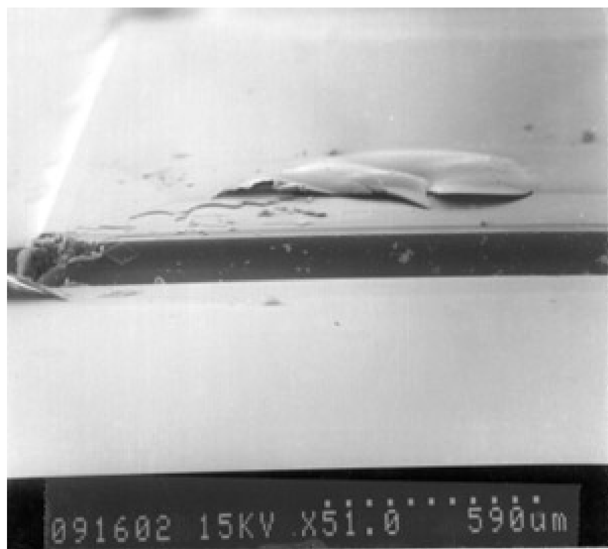
In actual applications, the production of vertically integrated MEMS would most likely take place on whole wafers; however, for prototyping or other smaller volume situations, chip-level prototyping (e.g., by processing a chip produced as part of a multiproject wafer) might be required. Several special considerations should be given to the processing of small (a few millimeters on a side) foundry-fabricated chips. First, since foundry-fabricated chips are too small to conveniently handle during many processing steps, they should be attached to other substrates, such as silicon wafers or glass. Second, as is well known, in the spin-casting process, accumulation of spin-cast materials is observed on the edge of tiny chips (the so-called 'edge bead'). The edge-bead phenomenon is not a serious problem for larger wafers; however, in the case of small foundry-fabricated silicon chips, the edge bead may cover a significant area of the chip. As described above, 3 mm on a side MOSIS Tiny-Chip [15] test chips were used to develop appropriate interlayer systems. Figure 12 shows a measured surface profile after 5.6 μm thick PI/BCB/PI is spin-cast and cured on the chip. Figure 12(a) shows the surface profile for the center-to-center scanned data and figure 12(b) shows the corner-to-corner scanned data. As shown, for each side, around 17% of the total length of the chip shows hill-like, edge-bead structures. The edge bead alongside the chip is approximately 8.0 μm and at the corner of the chip approximately 9.8 μm, while the planarized center areas are 5.6 μm thick. The thickness of



(a)

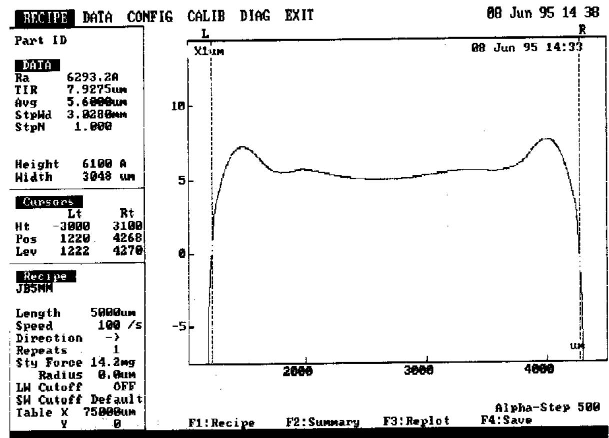


(b)

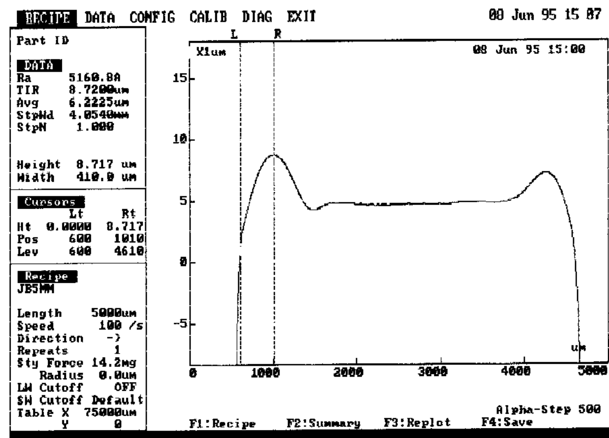


(c)

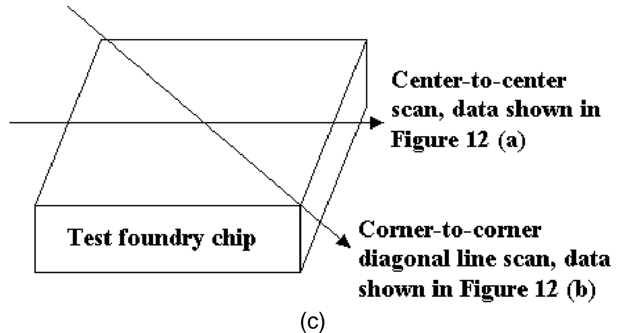
Figure 11. Photomicrographs of the top view of the 5.6 μm thick PI/BCB/PI-coated test chip after (a) the thermal cycle C-5, passed and (b) cycle D-5, failed; (c) an SEM photomicrograph of the side view of the crack on the PI/BCB/PI interlayer after the cycle D-5.



(a)



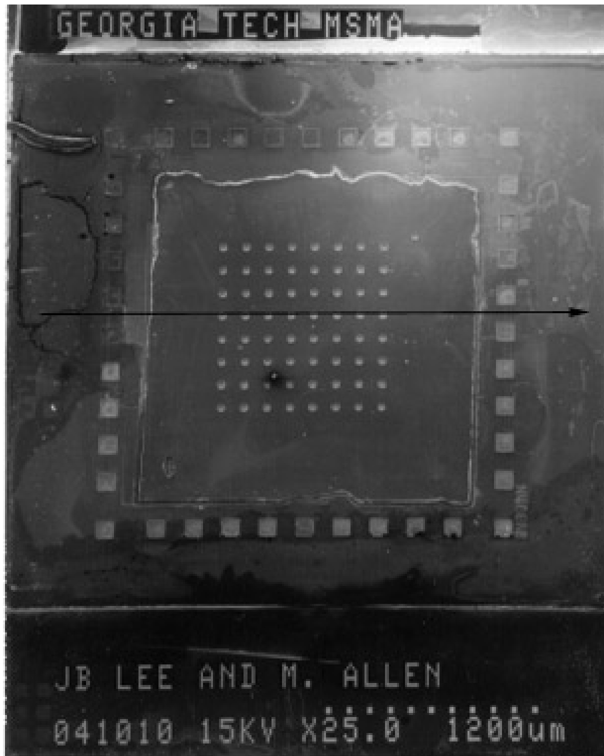
(b)



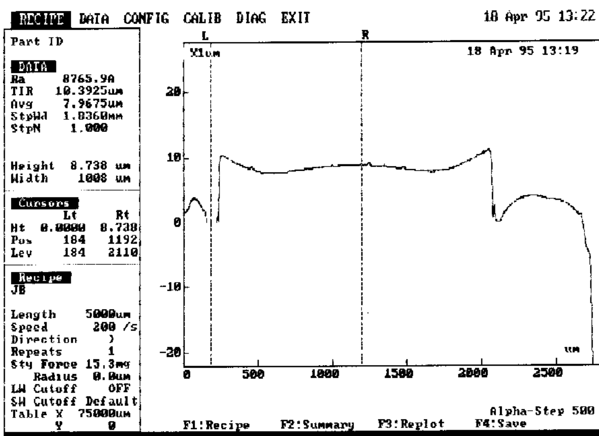
(c)

Figure 12. Surface profile data of the 5.6 μm thick PI/BCB/PI system on a foundry-fabricated test chip: (a) center-to-center scanned data; (b) corner-to-corner, diagonal scanned data; (c) scanning direction.

the edge bead heavily depends on the spin-casting speed of the BCB layer. The lower the spin-casting speed of the BCB layer, the higher the edge bead. If needed, the hill-like, edge-bead areas could be removed by RIE and the center areas subsequently used for micromachined device patterning. Figure 13 shows the top view photomicrograph of a foundry-fabricated chip after the edge-bead areas have been removed. As shown, the additional edge-bead removal step could be used to render the center areas suitable for subsequent fabrication processes to realize vertically integrated MEMS.



(a)



(b)

Figure 13. (a) A photomicrograph of the top view of the foundry-fabricated chip after the edge bead removal; (b) the corresponding surface profile data through the scanned line.

9. Conclusions

Fabrication techniques required for vertically-stacked integrated MEMS on top of silicon circuitry wafers/chips have been described with emphasis on the development of suitable interlayer systems. A PI/BCB/PI interlayer system has shown a DOP of over 95% as well as has passed the Method 107G Thermal Shock from the military standard MIL-STD-202F [22]. A BCB/SiO_2 interlayer system and a SiO_2/BCB/SiO_2 interlayer system have also been investigated as alternatives to the PI/BCB/PI system. Edge beads of interlayer materials which accumulate during the processing of small chips could be removed by RIE and the remaining center areas of the chips used for interconnect and microstructure fabrication. The combination of the interlayer system (a PI/BCB/PI system, a BCB/SiO_2, or a SiO_2/BCB/SiO_2 system) and subsequent electroplating-based metallic micromachining techniques offers the possibility to realize low-cost manufacturing of additive, vertically-stacked integrated MEMS.

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