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MICROMACHINED FLEXIBLE INTERCONNECT FOR WAFER LEVEL PACKAGING

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ABSTRACT

Wafer Level Packaging (WLP) of microelectronic circuitry, in which critical package elements are formed on the silicon wafer prior to dicing, has several advantages over conventional packaging techniques, such as one-step testability of multiple chips on a silicon wafer prior to dicing, and the possibility of high input-output (I/O) density. One of the critical elements of WLP is the interconnect. Freely movable interconnects, which act like springs when thermally and mechanically loaded, can be used to relieve thermal and bonding-generated stresses, potentially resulting in improved testablility and reliability in WLP. In this work, flexible free-standing and no-underfill inteconnects were fabricated in a CMOS-compatible surface micromachining technology directly on a silicon wafer. The compliance of these interconnects up to 50 microns in the direction normal to the wafer was measured. Deflections and thermal expansions under mechanical-thermal stress were also simulated using finite element methods. Good agreement was achieved between the measured compliance and that predicted by the finite element analysis.

INTRODUCTION

Advances in electronic packaging from the DIP (Dual Inline Package) to the CSP (Chip Scale package), have mirrored the advances in shrinking integrated circuit (IC) feature sizes, resulting in extremely compact microelectronic systems [1-5]. In recently developed advanced electronic devices, additional considerations need to be satisfied such as lower cost and smaller, thinner, and lighter packaging of ICs [2-4, 6-7]. Wafer Level Packaging (WLP) of microelectronics, in which packaging passivation and leads are formed on the silicon (Si) using the same semiconductor infrastructure and micro-fabrication techniques as those used to fabricate portions of the ICs themselves [5], [8-9], has numerous merits that include a smaller number of processing steps, one-step testability of multiple Si circuits prior to dicing, and the possibility of high I/O density. In general, WLP is characterized by the following attributes [1-9]:

1) *Batch fabrication*: WLP is fabricated on a wafer unit. This means the packaging is realized using batch fabrication. This advantage also yields a potential cost reduction.

2) *Reduction in processing complexity*: Conventional electronic package processing is significantly more than its fabrication alone, and is composed of the following steps: *fabrication, dice, packaging (mounting and bonding) of individual ICs, burn-in and functional test*. However, the WLP uses only three main steps: *fabrication, burn-in and test on wafer level, dice*. This approach greatly reduces the time and labor for test and fabrication per chip.

3) *Better reliability and testability*: In conventional packaging approaches, ICs were diced into individual chips after testing and burn-in processing. Using WLP, dice are only handled in packaged form. Smaller handling time gives better reliability.

4) *Low cost*: Reduction of the number of processing steps and wafer-level (as opposed to die-level) test/burn-in lowers the cost per die.

Although WLP offers advantages in terms of ease of processing and lower cost, a problem that arises is the thermal mismatch between the printed wiring board (PWB) and the Si die when a solder ball itself acts as the interconnect. Also, the difference in height between the solder balls and the non-uniformity of the PWB surface can present problems while testing. These problems are exacerbated as the physical size of the Si chip and the number of I/O increase, which is precisely an area of application of great promise for WLP. In this paper, freely-movable interconnects fabricated using micromachining technology, which can compensate for PWB nonuniformity and thermal stresses, are presented. These interconnects can deform elastically in response to thermal or mechanical loads,

thereby potentially increasing testability and reliability in WLP.

DESIGN AND FABRICATION

The primary goal of the design is to obtain flexible interconnects for WLP. Three flexible interconnect types are fabricated using surface micromachining technology followed by electroplating. The schematic of these structures is shown Figure 1.

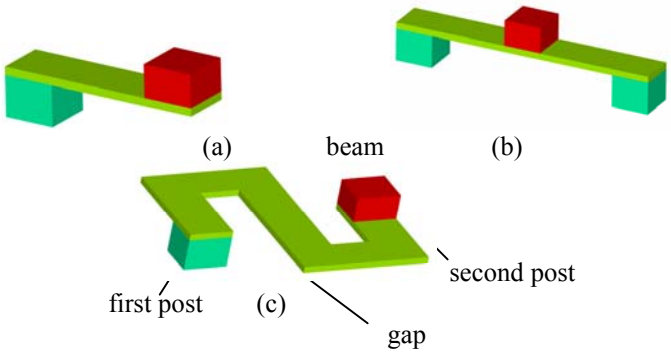

Figure 1: *Schematic of surface micromachined interconnects. (a) Step type (b) Bridge type (c) Semi- spiral type.*

Figure 1(a)–(c) show three different geometries of flexible interconnect labeled stair, bridge, and semi-spiral type. The required vertical deflections of each type of interconnect were assumed to be 20-30um by considering the typical roughness of the PWB (10-15um) surface and of the non-uniform height of the solder bump (10-15um). The design also considered the potential for thermal horizontal expansion by calculating the difference of the coefficient of thermal expansion (CTE) for the Si die and PWBs. An estimate of the required horizontal deflection was obtained by considering the CTE mismatch between PWB (20ppm/°C) and Si (2.6 ppm/°C), a temperature cycle of 100°C, and a typical die area of $1cm^2$ to obtain 8.6um. If chip sizes expand to 2.75cm on a side (as slated in the ITRS roadmap for 2010), the horizontal expansion requirement increases to approximately 20um. Stair and bridge type interconnects were designed for vertical movement, while the semi-spiral was designed to accommodate both horizontal expansion and vertical deflection.

Each interconnect is composed of three electroplated Cu structures: the first post, the beam, and the second post, as illustrated in Figure 1. The first Cu post acts as an anchor point and electrical connection to the silicon substrate. The size of the first post is 50um × 50um × 50um. The second electroplated Cu structure, which has 50um × 10um cross-sectional area, and which will be moved when external loads (mechanical force, pressure, or heat) are applied on the die or on the system, is fabricated in 6 different lengths for assessment purposes. The beam length of all interconnect types (from right edge of first post to left edge of second post) varies from 100um to 200um in increments of 20um. In the case of the semi-spiral, two gaps and the beam width determine the beam length. Solder bumps can be placed on the 50um × 50um × 40um Cu post that is plated on the second movable beam. Also, this post pad can be used for mechanical measurements. These three different Cu electroplated layers are connected by a sequential electroplating process.

The flexible interconnect fabrication process is based on CMOS-compatible plating-through-mold technology [10], followed by standard surface micromachining to release portions of the interconnect and achieve flexibility. The stair type interconnect fabrication process is described in Figure 2. The fabrication processes for the other flexible interconnects are similar to the process for the stair type. To provide insulation and mimic the surface of a conventional CMOS chip, the silicon wafer is coated with a passivating SiO_2 layer (490 nm) using PECVD as shown Figure 2a.

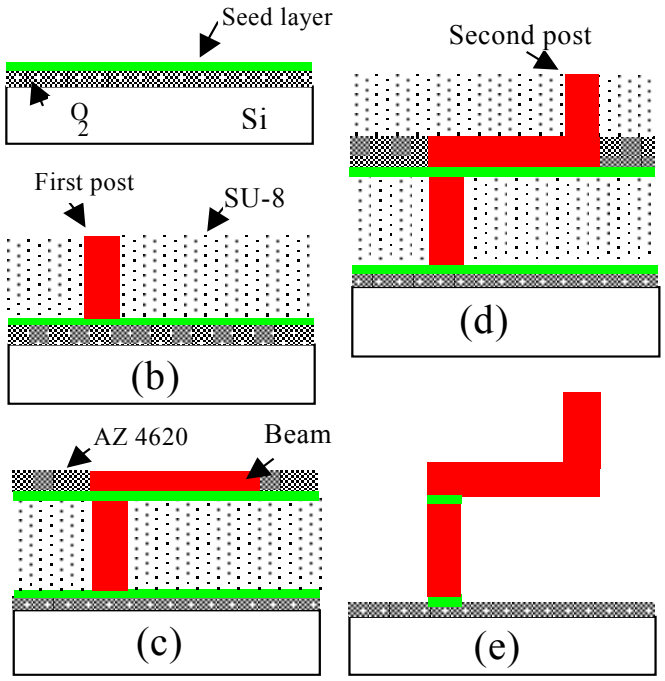

Figure 2: *Fabrication process of flexible interconnect.*

A seed layer for electroplating consisting of a Ti/Cu/Ti multiplayer stack (30 nm /250 nm /30 nm) is then deposited. On this layer, an electroplating mold 50 um in thickness is formed using photosensitive epoxy (SU-8, Microchem, Inc.) and patterned using a conventional CMOS photolithography process. The mold is then filled to the top using a Cu electroplating bath. Figure 2b shows the first electroplated Cu post which is 50um in height. A second seed layer (identical to the first layer) is sputtered for electroplating the Cu beam and second Cu post. Using a thick positive photoresist (AZ 4620, Hoechst Celanese) and electroplating in a similar manner to the

first post, a Cu beam is formed as shown Figure 2c. After removal of the positive photoresist layer, the epoxy resist and electroplating process is repeated to form a 40 um second Cu post (Figure 2d). After the formation of the electroplated Cu structures, the polymers are etched away to release the final compliant structures as shown Figure 2e.

Figure 3 shows the optical photomicrograph (a) and SEM (b) of the fabricated structures. Figure 3a shows, from top to bottom, stair, bridge, and semi-spiral flexible structures fabricated on a 1cm × 1cm Si die, with each die having 16 × 16 = 256 flexible interconnects. The SEM pictures on Figure 3b are for 100um length structures of each interconnect type. Because each interconnect type has different beam lengths, the pitch of the structures is fixed at 500um. The pitch size can be scaled down by mask design; i.e., the number of interconnects can be determined in the design step. By simple calculation, 10,000 interconnects can be fabricated on a 1cm × 1cm Si die with a 100um pitch. This high packaging density that is possible is another advantage of surface micromachined flexible interconnects.

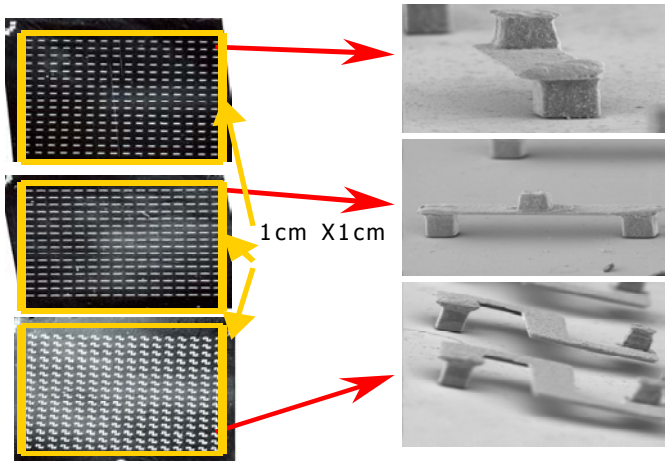

Figure 3: *Photomicrograph (a) and scanning electron micrograph (b) of fabricated surface micromachined flexible interconnect structures.*

SIMULATION AND MEASUREMENT

Simulations of the flexible interconnects are performed for both the mechanical (vertical) deflection and thermal (horizontal) expansion using a 3D FEM simulation program, ANSYS 5.6. Also, the electrical properties of the interconnects are calculated with MEMCAD 4.8.2 (Coventor, Inc). The mechanical simulation is performed for the three different interconnect types with 100um beam lengths. Unlike the mechanical simulation, the thermal effects of only the semi-spiral type interconnects were calculated under a 100degree C thermal load. The material properties for simulation are given in Table I. The silicon die and the PWB are both 1cm × 1cm in area and 500um thickness for the thermal simulation. The solder bump is assumed to be 50um × 50um × 50um.

Table I: *Material properties of flexible interconnect*

Materials	Young's Modulus (GPa)	Possion's ratio	CTE (ppm/°C)
Silicon Die	130	0.23	2.62
Cu Lead	129	0.34	16.7
Solder bump (Sn/Pb)	32.58	0.37	24.2
PWB	20.68	0.14	20

The measurement system consisted of a probe station equipped with a small scale on the probe chuck. The wafer was placed on the scale and a micromanipulator probe tip was utilized to apply mechanical load to the interconnect structure as shown in Figure 4. The total force applied to the interconnect structure could then be measured by the scale, while the deflection could be measured by determining the vertical travel of the microscope head necessary to keep the tip of the deflecting interconnect structure in focus.

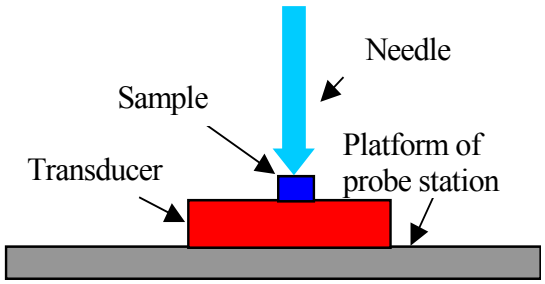

Figure 4: *The measurement system for mechanical deflection of the interconnects.*

Three geometries were tested: the stair-type, the bridge-type, and the semi-spiral-type structures. When force is applied to the stair type connector, the connector is totally bent to the substrate surface (tip deflection of 50 microns) for 0.02mN of applied load and remains deformed after removal of the load. A permanent plastic deformation is observed. From the simulation that is described as Figure 5, the stress on the neck (A-A') of the movable beam is over 250MPa under a load of 0.02mN. Noting that the bulk yield stress of copper is typically quoted as between 50 and 700MPa, the simulation and experimental results agree well. For the bridge type, no noticeable deflection was observed even under 0.3mN of load. From the simulation of this shape, the maximum deflection was under 4um. In addition to mechanical compliance, electric current density was measured with this structure. The structure can withstand 4A of applied current before fusing. By simple calculation, the current density is approximately $4 / (50e\text{-}6)^2 = 0.2e10[A/m^2]$.

This result indicates the Cu electroplated interconnect can be used as a high power I/O interconnect.

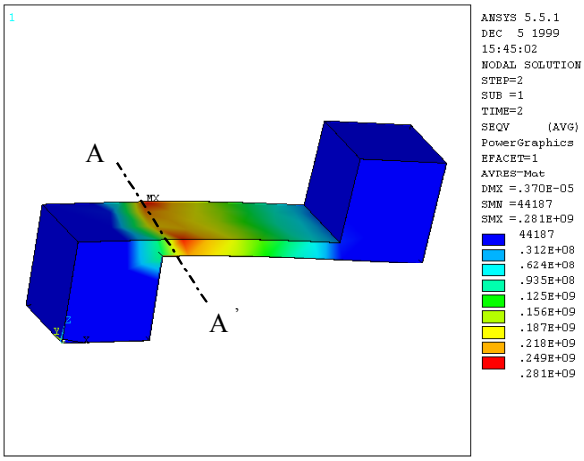

Figure 5: *Stress simulation of stair interconnects with 0.02mN applied load.*

For the semi-spiral type connector, a promising result was obtained. This structure acted like a spring (Figure 6); no permanent plastic deformation was detected for loads up to 0.03mN.

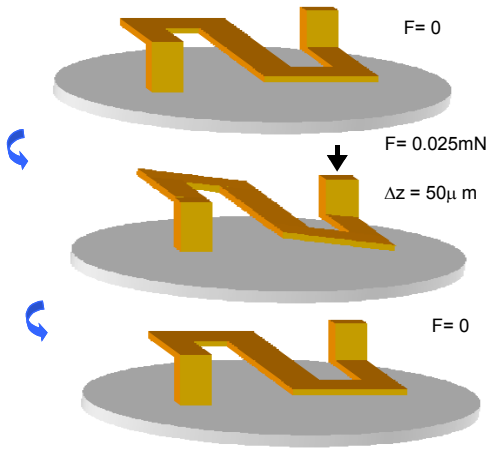

Figure 6: *Semi-spiral type interconnect acting like a spring under 0.02mN applied load.*

Experimentally, this structure would easily bend for loads ranging from 0.02mN to 0.03mN, giving a total deflection of 50 um at these load levels. These results agree well with the simulation as shown in Figure 7. Figure 8 shows the simulation and measurement data for displacement vs. force. They agree very well and have almost the same trend-line.

In the thermal simulation, a 100°C temperature is uniformly applied to an entire chip/interconnect/PWB system which consists of a 1cm × 1cm Si die with 500um thickness, the semi-spiral Cu interconnect, a 50um × 50um × 50um solder bump, and 500um thick PWB.

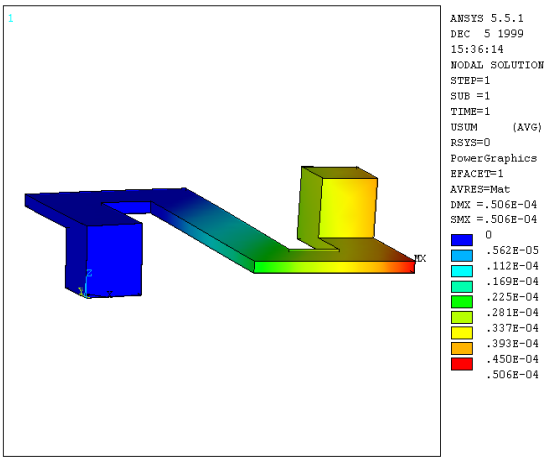

Figure 7: *ANSYS simulation for semi-spiral type interconnects with 0.025mN load.*

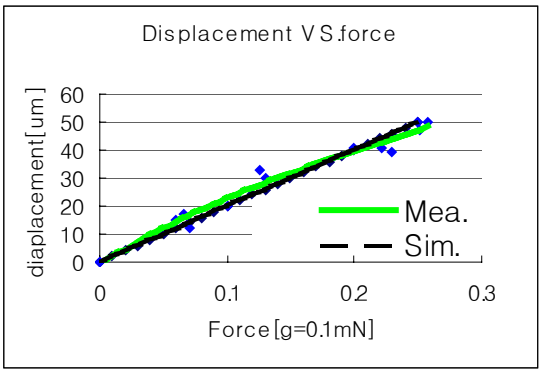

Figure 8: *Comparison of measurement and simulation data for displacement of semi-spiral type structure.*

The thermal simulation is executed with three assumptions: 1) no expansion occurs at the center of the system due to the uniform distribution of the heat; 2) each layer (Si die, Cu-lead, solder bump, and PWB) of the system is very well thermally connected (i.e., the system is isothermal); and 3) the structures are arranged directionally (i.e. the X and Y-axes have the same number of interconnects and the interconnects are oriented in the same direction). By making use of symmetry, the total modeled system is designated to have dimensions of 0.5cm × 500um × 1150um as shown in Figure 9. Figure 9a shows the thermal expansion of the designed system. The maximum expansion is approximately 10um on the PWB. With this expansion, the stress simulation result is as shown as in Figure 9b. The maximum stress occurs on the outermost structures along the X and Y-axes, and the stress is concentrated on a small portion of that structure. Finally, a simple manual horizontal deflection test was performed on the interconnect to verify the mechanical flexibility of the structures. This simple experiment demonstrated elastic deformation of the

interconnect in excess of the 10 micron deflections required by the simulation and gives assurance that the X and Y displacement of the interconnects will be sufficient for the designed system.

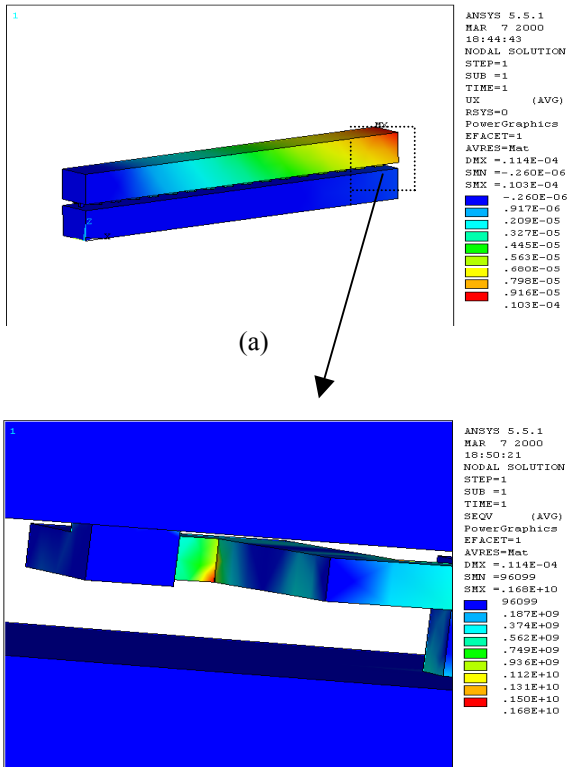

Figure 9: *Thermal expansion and resultant stress for16 semi-spiral interconnects under 100 degree* C *temperature variance.*

A preliminary simulation of the electrical properties of the interconnects with 100um beam length at 1 GHz was performed using the FEM simulation tool MEMCAD 4.8.2. Simulation of only the resistance and inductance were performed. Although the results of the simulation are preliminary, they indicate superior electrical performance due to lowered package parasitics. The results of the simulation are shown in Table II.

Table II: *Electrical properties of interconnects at 1GHz*

Interconnect type	Resistance[mΩ]	Inductance[nH]
Stair	16.1748	0.06998005
Bridge	16.9742	0.06990578
Semi-spiral	64.9272	0.1824060

CONCLUSION

A flexible interconnect technology for WLP has been proposed and demonstrated. This flexible micromachined interconnect is compatible with standard back-end CMOS processing and combines electroplating of copper lines with surface micromachining technology. Fabricated structures have demonstrated the compliance required in typical WLP applications. The mechanical, thermal and electrical properties are simulated with 3D FEM simulation tools, ANSYS and MEMCAD. Measured mechanical results for vertical compliance agree well with simulation predictions.

ACKNOWLEDGEMENT

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