Embedded Solenoid Inductors for RF CMOS Power Amplifiers

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SUMMARY

The fabrication of a surface micromachined, epoxy-embedded, high-Q electroplated inductor, and the simultaneous integration of four of these devices with a foundry-fabricated CMOS RF power amplifier, is described. The embedded nature of these inductors allows conventional handling and packaging of inductor/chip systems without additional consideration for the inductor structure. A 6-turn inductor fabricated on silicon shows a peak Q-factor of 20.5 at 4.5 GHz and an inductance of 2.6nH. To demonstrate the technology, a power amplifier was implemented in a 0.24-μm CMOS foundry technology. Four inductors were integrated on the power amplifier. The resultant system demonstrated a gain of 6.7 dB at 0.8 GHz.

Keywords: *embedded solenoid inductor, high-Q, CMOS integration, electroplating*

INTRODUCTION

Many RF systems, e.g. cellular phones, pagers, GPS receivers, and Bluetooth transceivers, motivate the integration of passive inductors with CMOS circuitry. It has been demonstrated previously that such inductors can be fabricated in a CMOS-compatible fashion [1-3]. An important issue for integrated RF inductors on silicon is minimization of parasitic effects, e.g., coupling capacitance between the inductors and the substrate, and losses caused by induced eddy currents in the substrate. To reduce these parasitics, various techniques have been employed for conventional spiral-type planar inductors, such as bulk etching the Si underneath the inductors [4-5], using a high-resistivity Si substrate or Si on sapphire [6-7], and introducing a large gap between inductor and substrate [1]. As an alternative to the planar-type spiral inductor, 3-D solenoid-type inductors using MEMS surface micromachining have been suggested for high Q-factor and low substrate coupling [2-3]. A drawback to many of these approaches is that the resultant etched wafers and/or inductor structures may be too delicate to withstand subsequent conventional injection-molding-based or other chip packaging approaches.

In this research, surface micromachined, epoxy-embedded, high-Q electroplated inductors have been fabricated. These inductors combine the desirable features of: (1) being supported by both electroplated posts and a deposited thick dielectric layer, thereby separating them from the lossy silicon substrate; and (2) being embedded in the epoxy molds from which they are formed, minimizing microphonics and allowing sufficient mechanical stability such that the chips bearing the inductors can be packaged using standard injection-molding processes. An additional processing benefit from the embedded structure is that the epoxy mold used to form the inductors need not be removed in a lengthy etch step. To demonstrate the compatibility of the reduced-parasitic, embedded inductor process with CMOS circuitry, four inductors are post-processed onto a foundry-fabricated RF CMOS power amplifier.

DESIGN AND FABRICATION

The schematic of an embedded solenoid inductor is shown in Fig. 1, where the embedding mold layer is omitted in Fig. 1(a) for the purpose of structural clarity and is presented in Fig. 1(b). A variety of inductor geometries were designed and analyzed using MEMCAD [8]. The main considerations for the design are: (1) to reduce coupling effects between the Si substrate and the coil by separating them by a substrate

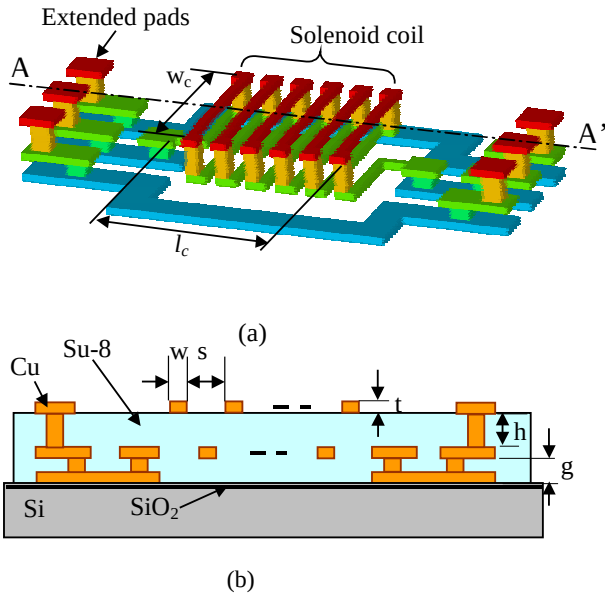


Fig. 1: *Schematic of solenoid inductor. (a) perspective view (SU-8 mold is not illustrated for structural clarity); (b) cross-sectional view of A-A'.*

gap, *g;* and (2) to reduce turn-to-turn stray capacitance between the lines by orienting the lines in parallel [2] and by adjusting the spacing between lines, *s*, and the layer-to-layer core height, *h*. In the final design, a line spacing, *s*, core height, *h*, and gap, *g*, of 60 μm, 40 μm, and 25 μm, respectively, were used. The thickness, *t*, of the metal layers was 10μm and the line width, *w*, of the coil was 20μm. Since the skin depths of copper at 1GHz and 10GHz are approximately 2μm and 0.66μm, respectively, the designed *w* and *t* are not a limiting factor for high-Q inductors. In addition, inductors with varying numbers of turns and varying solenoid core width, w_c, were analyzed. To enable electrical probing of the test inductors, extended pads were designed since the inductor structure itself will be inaccessibly embedded in epoxy.

The inductor fabrication process is based on photosensitive epoxy (SU-8, Microchem, Inc.), negative photoresist (NR9-8000, Futurrex, Inc.), and copper (Cu) electroplating. The fabrication processes for test inductors and for inductors fabricated on CMOS circuitry differ slightly. For the test inductors, the first layer is Cu and is patterned to form grounds in a ground-signal-ground (G-S-G) configuration as well as to form the extended pad connection. For the CMOS integrated inductors, the first layer is made from Cr/Au and is in contact with a CMOS Al pad. The rest of the process is the same for both inductors. Here the fabrication process for the inductor on CMOS is described.

Referring to Fig. 2a, a Cr/Au pad layer (200Å/3000Å) is deposited and patterned on the CMOS chip using a standard lift-off process. This layer serves as a contact layer between the CMOS circuitry and the inductors, and also protects the CMOS probe pads from the Cu electroplating bath. An SU-8 epoxy layer (25μm) is spin-coated and patterned for the first via definition (Fig. 2b). After seed layers (Ti/Cu/Ti) are sputtered, a thick (10μm) negative photoresist NR9-8000 is coated and patterned for the lower metal layer and the first via hole (Fig. 2c). Two metal layers (the first via hole and the coil lower metal layer) are formed simultaneously with a single electroplating step. After the first electroplating, the PR mold and seed layers are removed, but the SU-8 mold surrounding the via as well as the electroplated Cu structure remains. Note that both the via post and the SU-8 mold mechanically support the entire solenoid coil thereafter (Fig. 2d). The steps *(b)* through *(d)* are repeated for the next via (40μm thick) and the coil upper metal layer. Note that the core of the embedded inductor is filled with SU-8 (Fig. 2e). Since the core of the inductor has already been filled, and is mechanically robust, the inductance and Q-factor of the inductor are not expected to change after a subsequent packaging process, such as plastic injection molding. However, the electrical properties of the epoxy may influence the inductor properties in this configuration.

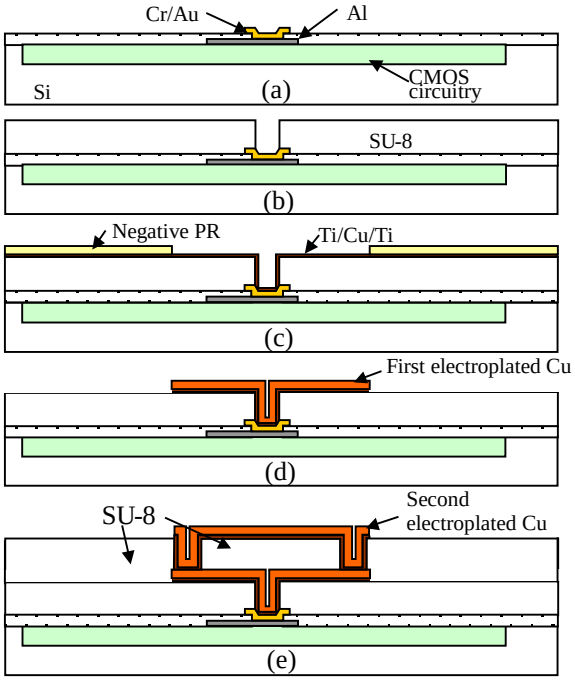


Fig. 2: *Fabrication process for the inductor on CMOS*

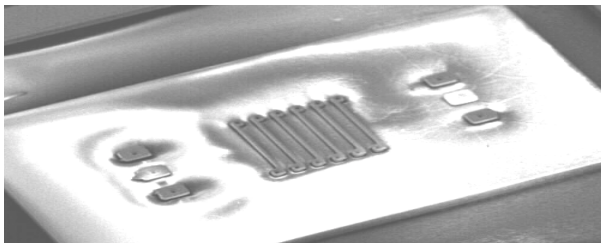
Fig. 3 shows an SEM view of a fabricated embedded inductor. This device is a test inductor and the extended probe pads can be seen as the three G-S-G pads on either side of the device (Fig. 3a). Fig. 3b shows an SEM view of the device after the embedding epoxy has been etched away for clarity. The solenoid coil is 25μm above the Si substrate. The coil width, *w*, is 20μm, the turn-to-turn pitch, *p (= w+ s)*, is 80μm, and the height of the solenoid core, h_c, *(= h+ t)* (i.e., the distance between the center of the lower metal layer of the coil and the center of the upper metal layer of the coil) is 50μm. The via has a cross-section of 25μm×30μm.

RESULTS

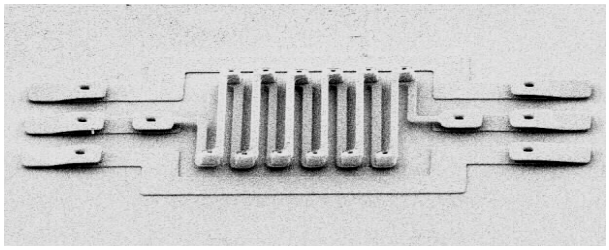
Results are divided into two parts: results of individual test inductors, and results of CMOS-integrated inductors.

Test Inductor Results

Fig. 4 shows the measured inductance and Q-factor of an embedded test inductor with 6 turns and a core width, w_c, of 400μm. The peak Q-factor and inductance at 4.5GHz are 20.5 and 2.6nH, respectively. The measured data were compared with a MEMCAD simulation for the same geometry. The results of measurement and simulation are consistent up to 6GHz.



(a)



(b)

Fig. 3: *SEM of the fabricated 6-turn embedded test inductor: (a) embedded; (b) after removal of SU-8.*

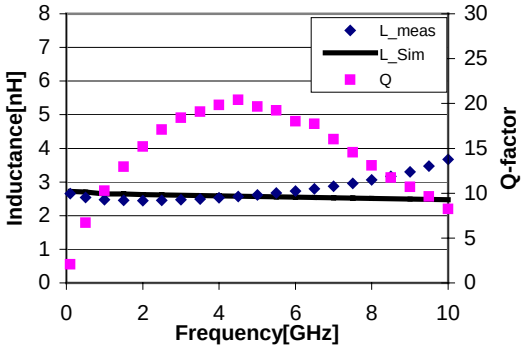


Fig. 4: *Measured inductance (diamonds) and Q-factor (squares) of an embedded test inductor (6 turns and 400μm core width) The solid line is a simulation of the inductance using MEMCAD.*

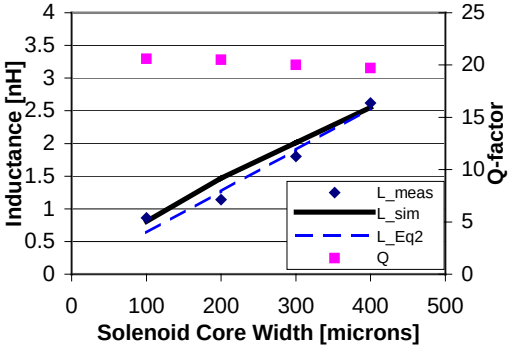


Fig. 5: *Measured inductance and Q-factor at 4.5 GHz of 6-turn embedded test inductors as a function of core width. Simulation (solid line) and fit to Equation (2) (dashed line) are also shown.*

The inductance for an ideal solenoid coil can be expressed in Eq. (1).

$$L = N^2 \mu_c \frac{w_c h_c}{l_c} \qquad (1)$$

where N is the number of turns, μ_c is the core permeability, w_c is the core width, h_c is the core height, and l_c is the core length. The micromachined solenoid-type inductor is not an ideal solenoid in the sense that the core is not cylindrical in shape and the wire is not wound closely enough only to have the magnetic flux inside the core. In addition, the geometric constraints of a single layer of winding yield a relationship between pitch and core length. As a result, the inductance for the micromachined solenoid-type inductors should be written as Eq. (2):

$$L = \kappa N \mu_c \frac{w_c h_c}{p} \qquad (2)$$

where κ is a constant of proportionality which may be determined by fitting to experimental data, and the geometric substitution $l_c = N\,p$, where p is the turn-to-turn pitch, has been made.

Fig. 5 shows the measured inductance and Q-factor, and simulated inductance, of 6-turn inductors at 4.5GHz as a function of core width (100μm, 200μm, 300μm, 400μm). The inductance data are also fitted using Eq. (2). Good agreement with Eq. (2) is observed. The best-fit constant of proportionality for this case is 1.35. A similar analysis for number of turns is shown in Fig. 6, with good agreement and a best-fit constant of proportionality of 1.25.

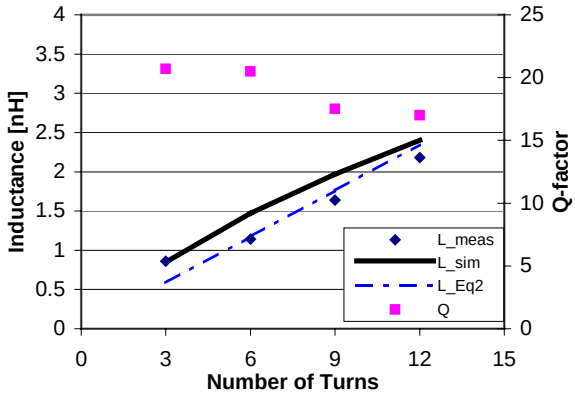


Fig. 6: *Measured inductance (diamonds) and Q-factor (squares) at 4.5 GHz of 200 μm wide embedded test inductors as a function of number of turns. The data are compared with simulation (solid line) and are fitted to Equation (2) (dashed line).*

Integrated CMOS Power Amplifier Results

A power amplifier with a single-stage common-source topology was designed as a test vehicle for the embedded inductors. The schematic diagram of the amplifier is shown in Fig. 7. The design utilizes four micromachined inductors and one integrated spiral inductor. The amplifier was fabricated using a 0.24-μm CMOS foundry technology. The die area of the amplifier is 1,860x1,180 μm^2. Following the foundry fabrication, the four embedded micromachined inductors were fabricated on the CMOS chip as described above. Fig. 8 shows an optical photomicrograph of the power amplifier with the integrated embedded inductors.

Upon testing (Fig. 9), the power amplifier integrated with inductors shows a gain of 6.7dB and a 20% maximum power added efficiency (PAE) when it is driven at 0.8GHz, with a power supply voltage V_{dd} of 2.5V and a gate DC bias V_g of 0.95V. These results indicate that the embedded inductors are performing successfully.

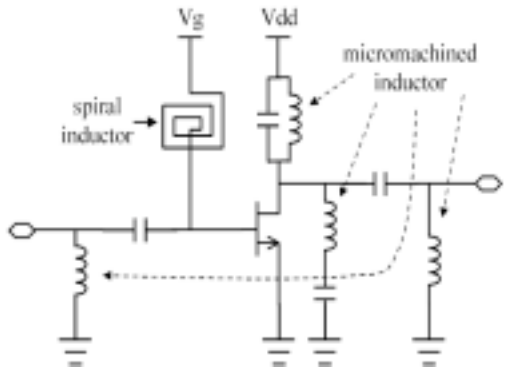


Fig. 7: *Schematic of power amplifier, showing locations of embedded inductors.*

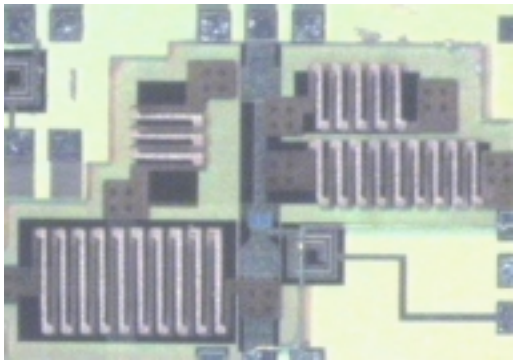


Fig. 8: *Photomicrograph of integrated power amplifier. Note the four embedded inductors.*

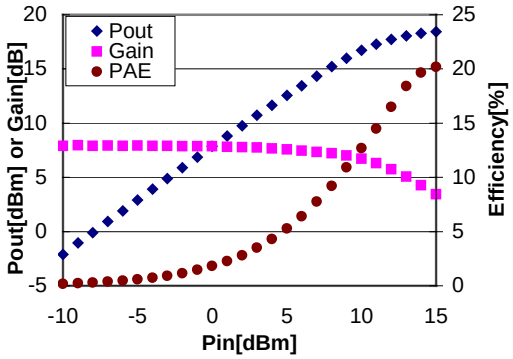


Fig. 9: *Output power, gain, and Power Added Efficiency (PAE) of the power amplifier with integrated embedded inductors at 0.8GHz*

CONCLUSION

A CMOS-compatible fabrication process has been demonstrated for embedded solenoid inductors. The process is based on surface micromachining with SU-8 molds and Cu electroplating. The embedded inductors show a Q-factor of up to 20 on Si substrates. To demonstrate compatibility with CMOS circuitry, inductors are formed on top of foundry-fabricated CMOS RF power amplifiers, and the resultant amplifiers were successfully operated. This integration of CMOS RF circuits with micromachined components can be a potential solution for packaging-compatible, compact, and high performance CMOS RF ICs.

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