Electroless Ni-P/Ni-W-P Thin-Film Resistors for MCM-L Based Technologies

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Abstract: A novel technique of fabricating MCM-L compatible integrated resistors on large area substrates is presented. Electroless plated Ni-P/Ni-W-P alloys are used to achieve resistivity values in the range of 5 - 50 ohm/square and absolute temperature coefficient of resistivity below 50ppm/°C, which is sufficient to satisfy many resistor application needs. Fine line structures (<50 μm linewidth) are achieved by a three step process: electroless plating a thin (100 - 200 Å) seed layer on patterned photoresist; lift-off of regions of the seed layer by dissolution of the photoresist; and electroless plating of the resultant structures in the seed layer to the desired thickness to achieve a specific sheet resistance. Improvements in seeding uniformity of the initial blanket seed layer were achieved by use of an organosilane-based surface treatment prior to deposition, as well as tight control of temperature across the substrate during plating. A test vehicle consisting of various resistor structures to evaluate electrical and mechanical properties, processing conditions, and reliability was designed and fabricated. Electrical properties, (including scattering parameters (S-parameters) of the resistor structures up to 20GHz), temperature coefficient of resistivity (TCR), and power handling capabilities of the resistor structures on different substrates are presented.

***Key words*:** Integrated, embedded, resistor, electroless, Ni-P, Ni-W-P, PWB substrate.

I. Introduction

The rapid development of mixed-signal products for a variety of applications is providing multichip modules (MCMs) with many new challenges. Among the many approaches to MCMs, the MCM-L/D approach is attractive as it combines the benefits of thin-film (high density fine line capability) and printed wiring board technologies (low material and process cost) [1]. At present, significant research and development work in the area of integrated passives (esp. resistors, capacitors and inductors) is required for advancement of MCM-L/D towards mixed-signal applications. Volume driver products for the mixed-signal market are wireless communication products operating in the lower GHz range. Surface mounted passives can occupy as much as 60% of the surface area in these products. Thus integration of these passives within the dielectric layer is of critical importance.

Apart from improved packaging efficiencies, other benefits of integration are the potential for improved electrical performance, reliability, and cost, as well as low profile design options. The Georgia Tech Packaging Research Center (PRC) is working towards next generation low-cost packages for high performance digital and mixed-signal applications, and integration of passives in these packages is of utmost importance. Passives provide many functions such as line termination, pull-up, decoupling, RF-choke, impedance matching, etc.

For integrated resistors, two to three material systems are needed to cover the majority of electronic products for various applications (e.g., aerospace, computing, telecommunications, low-cost electronics, etc.); one in the range of 5 - 50 ohm/square, a second in the range of 500 - 1000 ohm/square, and a third possibly in the range of 5K - 20Kohm/square [2, 3]. These materials should also exhibit good stability and a temperature coefficient of resistance (TCR) on the order of ±50 ppm/°C or less. Various techniques have been explored and presented in the literature for resistor integration in MCMs and some of these are outlined in Table I. The materials in Table I are also a good indication of the material requirements needed to satisfy integrated resistor needs for most applications.

Table I. Resistor materials for MCMs and their fabrication methods [3 - 10].

Technology & examples	Resist. Ω/sq.	TCR (ppm/ °C)	Deposition/ comments
Thin Films: TaN, Ni-Cr, Ta_2N, Ta-Si, Cr-Si,cermets	10 - 300	-200 to +200	- Reactive sputtering, RPIB, evaporation. - Low noise current - Temperature stable
Thick Films: Ru_2O, IrO_2 - based	1 - 1M	-150 to +300	- Fired at ~850 °C - High power handling capability. - Highly freq. dependent - High noise current
Filled-polymers	10 - 100K		- Screen printing, stencil printing. - Highly freq. dependent - Low noise current

Excellent thickness uniformity in thin-film deposition of resistor materials can be achieved with vacuum deposition techniques and thus are commonly used. However, the overall-cost associated with vacuum deposition techniques typically tends to be high.

Filled polymers [4], a proven low-cost approach, is an alternate technique that can be used in fabricating resistors in MCM-L based substrates. However, the materials as they exist today are in thick film form, and it can be difficult to precisely control as-deposited resistivity values, largely due to percolation effects and difficulty in dimensional control. Thus, this technique may not satisfy all the requirements necessary for integrated resistors.

Apart from materials challenges, other challenging aspects to successfully achieve resistor integration in MCM-L/D are:

(1) To make resistor lumped, the largest dimension should be less than $\lambda/5$.
(2) For low thermal resistance the area of the film should be as large as possible. This condition and (1) should be optimized in designing integrated resistors. This may prove to be a major challenge for high power resistors in MCM-L/D.
(3) To reduce noise the substrate should be as smooth as possible since resistors exhibit higher noise values on rougher surfaces.
(4) The resistor as deposited should be as close to its desired value as possible to minimize trimming.
(5) Low and reproducible TCR are required to maintain a minimal resistor value fluctuation during usage as well as ease of design.
(6) Good power handling capability.
(7) Material stability and compatibility during processing.

To minimize the discontinuity effects on electrical signals (esp. terminating resistors), the width of the resistive films are required not to differ markedly from the width of the conductive traces which feed them. Signal interconnect line pitch below 25μm is predicted in MCM-L/D (4-chip MCM interconnected by a 4-layer wiring substrate) over the next decade [11]. Such dimensions, and even smaller widths for large resistor values, also will be required for integrated resistors. Further, the challenge is to be able to fabricate resistors on large area substrates with good reproducibility and yield. These challenges are kept in mind in developing a integrated resistor processing technique as discussed below.

II. Approach:

Many resistive materials are metallic in nature and thus can be deposited using low cost processing approaches such as electroless- and electro-plating techniques. Some of the common materials that have been deposited using these techniques for resistors include Ni-P alloy [12 - 14] and Ni-W-P alloy [15 - 17]. These materials when processed under controlled conditions can provide similar properties as outlined in Table I for thin films. The electroless plating technique is preferable to electroplating as simultaneous electrical connection to each resistor structure during deposition is not required. The required equipment for plating is simple and low capital cost as compared to vacuum deposition techniques. However, this technique is not without challenges. Among these are: (1) determining a suitable electroplating bath, (2) optimum plating conditions (e.g. temperature, time, volume/surface area ratio, etc.), (3) uniform plating on large area dielectric substrates, (4) good adhesion, (5) chemical compatibility with the substrate material. Some of these issues are the main focus of this paper. In particular, the use of Ni-P and Ni-W-P alloys is examined.

Electroless plated Ni-P [13, 14, 18]:

The chemistry of electroless plating of Ni-P is well understood and excellent uniform plating can be achieved on large area substrates. The resistivity of Ni increases with increasing phosphorous (P) content in the films. A phosphorous content of 12 - 14% is desirable for resistor applications. Films formed with high phosphorous content have high resistivity, high thermal stability and are non-magnetic. Many recipes for the electroless plating of high phosphorous content films at various pH and bath temperatures have been reported in the literature. One of the problems associated with Ni-P as a resistor material is its high TCR value. The as deposited films are amorphous and conductivity does not change up to a temperature of 400 °C.

Electroless plated Ni-W-P [15 - 18]:

This material is commonly used to achieve low TCR resistors for various applications. It has many superior properties to Ni-P (e.g. better abrasion resistance, good adhesion to most substrate materials, etc.). The TCR of the material can be varied over a wide range depending on the composition of the bath used.

Table II. Properties of electroless Ni-P and Ni-W-P alloys for resistors.

Properties	Ni-P	Ni-W-P
TCR (ppm/°C)	> 100	-5 to +60
Spec. resist. (μΩ-cm), t> 0.1μm	~ 170	~ 150
Max. temp. stability (°C)	~ 300	~ 400

III. Experimental

Electroless plating onto a nonconductive substrate requires the surface to first be sensitized and then activated. Tin chloride ($SnCl_2$) and palladium chloride ($PdCl_2$) dissolved in diluted hydrochloric acid (HCl) are used as sensitizers and activators respectively.

Acid hypophosphite-based baths were used in this work for their low pH (most polymers can withstand low pH baths). The composition of the electroless plating bath used are the same as reported in ref. [18] for Ni-P and ref. [17] for Ni-W-P alloys. Compositions used are highlighted below in Table III for convenience.

Table III. Electroless plating recipe for Ni-P and Ni-W-P.

Materials	Ni-P	Ni-W-P
Nickel sulphate ($NiSO_4$)	57.8 g/l	7 g/l
Sodium hypophosphite	42 g/l	10 g/l
Maleic Acid	35 g/l	---
Sodium Succinate	17.4 g/l	---
Sodium Tungstate	---	10 g/l
Sodium Citrate	---	45* g/l
pH	4.5 - 5.5	
Bath Tempetature (°C)	90	90

* Modified from the recipe presented in ref. [17].

Old baths, esp. Ni-P baths, led to poor adhesion of films to substrates largely due to spontaneous decomposition of the bath during plating and formation of grain-like structures on the substrate, resulting in poor quality of the patterns obtained. Thus, fresh baths were used for each of the samples presented in this paper.

Sheet Resistance (Rs):

A simple method of measuring Rs is to prepare a rectangular sample of film, measure its resistance, and divide by the number of squares of the film material that lie between the end contacts. In order to remove the contact resistance from the measured results in a two-point-probe measurement, multiple line lengths are needed and the contact resistance is determined by extrapolating the resistance value to a zero resistor length. The resistance is calculated from:

$$\text{Resistance} = R = \left(\frac{\rho}{h}\right)\left(\frac{l}{w}\right) = R_S\left(\frac{l}{w}\right) \quad \ldots. (1)$$

where l = resistor length, w = resistor width, h = resistor film thickness , and ρ = film resistivity. Film thickness was measured using a Tencor Instruments Alpha-Step 500 surface profiler.

Temperature Coefficient of Resistivity (TCR):

The TCR of the films was measured from 22 °C - 160 °C in an oven (air ambient) with a decreasing temperature / time profile. Large resistor structures with varying lengths were used and the effects of the contacts was removed from the measured results. The TCR of metallic films over a considerable temperature range from a reference or base temperature (T_o) can be deduced from the following resistance (R) - temperature (T) equation [4]:

$$R = R_o\left[1 + \alpha\left(T - T_o\right)\right] \quad \ldots. (2)$$

where T = temperature of material (°C); T_o = reference temperature (typically 20 °C); α = temperature coefficient of resistivity (TCR) ($°C^{-1}$); and R_O = resistance at temperature T_o.

Power Handling:

The current-voltage (I-V) characteristics of the resistors were measured for resistors of varying lengths, widths and thickness. Voltage across the resistor was applied (with 30s hold time between the voltage steps) until an open in the circuit was measured or the resistivity began to degrade (i.e., significant nonlinearity in the I-V curve was observed). The effect of contact resistance on the measured results was removed and the data was then expressed in terms of power consumed by the resistor structures. The power density consumed by a resistor structure is given by:

$$\text{Power density} = \frac{P}{A} = \frac{V^2}{RLW} \quad \ldots. (3)$$

IV. Thin Film Deposition/Resistor Fabrication:

To achieve fine features and good resistivity tolerance across the substrate, uniform plating of resistor material with minimum defects (blank spots) is critical. The surface of the dielectric material on which the film is deposited plays a critical role in the quality of film plated. As a first study, various substrate materials were used to gain insight into electroless-deposition of Ni-P and Ni-W-P alloys. It was noted that the Ni-P alloy more uniformly covered organic-based substrates (epoxy dielectric) than inorganic substrate (glass), while the opposite behavior was observed for Ni-W-P. No difference in uniform coverage of PWB substrates (organic/inorganic composite) was observed between the two films. However, the plating of either material was not of satisfactory quality to allow fabrication of fine-line structures. An increase in the immersion time of the substrates in the catalyst bath did not significantly improve the plating quality, and was therefore fixed at five minutes. In order to improve the plating quality, various experiments were carried out and are discussed briefly:

Polymer Curing Effect:

Electroless plating of Ni-W-P and Ni-P on partially cured epoxy led to blistering in epoxy layer, with the most severe blistering observed with Ni-W-P films. No blistering was observed with Ni-P films deposited on epoxy layers cured at 145 °C for 30 min. However nonumiform plating resulted, esp. for Ni-W-P, for films cured under these conditions. Similarly, good plating on "as-is" PWB was noted and upon annealing at 150 °C the plating quality reduced significantly (reduction in plated area) for both alloys. Chemical roughening and oxygen-plasma roughening can be carried out on cured films to help improve plating quality. These approaches were not used in this paper due to poor electrical properties associated with resistor structures fabricated on a rough surface.

Surface Treatment:

To further enhance plating quality, the surface of the substrates (glass, PWB and epoxy coated glass) were treated with organosilane (VM651 adhesion promoter, Dupont Electronics). The material used consisted of a mixture of methanol, deionized water and organosilane agent. The substrate was then catalyzed and plating was carried out in both Ni-P and Ni-W-P as described above. Smooth films with no visual discontinuities were achieved for Ni-P on organic substrates and Ni-W-P on inorganic substrates.

Further improvements in uniform seeding were achieved by maintaining a uniform temperature across the substrate. This was ensured by placing the substrate horizontally and face down in the plating bath during film deposition. For vertically-mounted substrates, a Ni-W-P film thickness variation of approximately 35% across the substrate (7.5 cm X 5 cm glass substrate), with an average film thickness of 332 Å was observed; while for horizontally-mounted substrates, a thickness variation of approximately 12% across the substrate with an average film thickness of 240 Å was observed. Further, it was noted that for horizontally-placed samples the film thickness variation across the substrate decreases as a function of increase in film thickness (e.g., 7% variation for a 0.22 μm thick film).

After deposition of the seed layer, two additional processing steps must be performed: the seed layer must be thickened either by use of further electroless deposition or electroplating; and the resultant resistors must be patterned. These steps can be achieved in a variety of ways, namely: (1) lift-off patterning of the thin seed layer if suitably patterned photoresist has been deposited prior to the electroless

deposition, followed by additional electroless deposition on the patterned seed layer traces; (2) thickening the seed layer by additional deposition, either electroless or electrolytic, followed by a subtractive wet etch; and (3) additive processing by means of additional electroless or electrolytic deposition through appropriately patterned photoresist molds, followed by a self-aligned wet-etching-based removal of the seed layer. Some of the problems associated with wet etching of these materials, i.e., processes (2) and (3), are that the etching solutions required may attack the bottom Cu-layer through via holes; in addition, this wet etching solution must be stored, handled, and disposed of. In the lift-off technique, wet etching is not required; in addition, the mechanical stress faced by the substrate during processing is expected to be lower due to the already-patterned nature of the seed layer. Due to these inherent benefits associated with the lift-off technique, this technique was used in further processing of the resistor structures. Two major concerns in using this technique are: (1) the potential for increase in via resistance due to undesired plating of the resistor material in copper vias; and (2) the extended processing time required for carrying out a successful lift-off.

The processing sequence is briefly outlined in Figure 1. Substrate material is spin coated with epoxy, which is dried, exposed, developed and partially cured (30 min. at 145°C for XP-9500, Shipley). Photoresist material is coated and patterned on top of the epoxy layer. The sample is then surface treated with organosilane and followed by immersion in catalyst baths (5 min. each). Rinsing in DI-water is carried out between each step. The substrate is then placed horizontally in a 90 °C Ni-P bath to maintain uniform temperature across the board for 1.5 to 3 min. to form a thin seed layer. After annealing the substrate to improve the adhesion of the seed layer (~100 °C, air ambient), the Ni-P patterns are formed by lift-off in photoresist stripper. The epoxy layer is then completely cured with the thin seed layer structure still present on the surface. Upon curing, the substrate is then immersed in the Ni-W-P plating bath and plated to desired thickness to achieve specific sheet resistivity. This is possible due to the cross-catalytic activity between Ni-P and NiW-P films in electroless deposition. This final deposition is then followed by annealing the resistor pattern at 150 °C for 30min (to improve adhesion) and deposition and patterning of Cu-pads to form the final resistor structure.

V. Properties of Resistor Films:

Preliminary studies were carried out using large electroless thin-film resistor structures deposited on various substrates (glass, epoxy-coated glass and PWB) to varying thickness. A lift-off technique described above was used in patterning the resistor structures and no Cu-pads were used. The dimensions of the resistor structures used are outlined in Table IV. This table also provides a reference to the data presented below.

Table IV. Dimension of structures used in preliminary study.

L / W	w = 500 μm	w = 1000 μm
l = 2500 μm	R11	R21
l = 5000 μm	R12	R22
l = 13000 μm	R13	R23

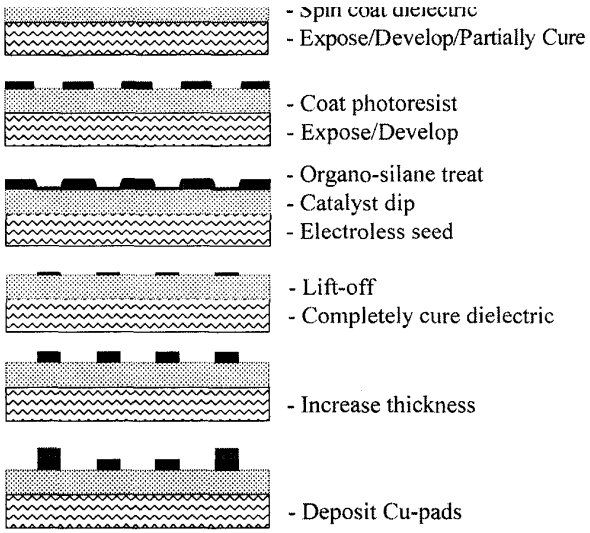

Figure 1. Resistor structure fabrication sequence.

Resistivity as a function of film thickness:

Films with varying thicknesses of Ni-W-P and Ni-P were grown on glass substrates. Table V outlines the measured sheet resistance values as a function of film thickness. The specific resistivity values obtained from this table are consistent with those given in Table II.

Table V. Resistivity of Ni-W-P and Ni-P as a function of film thickness on glass substrates.

Ave. Film Thickness (Å)	Ni-P Ave. Rs (Ω/sq.)	Ni-W-P Ave. Rs (Ω/sq.)
170	168	----
440	----	51
1600	----	9.8
2450	----	5.9

Power handling:

Low TCR values (< ±50 ppm/°C) and high power handling (~ 50 mW) capability is preferable for integrated resistors. The maximum power handling capability of a resistor structure is dependent on the thermal properties of the substrate material, resistor material, resistor size, geometry, etc. For improved integrated resistor reliability, power dissipation in the resistors should be considered, esp. in MCM-L/D approaches.

Figures 2 and 3 shows the power characteristics of resistor structures fabricated on glass and PWB substrates respectively. The resistors on PWB were fabricated with Ni-P seed layer and followed by deposition of a thicker Ni-W-P layer. Only Ni-W-P seed layers were used on glass substrates. As much as a watt of power can be consumed by these resistor structures on a glass substrate, and nearly 500mW for these structures on a PWB substrate without any significant change in the resistivity of the resistor thin-films. Power dissipated in the resistor structures in typical MCM-L/D applications is expected to lie below 50 mW and thus the Ni-P/Ni-W-P material combination satisfies this need. Further, the maximum power dissipation is limited by the PWB

substrate rather than the resistor material itself, as evidenced by the experiments on glass substrates.

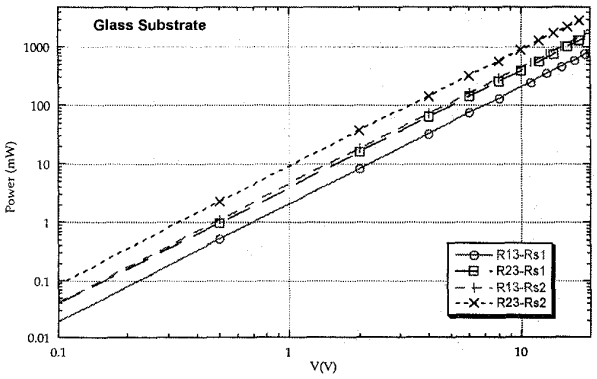

Figure 2. Power handling characteristics of resistors on glass substrates (Rs1 = 10 Ω/sq. and Rs2 = 5.9 Ω/sq.).

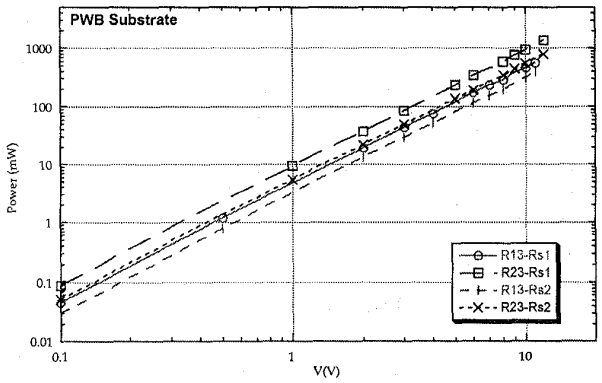

Figure 3. Power handling characteristics of resistors on PWB substrates with variying sheet resistivity (Rs1 = 18 Ω/sq. and Rs2 = 11 Ω/sq.).

Temperature Coefficient of Resistivity (TCR):

For integrated resistors it is critical that the values do not drift significantly upon heating (especially for integrated structures). TCR values ranging from 30 ppm/°C to 110 ppm/°C were measured for Ni-P thin films on glass substrates for average film thickness ranging from 170 Å to 0.15 μm. Low TCR of very thin films are expected [4]. The TCR of Ni-W-P was measured for various thicknesses on glass substrates and was found to lie near zero. The resistance values of a Ni-P/Ni-W-P composite system, Rs = 35 ohms/square, were measured at different temperatures and the percentage change in resistance values (normalized to room temperature (RT) values) are plotted in Figure 4. Low TCR, nearly zero, of the composite system is measured, thus indicating that the TCR of the film is dominated by the Ni-W-P layer.

Temperature Cycling:

It is expected that the integrated resistors will undergo many temperature cycles during processing of subsequent layers deposited above them. In order to evaluate this effect on the resistivity of the material, the resistor structures fabricated on PWB were subjected to thermal cycling from RT to 200 °C (> T_g of the PWB substrate) with a period of 10min. This included 5min. at room temperature followed by 200 °C in air ambient oven for 5min. Two samples with different sheet resistivities were used and the measured results are shown in Figure 5. From this it can be noted that the sheet resistivity of the Ni-P/Ni-W-P on PWB substrates undergo no significant change (i.e., change lies within measurement error), up to a total of 10 cycles. This indicates that the resistor material can withstand the MCM-L/D fabrication temperature cycling (>Tg of dielectric) of subsequent processing.

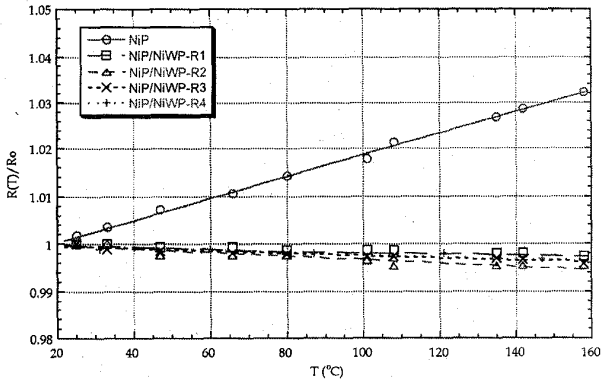

Figure 4. Resistance variation as a function of temperature for Ni-P and Ni-P/Ni-W-P thin film resistor structures (Ni-P: R = 567 Ω at RT; Ni-P/Ni-W-P: R1 = 145 Ω, R2 = 422 Ω, R3 = 350 Ω, R4 = 988 Ω at RT).

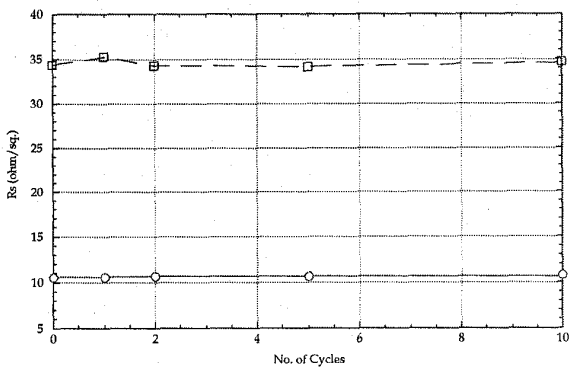

Figure 5. Temperature cycling of resistor structures on PWB substrate for samples with different sheet resistivities.

VI. Test Vehicle:

A test vehicle, Figure 6, consisting of various thin-film structures to evaluate electrical and mechanical properties, processing conditions, and reliability was designed and fabricated. It was built with the minimum number of layers that still allowed all the characterization to be done and at the same time underwent all the relevant processing steps used to fabricate large panel MCM-L/D. Simplified fabrication sequence of this test vehicle is outlined in Figure 1. Only some of the structures on the processed test vehicle were characterized for this paper and are discussed below. Figure 7 shows the interdigited capacitor and a long meander line structure which were used in evaluating the processing

conditions. These structures allow for evaluating the film uniformity, line discontinuities and interline shorts. For the test vehicle of this paper, resistance variation of less than 10% was measured between the multiple Cu-pads on the meander line structure.

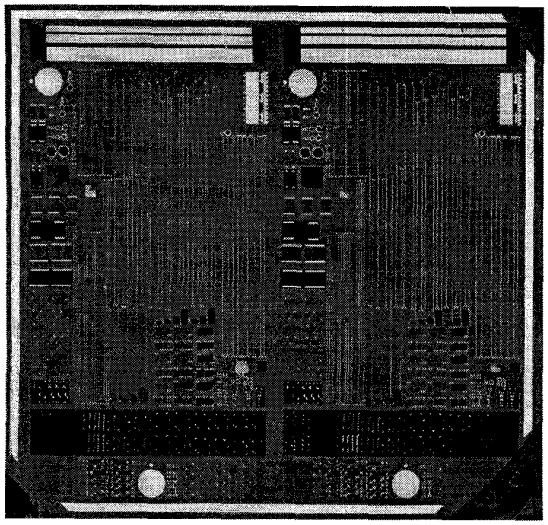

Figure 6. Photomicrograph of a resistor material/structures test vehicle on PWB substrate (approx. 95 cm^2 area).

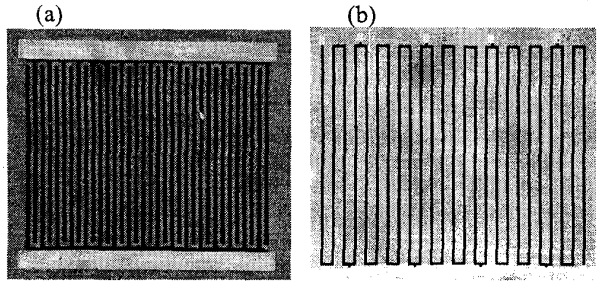

Figure 7. An example photomicrographs of (a) interdigited capacitor structures (line width, w = 50 μm, line spacing, s = 50 μm and line length = 2500μm) and (b) meander line structure (w= 50 μm, s = 200 μm, total length ~13 cm) used in evaluating the processing conditions.

Rectangular samples of resistor films with varying lengths (500 - 2500 μm) and width (25 - 500 μm) as shown in Figure 8 were made to directly measure sheet resistance and contact resistance (between the Cu and the resistor material). Behavior of resistance values as a function of linewidth are plotted in Figure 9 and a linear behavior is achieved, thus indicating good uniformity of the film within the resistor structures. However, the resistance values are higher, esp. for 25 μm wide structures, than the calculated values based on the measured sheet resistance. This was found to be due to the narrowing in the width of the resistor structures and which is believed to be largely affected by the photoresist patterning. This has to be taken into consideration especially when resistors with varying widths are designed in MCMs. For these structures, the contact resistance was found to increase with increasing width due to the varying ratio of the widths of the Cu-pads and the resistor structure. The contact resistance was subtracted from the data presented in Figure 9.

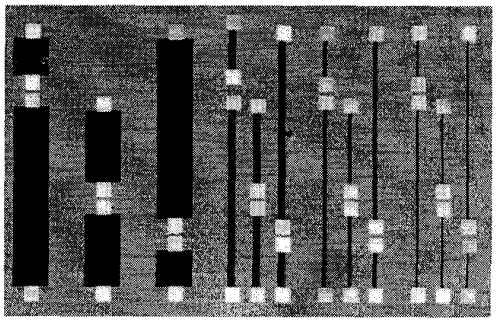

Figure 8. DC resistance test structures with varying widths and lengths (Cu-pad size = 150 μm X 150 μm).

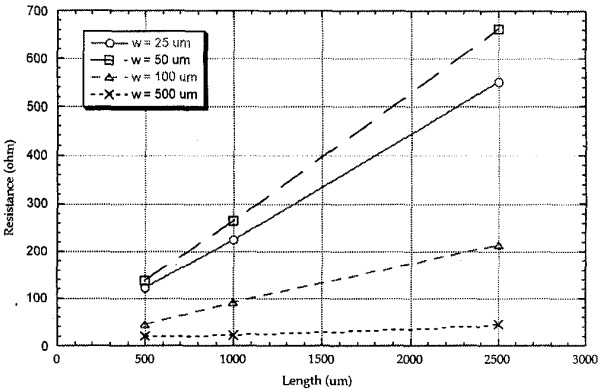

Figure 9. Resistance as a function of width and length. The resistance values of the 25 μm lines are divided by 10.

High Frequency Characterization of Integrated Resistors:

The high frequency measurements were performed with an HP 8510C vector network analyzer and ground-signal-ground (G-S-G) coplanar waveguide probes. Calibration to the probe tip was carried out using a standard LRM calibration kit. To reduce random errors, the process of calibrating the system and measuring the device characteristics was repeated ten times and the measured S-parameters averaged before any data analysis.

In order to evaluate the frequency dependent performance of thin-film resistors made from Ni-P/Ni-W-P, several resistor structures were included on the test vehicle. In this paper, the coplanar G-S-G resistor structures were used for high frequency measurements. Figure 10 shows the photomicrograph of the resistor structures used in measurements. Large Cu-pads on these structures were used to minimize contact resistance. The measured results of structures with a ground plane (floating ground plane) is presented below on a Smith chart, Figure 11. A 50 ohm coplanar resistor structure on the calibration kit was measured and is also shown in the figure for comparison reasons. It can be observed that the capacitive component of the parasitics is dominant in the measured results. Figure 12 shows the real component of the input impedance of the resistor structures for the 50 Ω resistor (resistance is divided by 10) and the

measured coplanar resistor structures (Ni-P/Ni-W-P based) on the test vehicle (R1 and R2 in Figure 10). Increase in resistance is due to the skin-effect. The measured results are as expected for metallic thin-films and thus indicate that Ni-P/Ni-W-P resistors can be used in mixed-signal applications.

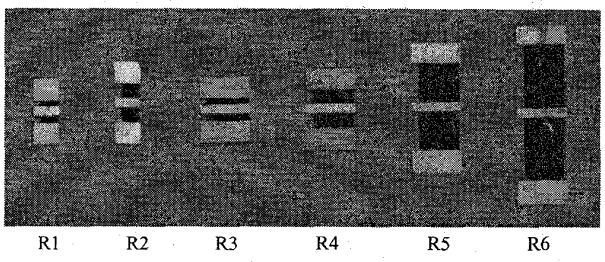

Figure 10. Photomicrograph of resistor structures used in the high frequency measurements. The middle probe pad is 50 μm wide for all structures.

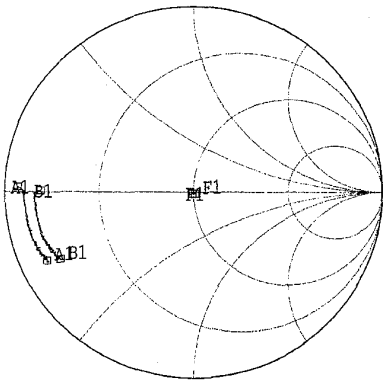

Figure 11. Smith chart (45 MHz - 20 GHz) showing the frequency behavior of a LRM standard 50 Ω and a fabricated resistor on the test vehicle; R1 and R2).

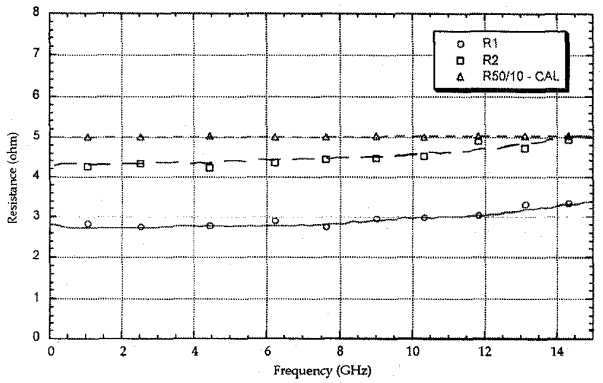

Figure 12. Real component of the input impedance (Z11) of the reference 50 resistor (divided by 10) and two of the measured resistor structures (R1 and R2) on the test vehicle.

VII. Conclusions/Future work:

A novel technique to fabricate high density integrated resistors, MCM-L/D compatible, is demonstrated. Fine line structures (< 50 μm range) can be fabricated using the electroless seeding (Ni-P) and lift-off technique followed by an electroless plating of Ni-W-P to the desired thickness (sheet resistivity). Better seeding was obtained with Ni-P on epoxy dielectric as compared to Ni-W-P. Improvements in the seed layer uniformity were obtained with the surface treatement of the epoxy surface with organo-silane adhesion promoter and maintaining a uniform temperature across the substrate during plating. The resultant films produce absolute TCR < 50 ppm/°C and can provide film resistivity in the range of 5 - 50 ohm/square with good uniformity across the substrate (<10% variation), satisfying the lower resistivity value requirements for mixed-signal applications. This totally electroless technique allows for use of low cost equipment and tailoring of sheet resistivity to be carried out during processing and the need of trimming of resistor structure after processing may be eliminated.

Further improvement in this technique are required from the view of improved plating bath, improvements in surface treatment and tooling set-up for large area processing (12" X 12" substrates). By optimization of the processing techniques introduced in this paper using a process of design of experiments (DOE), 1% tolerance resistors may be feasible on MCM-L substrates.

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