ELECTRICAL ISOLATION OF BULK SILICON MEMS DEVICES VIA THERMOMIGRATION

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ABSTRACT

Electrical isolation of bulk micromachined single crystal silicon MEMS devices is demonstrated using through-wafer junction isolation. Through-wafer npn junctions are fabricated using "temperature gradient zone melting" or "thermomigration" of aluminum in n-type silicon. The npn structures isolate various regions of the single crystal silicon from one another by acting as back-to-back diodes. Thermomigration is a potentially high-throughput process that is consistent with batch fabrication principles, avoids the necessity of a handle wafer, and retains the mechanical integrity of single crystal silicon. By use of this process, electrically isolated sensors and actuators can be fabricated from a single wafer of silicon. Breakdown voltages of multiple thermomigrated npn junctions in excess of 1500V are demonstrated. The utility of this technique is shown by fabricating a comb-drive electrostatic actuator from a single silicon wafer and driving it at 162Vpp.

INTRODUCTION

Bulk micromachined single crystal silicon MEMS devices enjoy a number of advantages including:

- good material properties, such as relative immunity from material fatigue and high Q-factors in resonant structures;
- simple processing, especially with inductively coupled plasma reactive ion etching (ICP-RIE) technologies;
- and potential for large thicknesses of devices, e.g. up to the thickness of the wafer.

The simplest way to fabricate these devices would be to etch them from a single piece of silicon. However, in that case all the components are electrically connected through the bulk silicon, necessitating an isolation scheme.

In the past, there have been three general approaches to fabricating electromechanical devices in bulk silicon. The first is to utilize a 'handle-wafer' approach, either by silicon-on-insulator technology[1,2], or by wafer-bonding[3]. The handle wafer acts to hold the parts of the device in a fixed position relative to one another, while the intervening silicon is completely etched away between the devices. Electrical isolation is thus achieved since the individual parts of the device are no longer physically connected by the original bulk silicon. The second approach is similar, but attempts to eliminate the need for a handle wafer by etching isolation trenches and subsequently backfilling the trenches with another material, e.g. silicon dioxide, to attempt to restore the mechanical integrity of the structure.[4] This second method does not require a handle wafer, since the separated silicon parts are now held together by the backfilled material. However, now the mechanical integrity of the bulk micromachined device depends on both the original silicon and the backfilled material. The third method is to use the bulk etched silicon as a mechanical material, isolate, and subsequently deposit conducting films, as in the SCREAM process.[5,6] To accomplish this, the microdevice is first bulk etched out of the silicon. Then an insulating layer is either grown or deposited on the bulk. Finally, to make the surface electrically active, conductive layers such as metallic films are deposited, including the sidewalls of the microstructure as well as the top surface.

A desirable alternative to these approaches is one in which various parts of the silicon itself are electrically isolated while the original mechanical integrity of the single crystal silicon material is maintained. Our approach is to take advantage of the semiconducting properties of silicon to form diodic isolation. This approach, widely used by microelectronics designers, is termed "junction isolation."[7,8] This method creates npn or pnp regions between devices, thereby in effect creating two back to back diodes that disallow current flow from one region to another.

Up to now, however, junction isolation has not been widely employed as an electrical isolation scheme for thick, bulk silicon MEMS devices. This is primarily because it is necessary to dope the silicon all the way through the thickness of the wafer (typically, on the order of hundreds of microns) to achieve isolation in these devices. Typical methods for doping silicon such as standard diffusion or ion implantation are not practical for extending a doped region all the way through the thickness of a typical wafer. However, methods such as directional diffusion, or temperature gradient-zone melting, can be used to achieve doping through the thickness of the wafer and is therefore suitable for isolation of bulk micromachined silicon devices.

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TEMPERATURE GRADIENT ZONE MELTING

Through-wafer doping of silicon has been demonstrated in a process known as thermomigration, or "Temperature Gradient Zone Melting (TGZM)."[9,10,11] The temperature gradient zone melting process was first applied to semiconductor processing in 1955 by Pfann[8]. Anthony and Cline[12,13] did much in the years 1973-1981 to clarify understanding of this process for various solvent/solute systems. This technology has also been applied to micromachining: e.g., in the early 1990's, the use of aluminum thermomigration in the fabrication of micromachined photosensing arrays and intracortical electrode arrays was demonstrated.[11,14,15]

TGZM is typically performed by first depositing and photolithographically patterning a dopant, e.g., aluminum, on one side of a silicon wafer. The other side of the wafer is then radiatively heated to a high temperature, e.g. on the order of 1200 °C. As a result of the one-sided heating, a temperature gradient is established through the thickness of the wafer. When heated, the aluminum melts, and dissolves some of the silicon at the surface. The resulting droplet follows the thermal gradient towards the hot surface. As the droplet moves from the colder to the hotter surface, the colder side of the droplet resolidifies epitaxially; the resolidified material has an aluminum concentration given by the solid solubility limit for aluminum in silicon at the solidification temperature. Typically, this concentration is on the order of 10^{19} cm^{-3}. The process is highly anisotropic, and relatively fast, with droplets traveling through a 300μm thick wafer in 8 minutes.

When appropriate patterns of aluminum are thermomigrated through an n-type silicon wafer (Figure 1), npn regions are created through which current (except for diode leakage current) is unable to pass, until the breakdown voltage of the reverse-biased diodes is reached. The npn regions allow a voltage drop across the junction isolation (e.g., between regions 1 and 2 of Figure 1d) to be sustained without compromising the mechanical integrity of the wafer, thereby enabling actuation of and/or sensing by bulk micromachined silicon structures. Appropriate stacking of multiple npn regions can also be used to increase the total breakdown voltage of the isolation regions.

FABRICATION OF TEST STRUCTURES

Referring to Figure 1, an n-type <100> single crystal 2" silicon wafer with a resistivity of 10-30Ω-cm is cleaned with a solution of H_2SO_4 and H_2O_2 at 120 °C for 10 minutes, rinsed, dipped in HF for 1 minute, and then rinsed again. The wafer is then metallized with aluminum, e.g., by placing it into an electron beam evaporation chamber where 5μm of aluminum are evaporated at a rate of 10 angstroms/second. The aluminum is then patterned photolithographically and

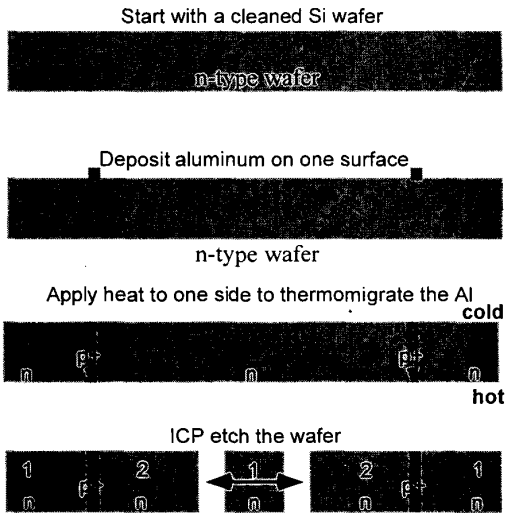


Figure 1: *Fabrication sequence for thermomigrated aluminum through-wafer npn junctions (a) cleaned silicon wafer; (b) after deposition and patterning of aluminum; (c) after thermomigration; (d) after ICP etching to release the micromachined structure.*

etched in a solution of phosphoric, acetic, and nitric acids (PAN etch).

To perform the aluminum thermomigration, the wafers are placed in a vacuum chamber which is fitted with a resistively-heated tungsten filament. The silicon wafer is placed as close to the filament as possible with the aluminum side facing away from the filament. The chamber is closed and a vacuum established on the order of 10^{-6} torr. The filament is heated to approximately 1500 °C, and radiatively heats the wafer to approximately 1200 °C from one side. As a result, a thermal gradient is established and the aluminum thermomigrates through the wafer within 8 minutes. The filament is switched off, and the chamber allowed to cool for 10 minutes. The chamber is vented and allowed to cool another 10 minutes prior to removal of the sample.

The surface of the sample is then lapped on both sides to remove heat-damaged silicon and any excess aluminum. The sample is then optionally stained with 99% HF and 1% HNO_3, which darkens the aluminum-doped areas, and allows alignment to the thermomigrated-aluminum-doped silicon regions.

To form npn test structures, the thermomigrated wafer is either cleaved or ICP-etched into easily-handled chips. To use ICP etching, a photoresist mask is patterned onto the wafer, placed into a Plasma-Therm ICP-RIE chamber, and etched using the SF_6 Bosch process.[16] Both the n-silicon and the Al-doped silicon

are etched using the standard Bosch process, however, the Al-doped silicon etches at about half the rate of the lightly doped n-type silicon. The etch-rate mismatch was reduced by taking advantage of RIE lag. The etched areas around the Al-doped silicon were made larger to increase its etch rate. After the ICP etch, the remaining photoresist is removed with acetone and the wafer is cleaned with a solution of H_2SO_4 and H_2O_2. Figure 2 shows a photomicrograph of fabricated test structures.

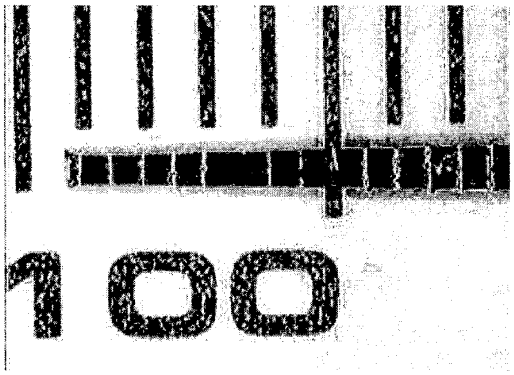


Figure 2: *Multiple npn junction test structure is shown on top of a ruler. Each mark on the ruler is separated by 1mm. The test structure is 8mm long. Each aluminum bar on the test structure is 100 μm wide and extends the length of the bar, resulting in individual npn regions.*

ISOLATION CHARACTERIZATION

Because junction isolation uses two back-to-back pn junctions, there is a finite voltage that the junction can sustain before breakdown occurs (the 'breakdown voltage'). Furthermore, because of generated charge carriers in the junction, there is a small leakage current that can flow from one side of the npn junction to the other. Both of these effects are limits on the ultimate isolation and must be quantified.

To measure these characteristics, a sample was built using the fabrication process described above. The sample had multiple numbers of thermomigrated aluminum npn junctions (Figure 2) so that the breakdown voltage and leakage currents for multiple npn junctions could be measured. The aluminum-doped silicon regions are 100μm wide and separated by 500μm of n-type silicon. Stainless steel probes were contacted to the n-type regions of the silicon. Current-voltage characteristics (from a Tektronix 370A curve tracer) were obtained as a function of the number of npn junctions between the probes; the number of junctions ranged from zero to 12.

The I-V curve for a single npn junction is shown in Figure 3. The curve exhibits a breakdown voltage occurring at –110V and +170V. At voltages less than the breakdown, the leakage current is less than 10μA.

Multiple npn junctions were tested to see if breakdown voltages increased for npn junctions arranged in series. Figure 4 shows that the breakdown voltage increases roughly linearly with the number of npn junctions. Each npn junction contributes an average of 138V breakdown voltage to the total, with a total breakdown voltage of -1550V and +1450V for 12 npn junctions. Figure 5 shows the I-V curve for 12 npn junctions. At voltages less than breakdown, the leakage current remained less than 10μA.

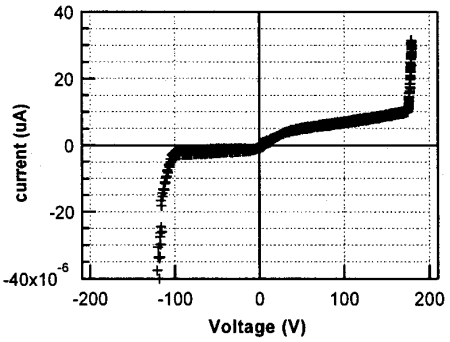


Figure 3: *I-V curve for a single thermomigrated npn junction. The breakdown voltage is at –110V and +170V for reverse and forward biases, respectively.*

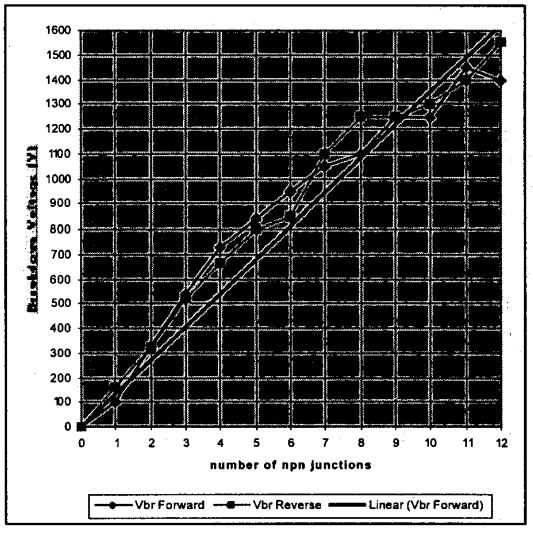


Figure 4: *Breakdown voltage as a function of the number of npn junctions.*

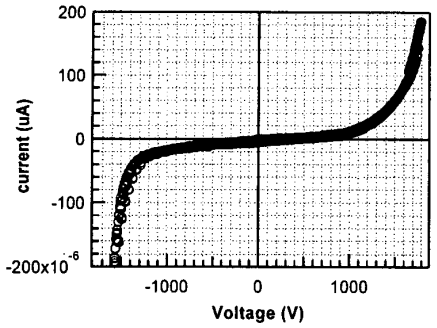


Figure 5: *I-V curve for 12 thermomigrated npn junctions. For 12 npn junctions, the breakdown voltages sum, with a resultant overall breakdown voltage of –1550V and +1450 V.*

ACTUATOR DEMONSTRATION

A demonstration actuator was fabricated using the above fabrication procedure to illustrate the application of this technique to bulk micromachined, electrically-isolated actuators fabricated from a single silicon wafer. In the fabrication of the actuator, the final ICP etch was used to form the spring and comb drive electrodes of a simple electrostatic actuator. A photomicrograph of the front and back of the device is shown in Figures 6 and 7. The thermomigrated aluminum line can be seen on both the front and back surfaces, illustrating that the aluminum doped silicon extends through the wafer (since on these wafers the lapping step after the thermomigration was omitted). The width of the aluminum-doped silicon region is 100μm. The length of the device is 2 mm overall and the fingers of the comb drive are 40 μm in width.

The demonstration actuator was placed on a probe station, with a probe contacting the stator and another probe contacting the rotor. The probes were driven by a Trek 50/750 high voltage amplifier at 300:1 voltage amplification. The amplifier, in turn, was driven byan HP 33120A function generator with a sinusoidal signal output. A Tektronix 2221 oscilloscope was connected in parallel to the probes to monitor the voltage across the demonstration device. The actuator was driven with an AC signal just under breakdown at 162 Vpp and 60 Hz with an 84 V DC offset. At this voltage, the actuator displaced by approximately 10 microns.

A close up of one of the fingers of the interdigitated electrostatic actuator is shown in Figure 8. In Figure 8a, the finger is shown with no voltage applied. In Figure 8b, the finger is shown moving at 60Hz (note the blurriness of the finger), demonstrating successful actuator operation.

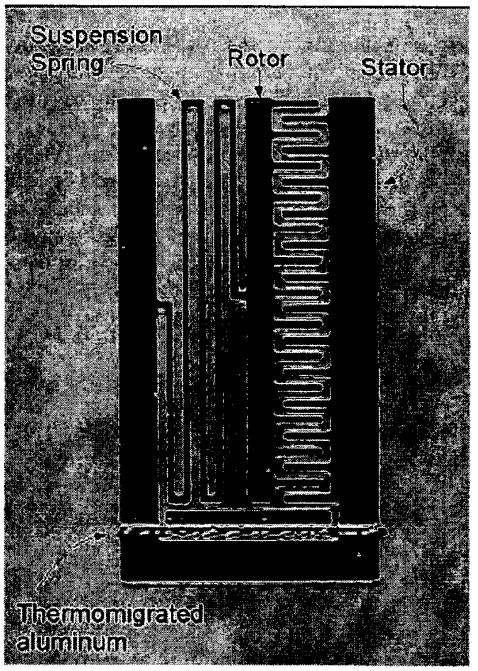


Figure 6: *Front side of demonstration actuator. The chip size is 1 mm wide by 2 mm tall.*

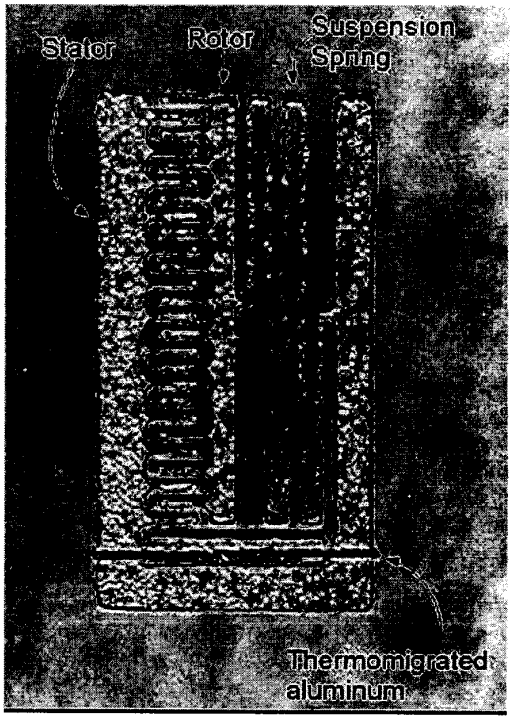
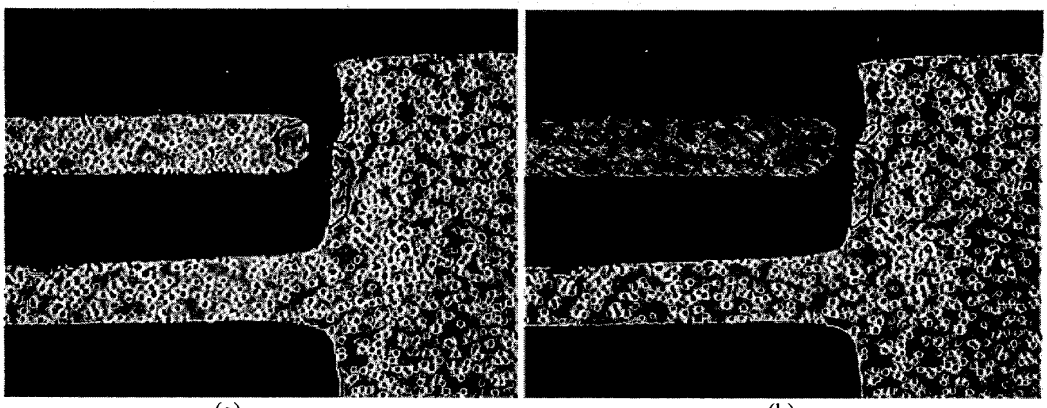


Figure 7: *Back side of demonstration actuator.*



(a) (b)

Figure 8: *Photomicrographs of the junction isolated demonstration actuator with and without an excitation voltage. In (a), no excitation is applied. In (b), the excitation voltage is 162Vpp with a 84V offset at 60Hz. The finger displacement is approximately 10μm, resulting in a blurring of the rotor comb shown in (b).*

CONCLUSION

The application of temperature gradient zone melting to the fabrication of a bulk micromachined single crystal silicon actuator was demonstrated. The breakdown voltage and leakage current of the thermomigrated junction isolation were characterized. Breakdown voltage multiplication could be achieved by stacking multiple npn junctions in series. The technique was demonstrated on a simple ICP-etched electrostatic comb drive actuator. Successful electrostatic actuation was achieved in the demonstration device.

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