ALIGNABLE DEPOSITION OF THIN FILM SEMICONDUCTOR MA TERIALS FOR INTEGRATED MICRO-OPTO-ELECTRONIC SYSTEMS

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ABSTRACT

The selective and alignable deposition of patterned thin film epitaxial GaAs/GaAlAs and InP/InGaAsP devices onto host substrates such as silicon for low cost hybrid integrated micro-opto-electronic systems is reported. Using a combination of semiconductor etch layers and selective etches, the epilayers can be separated from the growth substrate. We use a thin polyimide diaphragm as the transparent transfer medium for these epitaxial materials and devices. Each of these thin film devices or a group of these devices on the polyimide is optically aligned and selectively deposited onto the host substrate. Using this technique, GaAs and InP-based light emitting diodes and optical detectors which are microns thick were grown on lattice matched GaAs and InP substrates, lifted off, aligned and selectively deposited onto a silicon host substrate. The devices were then electrically contacted and tested using standard microelectronic fabrication and testing techniques. This method also enables the manufacturable, sparse distribution of costly photonic devices or the deposition of aligned arrays of devices to fabricate larger arrays. The integration of these light weight devices with micro sensors and micro actuators will foster micro-opto-electro-mechanical integration.

INTRODUCTION

The integration of high quality, single crystal thin film gallium arsenide (GaAs) and indium phosphide (InP) based photonic and electronic materials and devices with host substrates and structures comprised of material such as silicon (Si), glass, and polymers will enable the fabrication of the next generation of micro-opto-electro-mechanical systems and optoelectronic integrated circuits. Thin film semiconductor devices deposited onto arbitrary host substrates and structures create near-monolithic integrated systems which can be interconnected electrically using standard inexpensive microfabrication techniques such as vacuum metallization and photolithography. In particular, the low weight of these thin film devices makes them attractive for integration with micromechanical devices which may have difficulty supporting and translating the full weight of a standard device. In this paper, we discuss methods for the alignment, selective deposition, and interconnection of thin film epitaxial GaAs and InP based devices onto host substrates and host microstructures.

In integrated systems, it is often advantageous to utilize a variety of materials, each suited to a particular purpose. Compound semiconductors are useful optoelectronic devices, and silicon and polymers have been widely investigated for microstructure and microelectronic systems. High quality compound semiconductor devices, particularly those suited for optoelectronic applications, are generally grown lattice matched or near lattice matched. For the integration of GaAs on Si, heteroepitaxial growth has been intensively investigated [I). However, the crystal quality of this material is often insufficient for many optical applications. To integrate compound semiconductor devices with host materials which have no periodicity, however, the compound semiconductor cannot be grown directly

upon such a host. In many cases, the substrate which is used as a nucleation seed for lattice matched growth is not essential to the performance of the epitaxial device. In fact, some device structures can be significantly improved upon if the growth substrate is removed from the lattice matched epitaxial device layers. Thin epitaxial films are light weight and the device designer has access to both sides of the epilayer, uninhibited by the substrate.

One of the first reports of this type of epitaxial device layer separation is the epitaxial liftoff (ELO) process as described by Bellcore [2]. A thin aluminum arsenide (AlAs) sacrificial layer is grown lattice matched onto a GaAs substrate, and GaAs device epilayers of interest are grown on top of this AlAs layer. The GaAs lattice matched epilayers are separated from the growth substrate by selectively etching the AlAs sacrificial layer. These device layers are then mounted in a hybrid fashion onto a variety of substrates and are subsequently etched after deposition to defme individual devices. This ELO material is very high quality [2] and is currently being used for the integration of GaAs materials onto host substrates such as Si, glass, lithium niobate, and polymers [2-5}.

Although the Bellcore technique yields high quality material, it has several problems, including the inability to align and selectively deposit tIle thin film devices and difficulties in contactirlg both sides of the patterned device. In this paper, we report two modified ELO techniques which enable the alignment and selective deposition of a device or array of devices onto a host structure, and also allow tIle devices to be processed on both the top and bottom of the epitaxial sample while under support. This alignment and selective deposition place the relatively expensive compound semiconductor GaAs and InP based devices only where needed, thereby producing an inexpensive integrated system. The thin film epitaxial devices and the host structures can be independently optimized and tested, leading to high performance and high yield. This technique also enables tIle fonnation of large scale, repairable arrays of devices as well as the integration of thin film compound semiconductor devices with microstructures.

INTEGRATION PROCESS TECHNOLOGY

In the first Georgia Tech ELO technique, the GaAs and In P based device layers (Figure la) are defined on the growth substrate using mesa etch processing (Figure Ib). Processing steps such as contact definition can also occur on these mesa defined devices either before or after the mesa etch (Figure lc). These devices are then coated with Apiezon W (Figure ld) and, for the GaAs based devices, are exposed to a standard HF:H20 (1:10) etch solution to separate the epitaxial devices from the growth substrate (Figure Ie). The array of mesa defined epitaxial devices is embedded in the surface of the Apiezon W carrier, which is approximately 100 J.U11 thick and can be easily handled. At this point it is not possible to align these ELO devices with respect to features on a host substrate since the Apiezon W is opaque.

To overcome this difficulty, the ELO devices are contact bonded to a transparent polyimide diaphragm which serves as an alignment and selective deposition transport for the ELO devices (Figure If). The polyimide diaphragm is fabricated using standard rnicromachining techniques. This diaphragm is transparent, taut, and mechanically tough, and is thus ideal as a carrier for the liftoff layers. The ELO devices on the Apieon W carrier are then brought into contact with the polyimide, and through contact bonding, the ELO devices are attached to the polyimide (Figure If). The Apiezon W is dissolved with trichloroethylene, leaving the ELO devices bonded to the top of the polyimide. Note that the pre-liftoff processing (for example, contacts) applied to these devices now lies on the top of the ELO devices supported by the polyimide diaphragm. The devices can now be aligned through the transparent diaphragm and selectively deposited to the host structure as shown in Figure 19.

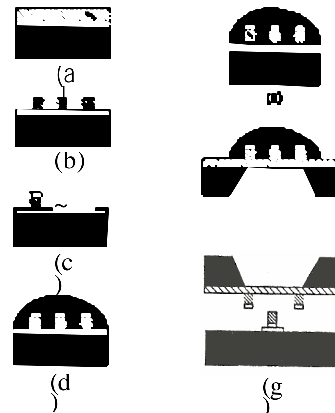

Figure 1. Georgia Tech epitaxial lift off process. (a) Starting substrate with grown layers; (b) after mesa etching; (c) after contacting; (d) after Apiezon W application; (e) after selective etch; (f) after adhesion to silicon supported polyimide diaphragm and removal of Apiezon W; (g) after selective deposition onto host substrate. Individual devices or the entire array can be aligned and deposited onto host substrates.

The second Georgia Tech ELO process utilizes a spun on film of transparent pol~de (DuPont PI-26 I I) as the handling layer instead of the opaque Apiezon W. The epitaxial devices are mesa etched, the polymide is spun on, a support ring is placed upon the polymide before curing, and the polyirnide is cured to form the protective handling layer. This assembly is then placed in the HF etch solution to release the epitaxial device. The devices can now be aligned and selectively deposited onto the host Structure.

An etch as highly selective etch as that which enables the ELO process in GaAs-based compounds has not yet been identified for InP based compounds. We have demonstrated the formation of thin film epitaxial devices in InP based compounds, namely, In P, InGaAs and In GaAsP, using a slightly different etch technique. This technique uses a single or a pair of selective etches and etch stop layers to dissolve the substrate, leaving behind the epitaxial layers of interest. An In GaAsP (bandgap of 0.95 eV) etch stop layer is grown lattice matched between the epilayers of interest and the InP substrate. The epitaxial devices are mesa etched, the handling layer is applied, and the assembly is placed into the HCl etch solution, which selectively etches the InP. The stop etch InGaAsP is subsequently removed with H2S04:H202:H20 {l:l:l) if this layer is not part of the functional epitaxial device. The alignment and deposition of these In P based devices then proceeds identically to the Ga As based devices.

RESULTS

Figure 2 is a photomicrographs of InP/InGaAsP/InP pin detectors mounted on a polyimide transfer diaphragm in a top view with illumination through the transparent diaphragm. This transparent diaphragm enables the user to align the ELO devices with respect to the host substrate prior to deposition. Current alignment and deposition capability

is to within 1 µm. After deposition, the uncontacted side of the ELO devices faces up, and

conventional photolithographic and processing techniques can be used to apply contacts to this side of the devices. This process sequence is in1portant, as we have noted some difficulty with processing steps such as contact deposition if these thin ELO samples are not supported by a substrate during deposition.

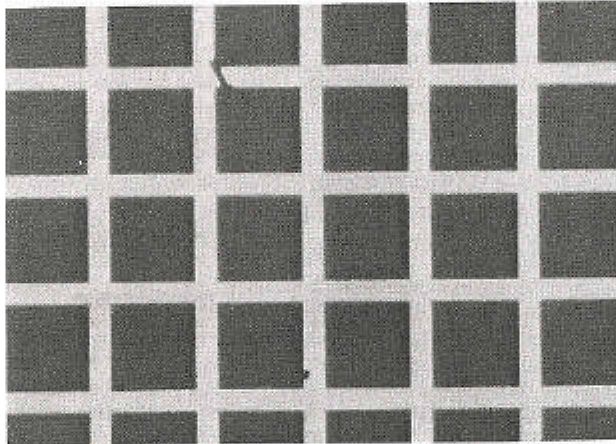

Fig 2: Photograph of an array of 250 urn x 250 urn x 4 urn thick InP/InGaAsP/InP double hetero-structure lifted-off devices on a 6 urn thick mylar diaphragm with bottom illumina- tion (through the transparent diaphragm).

since the ELO devices are on the order of microns thick, the surface profile of the devices on the host substrate is nearly monolithic, and conventional processing techniques can be used to electrically connect the devices to the host substrate. Figure 3 shows a photomicrograph of a GaAs/GaAlAs light emitting diode (LED) structure on Si which has been integrated using the Georgia Tech ELO technique. This device is emitting infrared light under forward bias, illustrating the successful liftoff, transfer, and electrical contacting of both sides of this device.

Figure 3. An epi- taxialliftoff LED, emitting radiation, which has been selec- tively deposited from the polyi- mide diaphragm onto a Si host substrate.

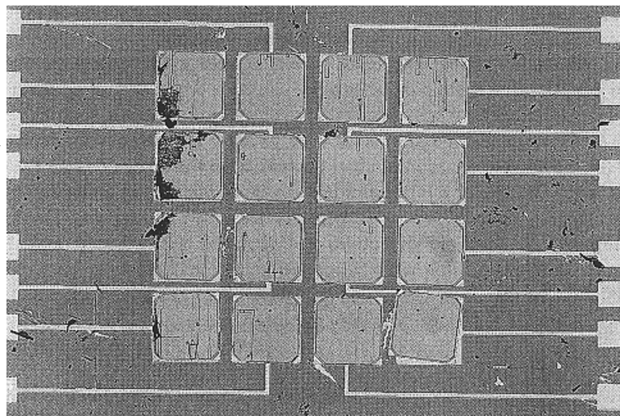

Figure 4. Four by four array of InP/InGaAsP/InP pin detectors on Si.

The alignment and deposition of single thin film devices or arrays of devices can be performed using the Georgia Tech ELO process. To form large (wafer scale) arrays of devices, sub arrays of devices can be aligned and deposited to form larger arrays. This eliminates the need for wafer-scale growth uniformity of devices for wafer-scale integration. Figure 4 shows a 4 X 4 array of InP/InGaAsP/InP pin detectors which have been deposited onto gold pads which lie on Si.

For high yield in integrated systems, the ability to repair devices is of paramount importance. The lower right hand element shown in the array in Figure 4 was slightly offset due to a particule which was included during deposition. This defective device was removed, as shown in Figure 5a, and a new device was aligned and selectively deposited onto that bare pad, as shown in Figure 5b. Thus the demonstrated integration technology allows the replacement of defective devices for high yield.

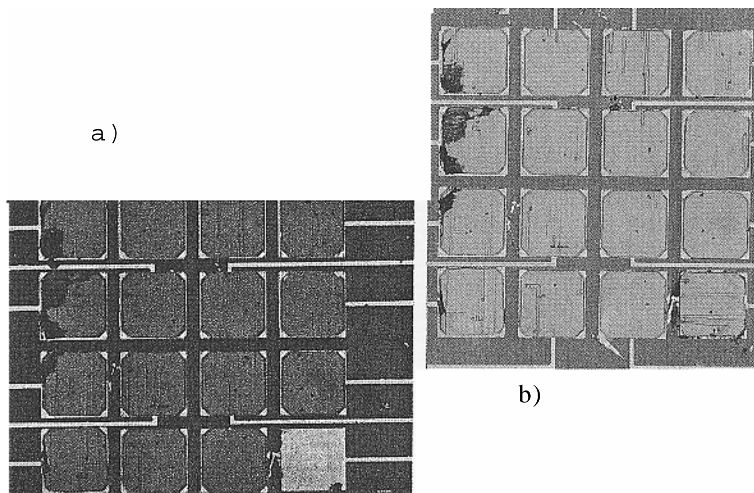

Figure 5. (a) Defective device removed from array of Figure 4; (b) Replacement device aligned and deposited to repair array of Figure 4.

CONCLUSION

Epitaxial lift off processes which utilizes a transparent polyimide diaphragm have been developed to realize the alignable, selective deposition of epitaxial GaAs and InP based thin film material onto host structures comprised of materials such as Si, glass, and polymers. This transparent diaphragm can be used to align and selectively deposit the thin film GaAs and InP based devices as individual devices from the array or as an entire array onto the host substrate. The use of the polyimide transfer diaphragm also allows both the bottom and the top of the device to be processed while under substrate support. These thin film devices can be removed if they are defective, and replaced with aligned and deposited replacement devices. The integration tools described herein will prove to be particularly useful for the integration of thin film GaAs and InP based devices, which, due to their light weight, are ideal candidates for integration with microstructures.

ACKNOWLEDGEMENTS

The authors wish to acknowledge valuable technical discussions with Professor M. Brooke, S. Fike, B. Rashidian and C. Ahn of Georgia Tech. Financial support was provided by the Newport Corporation, Digital Equipment Corporation, and the National Science Foundation. Microfabrication was carried out in the Microelectronics Research Center of Georgia Tech with fabrication assistance from the staff.

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