A Reduced Intermodulation Distortion Tunable Ferroelectric Capacitor—Architecture and Demonstration

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***Abstract*—A ferroelectric tunable capacitor device architecture is presented that allows for a reduction of intermodulation distortion (IMD), while maintaining high tunability at low bias voltages. The tunable capacitor is fabricated from epitaxial thin-film barium–strontium–titanate deposited on a sapphire substrate. The RF portion of the capacitor is a conventional planar gap capacitor with a 12–14-μm gap. However, rather than superimposing the dc bias on the RF pads, a separate bias structure is fabricated within the RF gap. The interdigital bias structure has narrowly spaced high resistance (2–3 $\times$ 10^4 $\Omega/$sq) oxide conductor electrodes, such as indium–tin–oxide electrodes or lanthanum–strontium–cobalt–oxide electrodes spaced 1–2 μm apart. The high resistivity of the bias electrodes decouples the dc bias from the RF signal path. This bias structure allows high dc fields to be developed with less than 30 V applied to tune the material permittivity (1 : 1.4), but is sufficiently resistive to avoid affecting the Q factor of the RF capacitor. Since the RF gap is wide, the IMD performance remains good, even at modest tuning voltages. The following three classes of gap capacitor have been fabricated for concept verification: 1) a conventional gap structure (without additional bias structure); 2) the proposed RF gap capacitor with the dc-bias structure; and 3) a narrower conventional RF gap-capacitor structure used as an IMD reference. The proposed RF gap capacitor with dc-bias structure has been fabricated in two versions: one in which the highly resistive bias electrodes are electrically connected to the RF electrodes (the attached-bias-electrode (ABE) scheme) and one in which the highly resistive electrodes are provided with a separate port for further control (the isolated-bias-electrode (IBE) scheme). In addition, parallel and perpendicular orientation of the bias electrodes relative to the RF field is investigated. The frequency response of the proposed gap capacitor with the dc-bias structure is characterized and its analysis shows that the highly resistive bias lines are serving as a dc-bias path for high tunability, but are not attenuating the RF signal. While the IBE structure has more degrees of freedom for biasing as compared to the ABE structure, the overall tunability at 30 V and IMD performance of both the ABE and IBE structures are similar. Two-tone IMD tests show that the IMD performance for the gap capacitor with the bias structure is improved by 6 dB over the conventional reference structure at the same tunability.**

***Index Terms*—Barium strontium titanate (BST), ferroelectric tunable capacitor, input third-order intermodulation intercept point (IIP3), Q factor, reduced intermodulation distortion (IMD).**

I. Introduction

BARIUM–STRONTIUM–TITANATE, $Ba_{1-x}Sr_xTiO_3$ (BST), is a very attractive RF tunable material due to its large field-dependent permittivity, high dielectric constant, and relatively low loss tangent. In addition, varactors created from this material have no junction noise and have no preferred polarity compared to semiconductor varactor diodes [1], [2]. By using these advantageous properties of BST, a number of advanced high-frequency tunable capacitors have been successfully demonstrated and integrated into RF components, such as phase shifters and RF filters [3]–[6].

One of the fundamental issues affecting tunable capacitors is *intermodulation distortion* (IMD). Since the value of a tunable capacitor depends on the magnitude of the voltage applied across it, RF signal levels that are on the order of the tuning voltage modulate the device capacitance and, therefore, can be distorted. In a conventional capacitor, the IMD is directly proportional to the tunability of the capacitor, as expressed in (1) [7] as follows:

$$\mathrm{IMD} \propto \frac{V_{\mathrm{RF}}}{V_{\mathrm{DC}}} \tag{1}$$

where V_{RF} is the amplitude of the RF signal voltage and V_{DC} is the voltage required for tuning. Based on this relationship, one approach to improve IMD performance in high RF power-handling devices is to make the dc tuning voltage much higher than that of any RF voltage level to obtain the desired tunability. While this approach is effective, tuning voltages required to achieve acceptably low levels of IMD often exceed 100 V. However, this approach to reduced IMD is severely limited by the desire to keep tuning voltages relatively low. Although no significant current is drawn to bias the capacitor, a system problem results in supplying the high static potentials required for this approach.

This paper describes a device architecture that addresses the IMD issue by means of a capacitor that has an additional highly resistive dc-bias structure constructed within the capacitor gap. This additional structure allows decoupling of the RF signal and dc tuning voltage levels, thereby enabling low IMD structures at low tuning voltages. Two structural implementations for this

Manuscript received April 17, 2003. This work was supported in part by the U.S. Air Force Small Business Innovative Research under Contract F33615-01-M-1950 and by MicroCoating Technologies Inc. under a subcontract.

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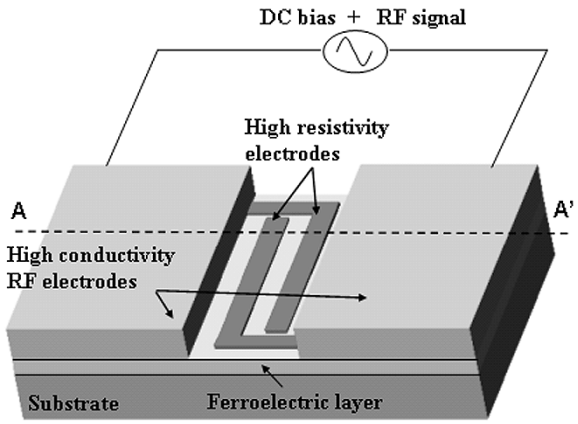
Digital Object Identifier 10.1109/TMTT.2003.820168



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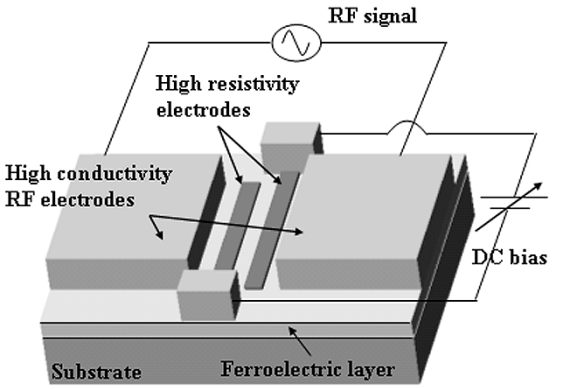

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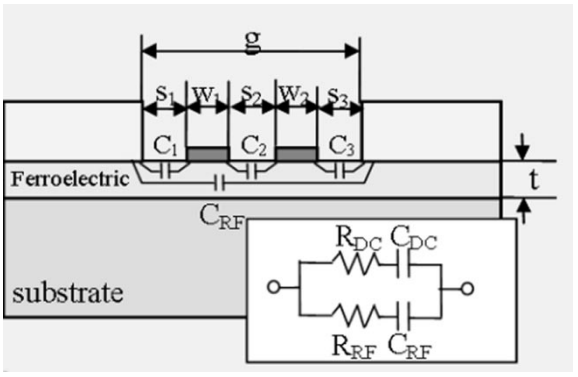
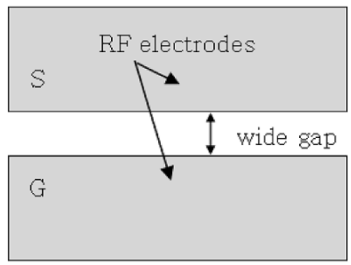


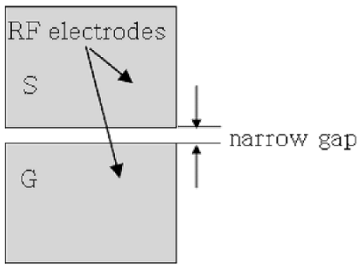
(c)

Fig. 1. Two architectures of a reduced IMD ferroelectric gap capacitor. (a) ABE pattern. (b) IBE pattern. (c) Cross-sectional view A–A' (an equivalent circuit is shown in the inset).

approach are shown in Fig. 1(a) and (b), respectively: a gap capacitor with attached-bias-electrodes (ABEs), having dc-bias electrodes connected to the RF pads; and a gap capacitor with isolated-bias-electrodes (IBEs) for dc bias, which can be energized independently of the RF electrodes. Fig. 1(c) shows the cross-sectional view of A–A' of the ABE pattern. The RF capacitor is a conventional microwave gap capacitor that uses thick and high conductivity electrodes to ensure high quality factor (Q factor). In contrast, the dc-bias structure is fabricated with high-resistivity interdigital structures. At low frequencies, such as those used to change the tuning bias voltage, the high-resistivity lines present a negligible impedance compared with that of the gap capacitor and the full tuning voltage appears across the lines, changing the permittivity of the structure and, therefore, the capacitance. However, at signal frequencies (i.e., RF frequencies), the impedance of the bias lines exceeds that of the gap capacitor itself so the RF current travels through the (permittivity-tuned) ferroelectric material. Since the RF field is effectively isolated by the high resistance of the bias structure, no degradation in IMD performance occurs. Furthermore, if the resistivity is kept high enough, no noticeable degradation in capacitor Q will occur since the RF field will preferentially interact with the low-loss low-impedance BST capacitor.



(a)



(b)

Fig. 2. Conventional gap capacitors (top view). (a) Wide gap capacitor (type I). (b) Narrow gap capacitor (type II).

II. Design Architecture

Fig. 2 shows two conventional gap capacitors, one with a wide gap and the other with a narrow gap. While the narrow gap capacitor requires less area and lower dc-bias voltage for required capacitance and tunability compared with the wide gap geometry, it will have degraded IMD performance, as seen from (1). For applications such as phase shifters and tunable filters, the IMD performance must be maintained. Hence, wide gap capacitors are mainly used at the cost of both device real estate and high required tuning voltage.

In contrast to the conventional gap capacitor, consider a gap capacitor with highly resistive bias electrodes in the RF gap. Fig. 3 shows three dc electrode design schemes for this type of capacitor. Fig. 3(a) shows a gap capacitor with short bias electrodes placed inside the RF gap parallel to the RF field and attached to the RF electrodes (the so-called "short ABE structure"). Note that the dc electric field generated between the short bias electrodes is perpendicular to that of the RF field. Fig. 3(b) shows a gap capacitor with long bias electrodes placed inside the RF gap perpendicular to the RF field and attached to the RF electrodes (the so-called "long ABE structure"). Note that the dc electric field generated between the long bias electrodes is par-

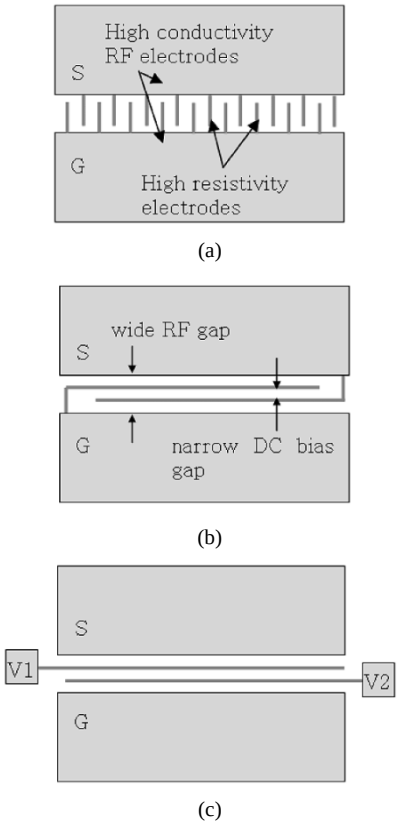


Fig. 3. Gap capacitors with high-resistivity bias electrodes inside the gap (top view). (a) Short ABE capacitor (type III). (b) Long ABE capacitor (type IV). (c) Long IBE capacitor (type V).

TABLE I
SUMMARY OF GAP CAPACITOR ARCHITECTURES

		Abbreviation	Features
conventional gap capacitor	**Type I** (Fig 2a)	wide gap capacitor	-wide gap -large area -high tuning voltage required **-low IMD**
	Type II (Fig 2b)	narrow gap capacitor	-narrow gap **-small area** **-low tuning voltage required** -large IMD
gap capacitor with high resistivity electrodes inside RF gap	**Type III** (Fig 3a)	short attached-bias-electrode capacitor (short **ABE** capacitor)	-wide RF gap (→ **low IMD**) -narrow DC bias gap -DC field perpendicular to RF field -DC electrodes attached to the RF electrodes -low tuning in RF range
	Type IV (Fig 3b)	long attached-bias-electrode capacitor (long **ABE** capacitor)	-wide RF gap (→ **low IMD**) -narrow DC bias gap -DC field parallel to RF field -DC electrodes attached to the RF electrodes **-large tuning in RF range**
	Type V (Fig 3c)	long isolated-bias-electrode capacitor (long **IBE** capacitor)	-wide RF gap (→ **low IMD**) -narrow DC bias gap -DC field parallel to RF field -DC electrodes isolated from the RF electrodes **-large tuning in RF range** -flexibility of biasing scheme

allel to that of the RF field. Finally, Fig. 3(c) shows a capacitor with long bias electrodes, but those electrodes are electrically isolated from the RF pads (the so-called "long IBE structure"). Similarly to the long ABE structure, the dc electric field of the long IBE structure is also parallel to that of the RF field. The overall gap-capacitor architectures are summarized in Table I.

Now that each geometry has been described, the electrical performance will be analyzed. Consider the cross-sectional view of the long ABE capacitor (type IV) and its associated equivalent circuit, as shown in Fig. 1(c). In the circuit, the upper branch consists of an equivalent series resistance of the highly resistive conductor line $R_{\rm DC}$ and a capacitance $C_{\rm DC}$ from the combined effects of C_1, C_2, and C_3. The lower branch has a series resistance $R_{\rm RF}$ and an RF capacitance $C_{\rm RF}$ with gap g defined primarily by the high-permittivity ferroelectric layer between the highly conductive conductors. It is assumed that the capacitance through the ferroelectric layer is dominant due to the relatively high dielectric constant of the ferroelectric material, and the capacitance through the substrate and the air may be ignored. Therefore, $C_{\rm RF}$, and the associated Q, as determined by $R_{\rm RF}$, is determined by the geometry of the metal. It is clear that for reduced IMD operation, the cutoff frequency of the dc-bias structure should be well below the RF frequency of operation of the tunable capacitor. This implies that $R_{\rm DC}$ should be as high as possible. The only restriction is that the time constant formed by this structure, i.e., $\tau_{\rm DC} = R_{\rm DC}C_{\rm DC}$, may limit the rate at which adjustment of the capacitance, i.e., tuning, may occur. At signal frequencies, the impedance of the RF path is much lower than that of the dc path and, therefore, the RF current travels through the ferroelectric material; however, the permittivity of this ferroelectric material has been adjusted by low-frequency tuning voltage applied by means of the dc path. In this way, the tuning and capacitance functionalities of the device are decoupled, and reduced IMD can be achieved at low tuning voltage.

III. FABRICATION

For device concept verification and performance comparison, the five types of gap capacitors mentioned above and in Table I (types I–V) are fabricated with RF electrodes of 1–2-μm thickness and 12–14-μm RF gap, and dc-bias electrodes of 1–2-μm spacing and 2–3-μm electrode width. Oxide electrodes, such as indium–tin–oxide (ITO) or lanthanum–strontium–cobalt–oxide (LSCO) of 3–10-nm thickness, are used for the high-resistivity dc-bias electrodes. The sheet resistance of these films is in the range of 2–3 $\times$ 10^4 Ω/sq. Alternate highly resistive materials, such as lightly doped silicon or polysilicon, could also be utilized.

Fig. 4 shows two fabrication processes utilized in the realization of the reduced IMD capacitors. Fig. 4(a) shows two sequential liftoff processes; the first for definition of the high-resistivity bias electrodes, and the second for definition of the high-conductivity RF electrodes. First, BST ferroelectric thin films (450-nm thick) epitaxially grown on sapphire substrates (430-μm thick) using combustion chemical vapor deposition (CCVD) [8] by MicroCoating Technologies Inc. (MCT), Chamblee, GA, are used as a starting substrate [see Fig. 4(a)1]. To create the highly resistive bias structure electrodes, an ITO layer 10 nm in thickness is deposited and patterned using RF sputtering and liftoff [see Fig. 4(a)2]. The measured sheet resistance of the ITO is 2–3 $\times$ 10^4 Ω/sq. Lastly, the RF conductors are formed using a standard liftoff process with 1-μm-thick copper and 0.3-μm-thick gold [see Fig. 4(a)3]. Since this process is an acid-free process, it prevents the BST layer from being damaged or degraded by any corrosive acidic chemical during the process.

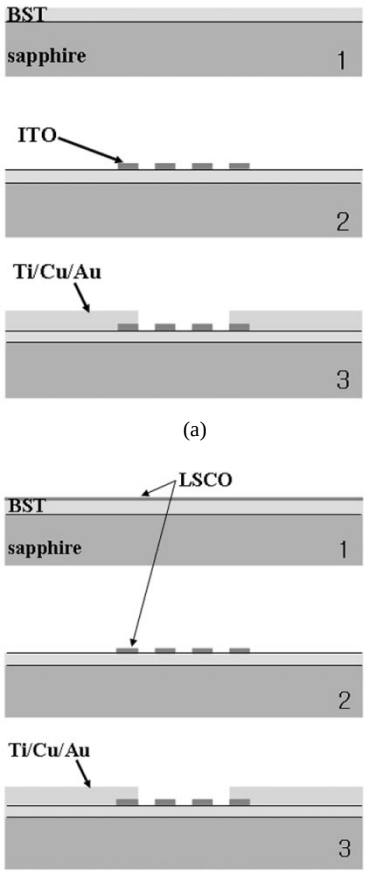


Fig. 4. Fabrication processes for ITO and LSCO electrode reduced IMD capacitors. (a) 1: BST/sapphire substrate. 2: ITO sputter deposition and patterning using liftoff. 3: RF pad patterning using liftoff. (b) 1: LSCO/BST/sapphire substrate. 2: LSCO pattering using etching. 3: RF pad patterning using liftoff.

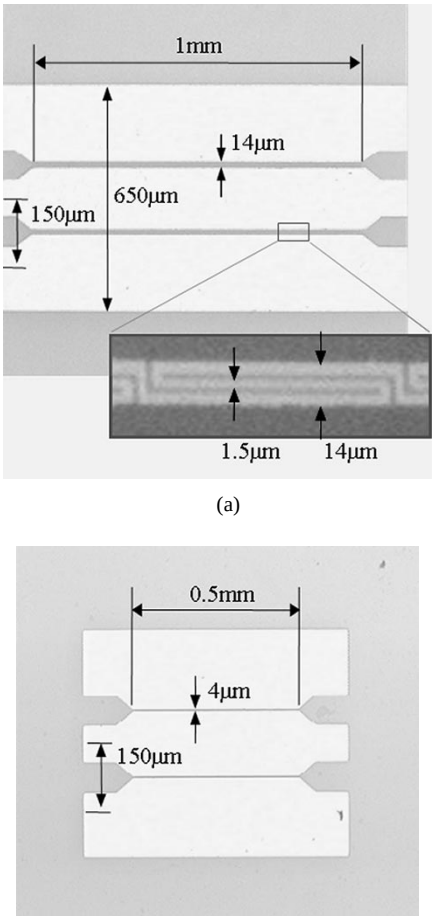


Fig. 5. Photomicrograph of the fabricated gap capacitors with ITO bias electrodes. (a) Long ABE capacitor (type IV, 14-μm RF gap, 1-mm RF electrode length, 1.5-μm dc-bias gap, and ten repeated bias structures), magnified unit bias electrodes in the inset (SEM photograph). (b) Conventional narrow gap capacitor for IMD comparison (type II, 4-μm gap, and 0.5-mm RF electrode length).

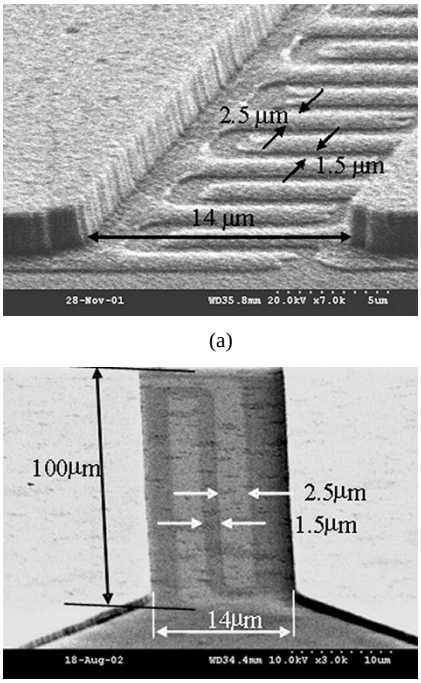
One drawback of the above process is the necessity for a separate sputter deposition step for the highly resistive material. It is known that CCVD can be utilized to deposit highly resistive oxides such as ITO and LSCO. Therefore, a manufacturing advantage can be obtained if, e.g., an LSCO layer can be deposited directly on the BST by CCVD. However, since CCVD is carried out at relatively high temperature, a liftoff process using conventional photoresists is infeasible. Therefore, a modified process requiring etching of the highly resistive material is required.

Fig. 4(b) shows a fabrication process, which uses one etch and one liftoff step. LSCO is grown on top of the BST layer on the sapphire substrate by MicroCoating Technologies Inc. using a sequential CCVD process [see Fig. 4(b)1]. Photoresist is patterned for dc-bias electrode definition. LSCO is etched in dilute hydrochloric acid and the photoresist is removed [see Fig. 4(b)2]. The RF conductor is formed as described above and shown in Fig. 4(b)3.

To minimize the parasitic capacitance between signal and ground lines, a shunt capacitor scheme was adopted using a coplanar-waveguide configuration. A fabricated device using ITO resistive electrodes is shown in Fig. 5. Fig. 5(a) shows a long ABE structure (type IV) with 1-mm-long RF electrodes, a 14-μm RF gap, ten repeated ITO bias electrode groups with 100-μm group pitch, and 1.5-μm dc-bias gap. Fig. 5(b) shows a conventional narrow gap capacitor (type II) with a 4-μm gap and 0.5-mm-long RF electrodes.

Since the thin ITO layer is optically transparent in visible wavelengths, scanning electron microscope (SEM) photographs are taken in the gap area for a clear structural viewgraph. Fig. 6(a) and (b) shows a short ABE structure (type III) and a long ABE structure (type IV), respectively. The RF gaps are 14-μm wide, the gap of the dc-bias electrode is 1.5-μm wide, and the width of the dc-bias electrode is 2.5-μm wide.

Fig. 7 shows gap capacitors with LSCO as a high-resistivity material. Four different samples are shown, respectively, (a) a conventional wide gap capacitor (type I), (b) a conventional narrow gap capacitor (type II), (c) a long ABE capacitor (type IV), and (d) a long IBE capacitor (type V). Note that LSCO is visible using an optical microscope. The RF gap, length of RF electrodes, spacing of the dc-bias electrode, and width of dc-bias electrode are 12 μm, 1 mm, 2 μm, and 2 μm, respectively. The length of the isolated electrodes is 1.2 mm.



(a)

(b)

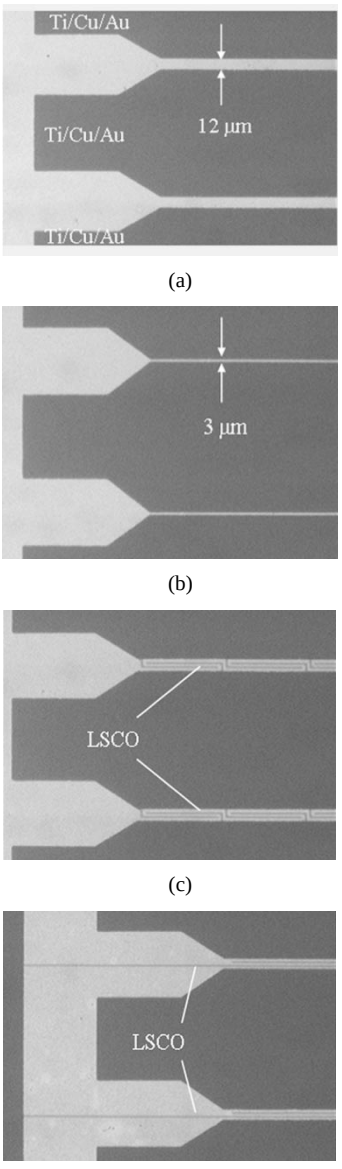
Fig. 6. SEM photograph of the fabricated gap capacitors with ITO bias electrodes. (a) Short ABE capacitor (type III). (b) Long ABE capacitor (type IV).

IV. RF Test and Simulation

A. Characteristics of Wide Gap Capacitor, Long ABE Capacitor, and Narrow Gap Capacitor

It is instructive to study the RF behavior of wide gap capacitors, narrow gap capacitors, and one of the reduced IMD capacitors (e.g., the long ABE structure) as a group. Assuming the geometries have been appropriately designed, the wide gap capacitor has the same capacitance and IMD behavior as the reduced IMD capacitor, but at greatly reduced tunability; the narrow gap capacitor has the same tunability as the reduced IMD capacitor, but at a greatly increased IMD. Hence, by comparison of the behavior of these three capacitor types, the simultaneous high tunability and low IMD of the reduced IMD architecture can be clearly seen.

The capacitance of a long ABE capacitor (type IV) fabricated using ITO and that of a conventional wide gap capacitor (type I) are compared as a function of frequency in Fig. 8. In the low-frequency region, the capacitance of the long ABE structure is attributed to the sum of the capacitance from RF electrodes (C_{RF}) and that from the high-resistivity bias electrodes (C_{DC}) [see Fig. 1(c)]. As the frequency increases, the impedance of the RF branch due to $C_{\mathrm{RF}}(=1/\omega C_{\mathrm{RF}})$ becomes smaller, while the impedance of the highly resistive bias structure is not changing much due to its smaller frequency dependence (R_{DC}). In the frequency range above 10 MHz, the overall impedance of the long ABE capacitor (type IV) is dominated by the RF path, resulting in its convergence to that of the conventional wide gap structure. This result demonstrates that the highly resistive bias line is not functioning as a capacitive component in the high-frequency regime. Meanwhile, the capacitance of the conventional wide gap capacitor is not dependent on the frequency, as expected.



(a)

(b)

(c)

(d)

Fig. 7. Photomicrograph of the fabricated gap capacitors with LSCO bias electrodes. (a) Wide gap capacitor (type I). (b) Narrow gap capacitor (type II). (c) Long ABE capacitor (type IV). (d) Long IBE capacitor (type V).

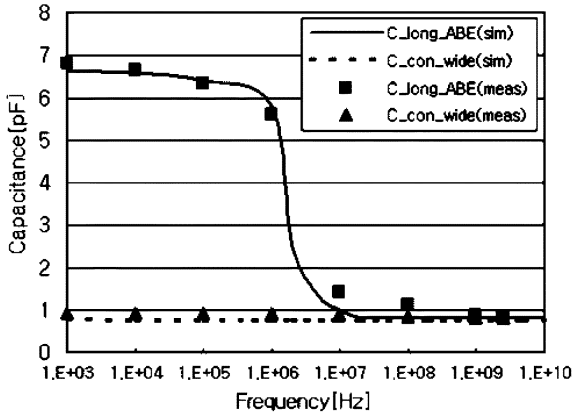


Fig. 8. Frequency response of the capacitance for a long ABE capacitor (type IV) and a conventional wide gap capacitor (type I). In the inset, long_ABE and con_wide represent a long ABE capacitor (type IV) and conventional wide gap capacitor (type I), respectively.

TABLE II
LUMPED PARAMETERS FOR A LONG ABE CAPACITOR (TYPE IV) AND A CONVENTIONAL WIDE GAP CAPACITOR (TYPE I)

	C_{DC}	R_{DC}	C_{RF}	R_{RF}
Long ABE capacitor (type IV)	6.8pF	$10^5\Omega$	0.80pF	5Ω
Wide gap capacitor (type I)	0	∞	0.75pF	5Ω

A circuit simulation is carried out using SPICE and *Microwave Office* (Appl. Wave Res. Inc.) with the simplified circuit in Fig. 1(c) inset to extract lumped parameter values. The simulation result of capacitance is also plotted in Fig. 8 with a solid and dashed line for the long ABE capacitor (type IV) and the conventional wide gap capacitor (type I), respectively. The extracted lumped parameters used for the simulation are summarized in Table II.

The measured capacitance and quality factor for three structures (types I, II, and IV) as a function of the dc-bias voltage at 2.5 GHz are shown in Fig. 9(a) and (b), respectively. Approximate tunability ($C_{\max}/C_{\min}$) of 1.27 at 30 V was obtained both for the narrow gap capacitor (type II) and the long ABE capacitor (type IV), while a tunability of only 1.08 was obtained for the wide gap capacitor. Q factors for all three structures were over 16 at zero-bias voltage. Note that the Q factor of the long ABE capacitor (type IV) was not materially degraded due to the highly resistive bias lines, as expected.

B. Short ABE Capacitor Versus Long ABE Capacitor

The capacitances of a conventional wide gap capacitor (type I), a short ABE capacitor (type III), and a long ABE capacitor (type IV) have been measured at 100 kHz and 2.5 GHz with zero bias and 30 V to determine and compare the frequency response and tunability of these structures. The measurement data are summarized in Table III. While the conventional wide gap capacitor (type I) shows little frequency dependence of capacitance, types III and IV show a large capacitance transition with frequency in the same fashion as shown in Fig. 8. However, the tunability of the short ABE capacitor (type III) at 2.5 GHz is the lowest of the three structures, which implies the dc field perpendicular to that of the RF signal is not contributing to permittivity change in the direction of the RF signal. Therefore, the short ABE (type III) structure is not suitable for reduced-IMD high-tunability capacitors.

C. Long ABE Capacitor Versus Long IBE Capacitor

All of the previously discussed capacitor architectures have two bias points at signal pad S and ground pad G. The long IBE capacitor (type V) has two additional bias pads, *V1* and *V2*, as shown in Fig. 3(c). The introduction of these independent bias pads offers additional flexibility in both tuning, as well as operation of the device in other applications. To assess these long IBE (type V) devices, their capacitance as a function of various bias schemes has been measured and compared with the previously discussed types I, II, and IV devices. All of the devices characterized in this section used LSCO as the highly resistive material (Fig. 7). The measured capacitance, tunability at 30 V, and Q factor are summarized in Table IV.

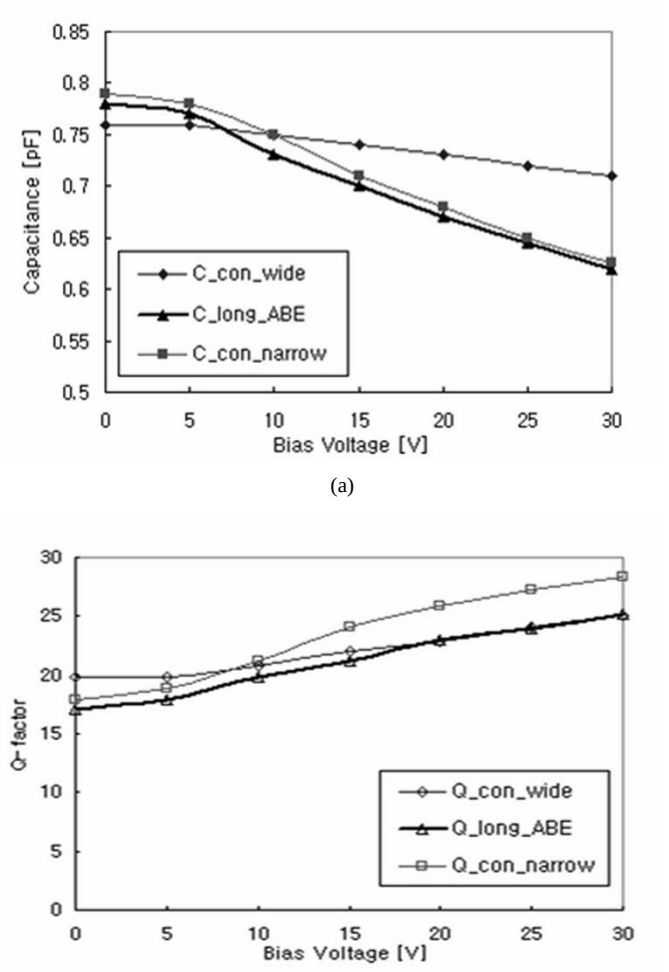


Fig. 9. Comparison of a conventional wide gap capacitor (type I), long ABE capacitor (type IV), and conventional narrow gap capacitor (type II) as a function of the dc-bias voltage at 2.5 GHz. (a) Capacitance versus bias voltage. (b) Q factor versus bias voltage. In the inset, con_wide, long_ABE, and con_narrow represent a conventional wide gap capacitor (type I), long ABE capacitor (type IV), and conventional narrow gap capacitor (type II), respectively. ITO is used for highly resistive dc-bias electrodes.

The capacitance and tunability of each architecture is slightly higher, and the Q factors slightly lower, than that of their ITO-based counterparts shown in Figs. 5 and 9. However, it is not clear whether this effect is intrinsic to the LSCO versus ITO or whether it is due to stoichiometric BST variations between each sample. In general, capacitance and tunability can be traded off against the Q factor by varying the stoichiometry of the BST film. Three different bias cases are applied to the long IBE (type V) capacitor. From the point-of-view of the tuning voltage, both the signal and ground pads were at or near ground since the excitation level of the RF source was low. The first case has 30 V applied to *V1* with *V2* held at ground. The second case has 30 V applied to *V1* and −30 V applied to *V2*. The third case has 30 V applied to both *V1* and *V2*. The second case shows the highest tunability (1 : 1.4) at 30 V, which is as high as that of the long ABE capacitor (type IV) at 30 V.

TABLE III
TUNABILITY COMPARISON OF A CONVENTIONAL WIDE GAP CAPACITOR (TYPE I), SHORT ABE CAPACITOR (TYPE III), AND A LONG ABE CAPACITOR (TYPE IV) AT 100 kHz AND 2.5 GHz

		Capacitance [pF]					
		Wide gap capacitor (type I)		Short ABE capacitor (type III)		Long ABE capacitor (type IV)	
		100kHz	2.5GHz	100kHz	2.5GHz	100kHz	2.5GHz
Bias voltage	0 V	0.74	0.68	3.10	0.73	4.56	0.79
	30V	0.69	0.64	1.86	0.69	2.40	0.60
Tunability (C_{max}/C_{min})		6.8%	5.9%	40.0%	5.5%	47.4%	24.1%

TABLE IV
TUNABILITY COMPARISON ACCORDING TO BIAS SCHEMES

	S[V]	G[V]	V1[V]	V2[V]	C_0[pF]	C_{30}[pF]	T_{30} (C_{max}/C_{min})	Q
Type I	30	0			1.0	0.9	1.11	11~13
Type II	30	0			1.28	0.78	1.64	9~14
Type IV	30	0			1.12	0.78	1.44	8~11
Type V	0	0	30	0	1.28	0.96	1.33	7~8
	0	0	30	-30	1.28	0.89	1.44	7~8
	0	0	30	30	1.28	0.97	1.32	7~9

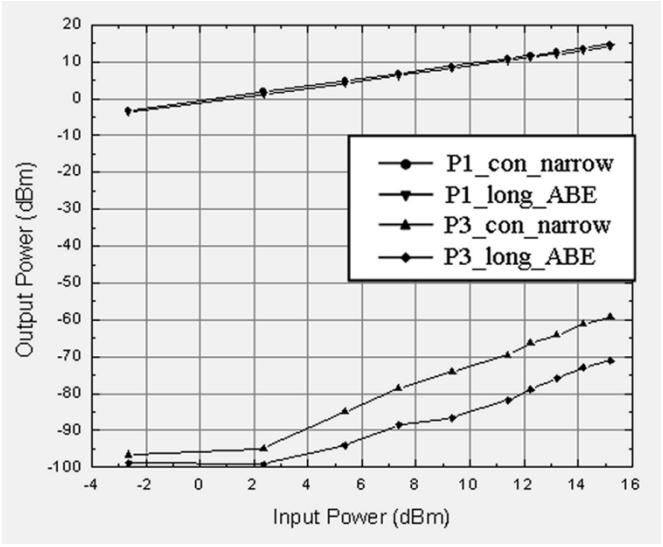


Fig. 10. Fundamental (P_1) and IM3 power (P_3) as a function of input power. In the inset, con_narrow and long_ABE represent a conventional narrow gap capacitor (type II) and a long ABE capacitor (type IV), respectively.

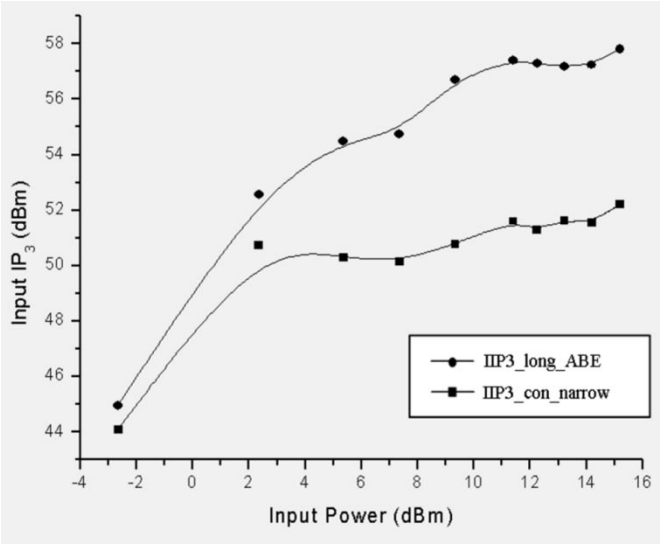


Fig. 11. Input IP_3 versus input power. In the inset, long_ABE and con_narrow represent a long ABE capacitor (type IV) and a conventional narrow gap capacitor (type II), respectively.

D. IMD Test

In order to unambiguously demonstrate that the capacitor architectures discussed above result in high tunability while simultaneously achieving low IMD, two-tone IMD tests have been performed for the long ABE capacitor (type IV) and the narrow gap capacitor with 4-μm gap (type II used for the IMD reference) in Fig. 5. The equal-power input signals are separated by 50 kHz ($f_{\mathrm{RF1}} = 1.9$ GHz, $f_{\mathrm{RF2}} = 1.90005$ GHz). A cancellation setup was used in order to keep the noise floor of the RF signal at a low level, making it possible to measure third-order intermodulation (IM3) distortion power over a wide range. Fig. 10 shows the fundamental output power and IM3 of the narrow gap capacitor (type II: an IMD reference structure) and the long ABE capacitor (type IV: a reduced IMD capacitor) as input power varies. At low input powers (below 2 dBm), the IM3 of both capacitors are close to each other, and the difference of IM3 of the two capacitors increases with increased input power due to the noise floor of the signal. Beyond input power of 10 dBm, the difference of IM3 is approximately 12 dB. The input third-order intermodulation intercept point (IIP_3) is plotted against the input power, as shown in Fig. 11. IIP_3 is calculated by measuring both fundamental output power and IM3, and applying the following formula:

$$\mathrm{IIP}_3 = \mathrm{OIP}_3 - \mathrm{Loss} = (P_{1\mathrm{out}} + \mathrm{IM}_3 \div 2) - \mathrm{Loss}. \quad (2)$$

Approximately 6-dB improvement of IIP_3 was obtained beyond the input power of 10 dBm. The high-frequency measurements at 2.5 GHz and two-tone test results at 1.9 GHz are summarized in Table V. Compared with the reference structure (type

TABLE V
SUMMARY OF HIGH-FREQUENCY MEASUREMENT AT 2.5 GHz AND TWO-TONE TEST AT 1.9 GHz FOR IIP3

	Wide gap capacitor		**Long ABE**		Narrow gap capacitor	
Capacitance [pF]	0V	30V	**0V**	**30V**	0V	30V
	0.76	0.71	**0.78**	**0.62**	0.78	0.62
Q-factor	19.8	25.0	**17.1**	**25.0**	18.0	28.3
Tunability (C_{max}/C_{min})	1.08		**1.27**		1.27	
IIP3	58dBm		**58dBm**		52dBm	

II), the same tunability and 6-dB IIP_3 improvement using the reduced IMD capacitor (types IV or V) can be achieved.

V. CONCLUSION

Low IMD tunable capacitor architectures with high-resistivity dc-bias structures within the RF gap were designed, fabricated, and tested. Five gap-capacitor architectures (two conventional gap capacitors; types I and II, and three bias-electrode capacitors with high resistivity dc-bias structure within an RF gap; types III–V) were characterized in detail. Thin-film oxide conductors (3–10-nm thick), such as ITO, and LSCO are used for highly resistive bias electrodes with the sheet resistance of 2–3 $\times$ 10^4 Ω/sq. The long ABE capacitor (type IV) and long IBE capacitor (type V) are suitable architectures for low IMD tunable capacitors. The long IBE capacitor (type V) has more degrees of freedom in biasing compared with the long ABE capacitor (type IV). The long ABE capacitor (type IV) and long IBE capacitors (type V) showed similar overall tunability ($C_{\max}/C_{\min}$) of 1.4 at 30 V. The performance of the reduced IMD capacitors showed 6 dB of improvement in IMD performance when compared with the equivalent conventional gap-capacitor design, where both structures showed tunability ($C_{\max}/C_{\min}$) of 1.27 at 30 V. From frequency response and impedance measurements, it was also concluded that the dc-bias structure did not significantly degrade the Q of the capacitor.

ACKNOWLEDGMENT

Deposition of epitaxially grown BST on sapphire was carried out at MicroCoating Technologies Inc. (MCT), Chamblee, GA.[1] All other microfabrication was carried out at the Microelectronics Research Center, Georgia Institute of Technology, Atlanta. Valuable technical discussions with P. Marry, T. Polley, and D. Kiesling, all of MCT, are gratefully acknowledged by the authors.

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