A Novel Integrated Decoupling Capacitor for MCM-L Technology

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Abstract:

This paper discuses the design, materials, fabrication and measurements of a novel integrated decoupling capacitor for MCM-L-based substrates. Based on modeling using the SIA Roadmap, it has been estimated that 13 - 72nF/cm^2 of specific decoupling capacitance will be required for the next decade. The capacitor in this paper addresses this need. The fabrication of the capacitor has been achieved using filled polymer materials in thin film form, with via diameters of 100um and below, through photodefinable processes. Dielectric constant as high as 65 with loss tangent below 0.05 and specific capacitance of 22nF/cm^2 have been achieved. The scattering parameters were measured up to 20 GHz using a network analyzer for various capacitor structrures to study input impedance and scaling of the devices. The input impedance of the capacitor is found to be low in the GHz range. The polymer-filled materials and capacitor structures are also scalable to a variety of sizes and values.

Key Words: decoupling capacitor, MCM-L, filled-polymer, composite, integrated, polyacrylonitrile, polyimide, photodefinable, polynorbornene, simultaneous switching noise (SSN), barium titanate ($BaTiO_3$), dielectric constant.

I. Introduction:

Decoupling capacitors, which act as a charge reservoir, are required to suppress the simultaneous-switching noise (SSN) which arises due to numerous drivers switching simultaneously in digital or mixed signal applications. Most MCMs fabricated today rely on surface mount capacitors for decoupling [1, 2]. However, surface mount devices are large in size, occupy space (low packaging efficiency) and have large parasitics which reduce their efficiency for decoupling. These bottlenecks can be overcome using a decoupling capacitor integrated into the substrate beneath the chip. Some benefits of integrated decoupling capacitors are: (1) better electrical performance; (2) increased packaging efficiency; (3) decrease in effective capacitance required as compared to surface mount devices due to reduced parasitics; and (4) elimination of a separate package and its assembly to the board. In this paper, a new technique to fabricate integrated decoupling capacitors at low temperatures (< 250 °C) consistent with MCM-L substrates is discussed. Details on design, material attributes, process steps, test, and rework of the capacitor are discussed.

I.1. Next Generation Requirements

The Semiconductor Industry Association (SIA) Roadmap provides details for the next decade of silicon feature size, power, bus width, frequency of operation, and voltage levels, based on handheld, telecom, and cost performance (e.g., computer) applications. This information was used to compute the decoupling capacitor requirements of two applications, namely, hand held and cost performance, using the equation [3, 4, 5]:

$$P = p(C_T V_{DD}^2 f)$$

where, P = power consumed, p = probability that a power transition occurs, f = clock frequency (Hz), C_T = effective chip capacitance, and V_{DD} = device voltage (V).

Assuming a maximum voltage variation of 10% (peak-peak), the capacitance C_T was computed as illustrated in Table 1. Using these data and assuming a 2um dielectric film thickness, the dielectric constant requirements for the two applications are calculated as shown in Table 2. From this table, a material with relative dielectric constant in the range of 28 - 164 is required for the next decade.

Table 1. Capacitance (nF/cm^2) required for next decade.

Years ----> Product	1995-1997	1998-2000	2001-2003	2004-2006
Hand Held	13	14	13	20
Cost Performance	39	43	51	72

Table 2. Dielectric constant required for next decade

Years ----> Product	1995-1997	1998-2000	2001-2003	2004-2006
Hand Held	30	32	28	46
Cost Performance	88	96	116	164

I.2. Prior Work:

Integration of decoupling capacitors in multichip modules has been pursued by many authors for various base substrate technologies. Some of these are:

(a) MCM-C related: Some of the earliest work reported was on capacitor integration in MCM-C substrates. This has largely been pursued by IBM [6, 7]. The difficulty lies in attaining a large capacitance which is an absolute requirement for decoupling capacitors for high performance systems [1, 8, 9].

(b) MCM-D related: Several authors are pursuing capacitor integration onto MCM-D substrates. Some of the methods that have been used are:

(1) Discrete and integrated capacitors fabricated using sol-gel technology. A deposition temperature near 650 °C is used with a resulting dielectric constant of >900 [10].

(2) Integrated capacitors fabricated on silicon substrates with solid top and bottom electrodes and Al_2O_3 (anodized

aluminum, ε_r = 9) dielectric layers. These dielectrics are formed by anodizing evaporated aluminum films to typical thicknesses of 0.15 um. Specific capacitances of 50nF/cm^2 have been achieved [11].
(3) Ta_2O_5 (Tantalum oxide) was previously introduced as a thin film surface mount decoupling capacitor [12]. Integrated capacitors using this material as a dielectric have been achieved by using sputtering techniques [13]. In that work, thin films of Ta_2O_5 were deposited on top of alumina substrates which had been smoothed by bright copper plating to improve yield. Specific capacitances of 20nF/cm^2 were achieved.

(c) MCM-L related: Benefits of using printed wiring board (PWB) as a substrate combined with other packaging techniques such as MCM-D type technology (a 'D-on-L' approach) include the possibility of fabricating large numbers of MCMs on a single, large area substrate. These MCMs can have through vias that allow for area array connection to the next level of packaging. This packaging approach has the potential of providing improved performance while maintaining low cost. This method is gaining attention in the packaging community [14, 15]. However, no significant work is reported regarding integration of decoupling capacitors in such a technology for high speed switching applications. The fundamental bottleneck of a MCM-L technology is low-temperature processing requirements (<230°C, optimum temperature ~180°C).

Liftoff and other techniques can be used for integrating capacitors; however, in this paper a different approach using ceramic filled polymer materials (composite material) has been taken. Polymers have the advantage of being processable at low temperatures while ceramics have good electrical properties needed for capacitors [16]. The filled polymers, therefore, can be expected to meet electrical and processing needs for MCM-L based technology. The approach taken at the Georgia Tech Packaging Research Center (PRC) is to extend this filled polymer technology to thin film form to achieve the large specific capacitance required to satisfy decoupling requirements as per the SIA roadmap.

II. Design:

The important criterion in designing a power distribution system is to provide a low impedance network with minimum equivalent series inductance (L_S) and small equivalent series resistance (R_S) over a broad bandwidth [1, 3, 8, 11]. Since decoupling capacitors form an important part of the power distribution system in a package, this criterion directly applies to capacitor design. Low impedance can be achieved by using thin film structures. The parasitic inductance and resistance are dictated by effective thickness and effective length the charges must travel during switching from the decoupling capacitor to the switching devices [17].

Minimum L_S can be achieved by placing the decoupling capacitor near the chip with multiple vias and lines connecting to the chip I/Os. The multiple vias and lines in parallel provide the necessary low inductance path to the switching device. However, another stringent requirement is that none of the signal vias pass through the high dielectric material of the capacitor to avoid severe signal degradation (through capacitive discontinuity). Minimum R_S can be achieved by using thick highly conductive electrodes (though this will not suffice at high frequencies). However, in the design a small resistance is allowed to quiet oscillations during switching. Figure 1 shows the MCM thin film structure on top of a printed wiring board (PWB) base layer with through vias. To allow for decoupling, the capacitors are designed in such a way that they are placed beneath the chips as the topmost layer. This topmost layer is patterned into regions of high and low dielectric constant material. The low dielectric constant material provides the path for signal I/Os and the high dielectric constant material is used to form the capacitor.

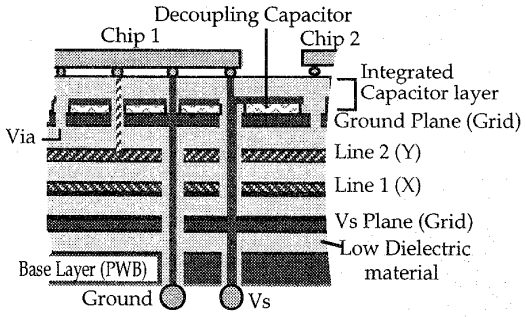

Figure 1. MCM built on top of a PWB substrate with integrated decoupling capacitors beneath and in between the chips.

Two layouts for integrating the capacitor near the chip are shown in Figures 2a and b. Figure 2a is a capacitor array consisting of several capacitors connected together in a matrix through top and bottom electrodes. This structure is easy to process because the vias required are large. The structure also has rework capabilities and the ability to precisely control the capacitance value by disconnecting selected lines interconnecting the capacitor array. In order to maintain high capacitance per unit area and for ease of processing the dielectric material is laid beneath the lines interconnecting the capacitors. Figure 2b is a grid-type interconnection where with the exception of signal interconnect vias the entire capacitor layer is formed from high dielectric constant material. The advantage of the grid-type structure lies in its maximum specific capacitance in comparison with the array-type. The difficulty in this case is in the fabrication of small vias in the high dielectric constant material. In this paper, both structures are built and tested. In both the structures the areas of the top electrodes are made slightly smaller than the areas of the high dielectric constant material in order to prevent shorting between the electrodes.

The minimum via size in the high dielectric constant material (Figure 2b) will be dictated by the capacitive discontinuity that can be tolerated on the signal line. This is produced by fringing fields and is dependent on:
- Thickness of the high dielectric material.
- Diameter of the via in the low dielectric material.
- Dielectric constant ratio of the two materials.

Another problem associated with capacitors is the standing wave resonance that can limit the performance of the capacitor (thereby decreasing decoupling efficiency) [4]. In order to maintain the standing wave resonance of

the capacitor structure above the chip operating frequency, it may be necessary to use several individual capacitor structures (array-type or grid-type) integrated beneath the chips.

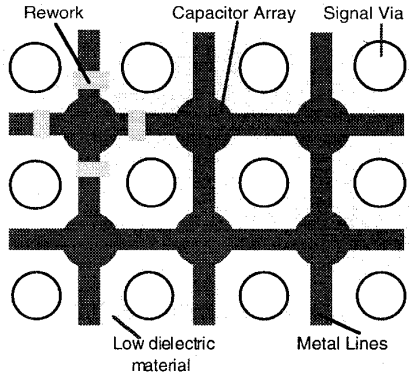

Figure 2a. Integrated array-type capacitor (interconnecting several small capacitors).

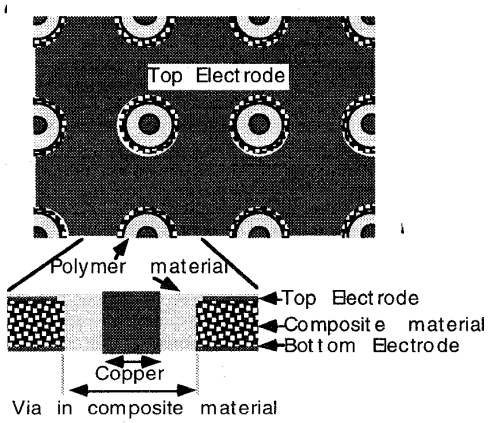

Figure 2b. Top and side view of a grid-type capacitor.

III. Capacitor Materials:

Polymers filled with ceramics have been studied for use as dielectric materials in thick film capacitors [16, 18] and have been used in the manufacturing of electronic substrates for high frequency operations [19]. Two approaches are available to achieve high dielectric constants using these composite materials: ceramic-filled dielectrics [16] and partially conductive-filled materials (i.e., grain boundary capacitors) [19]. In this paper the first approach is taken due to its inherently low leakage current. Dielectric constant above 50 can easily be achieved using ceramic filled polymers. However, there are several challenges in using composite materials:

(1) Determining a proper combination of materials to achieve good composite electrical and mechanical properties. A nondispersive dielectric material for operation into the GHz region is desired for decoupling capacitors.

(2) Achieving a uniform thin film of the composite over a large area of PWB.

(3) Patterning of the composite.

In composite materials, the volume fraction of ceramic in the polymer matrix is an important parameter which dictates the dielectric constant of the composite. The dielectric constant increases with increase in volume loading [16, 18, 19]. Thus in order to achieve a high loading the viscosity of the polymer material was decreased using suitable solvents recommended by the manufacturers. In this study several polymer materials were chosen on the basis of their good electrical and mechanical properties. Similarly, high dielectric constant ceramic fillers with small particle sizes were chosen. Table 3 lists the high dielectric constant ceramic particles selected.

Table 3. Ceramic fillers used.

Filler	Dielect. Const. (25°C)	loss-tangent (25°C)	Surface Area (m^2/g)	Average size (um)	Bulk Density g/cc
A	4,425	0.010	2.0 - 3.1	1.43	5.5
B	N/A	N/A	2.9 - 3.9	1.24	5.38
B'	N/A	N/A	—	~0.7	5.38
C	17,800	0.015	1.65-2.65	1.10	7.8
D	N/A	N/A	2.21	1.39	5.37

A: Barium Titanate (Ticon 5016)
B and B': High Purity Barium Titanate (HPBT-1, $BaTiO_3$)
C: Lead/Magnesium/Titanium oxide (Tamtron Y5V183U)
D: Barium Titanate
- Materials A - C were supplied by TAM Ceramics Inc.
- Material D was supplied by Ferro Corporation

The polymer materials were selected on the basis of their good electrical characteristics, high thermal stability, low processing temperatures (~250 °C) and good mechanical properties. A brief discussion and results are given for each of the composite materials studied.

III.1. Polyacrylonitrile (PAN)

PAN is a relatively low cost material and requires only the removal of solvent after casting onto a substrate. Two PAN homopolymer samples were filled with Type C and Type D ceramics respectively and cured at different temperatures. Both composite materials made using PAN were found to have a high dielectric loss (loss tangent). The films were porous in nature (possibly related to the molecular weight of the material) and had a rough surface (greater than 1um for 8um thick films). An approximate dielectric constant and loss tangent for C type filled material cured at different temperatures for 0.5 hr on a hot plate is shown in Table 4. The dielectric constant was found to increase with curing temperature due to oxidation. The loss tangent of the material was found to be a minimum when cured near 250 °C.

Table 4. Poly(acrylonitrile) composite (100KHz)

Filler type (volume % filled)	Cure Temp °C	dielectric constant	loss-tangent
None	200°C	3.86	0.0256
C (55 %)	150°C	~33	0.0415
C (55%)	250°C	~37	0.0252
C (55%)	300°C	~39	0.0427

III.2. Polynorbornene (PNB) based polymer

Polynorbornene with added functional groups (currently a proprietary product of BFGoodrich) has a very

low loss tangent, is moisture insensitive, and has a glass transition temperature above 380 °C. Table 5 outlines the results obtained using this material for two different volume percent loading. Several capacitor structures were made with wet etching techniques using dichlorobenzene as the etching solution; however, this wet etching technique still requires further optimization.

Table 5. Poly(norbornene) based material (100KHz):

Filler type (volume)	Cure Temp °C	dielectric const.	loss-tangent
None	300	2.65	0.0008
C (31%)	250	15	0.011
C (50%)	250	22	0.0083

III.3. Polyimides (PI)

(a) Non-photodefinable

PI2555 (Dupont Electronics) was investigated as a matrix material for filled polymer composites. Although successful films and structures were realized, typical problems faced were incomplete via opening and the development of cracks in the filled polymer during wet etching. Specific capacitance and loss tangent (at room temperature) of a 7.5 micron thick dielectric film of the material at 44% relative humidity were 3.2nF/cm^2 and 0.0097, respectively. Upon dehydration in a dry nitrogen ambient, the specific capacitance and loss tangent values both fell to 2.98nF/cm^2 and 0.0075 respectively. This effect is largely due to moisture absorption; it is well known that polyimide materials can absorb significant amounts of water from the ambient (especially incomplete imidized PI material). Further experiments on this material were not carried out in light of successful results obtained with photodefinable polyimide materials (described below).

(b) Photodefinable (PD)

When considering photodefinable composite materials, the issue of the transparency of the filler material to the wavelength of light used to expose the polymer matrix material must be addressed. Barium titanate is transparent to UV radiation (the region of interest). An additional problem is the scattering of light by the filler particles. In order to determine if highly loaded photodefinable composite material is a feasibility, several experiments with various volume loading (25% - 65%) were carried out for thickness ranging to 18um. Ultradel® 7505 Coating (supplied by Amoco) was used as the polymer matrix material. It can be cured between 200 °C - 300 °C. All films were cured at 225 °C (1/2 hr) on a hot plate. An increase in exposure (1500mJ to 2500mJ) with increase in volume loading and thickness was required to obtain structures below 100um in width. Photodefinable polyimide PD-2721 and PD-2722, products of Dupont Electronics, also showed promising results. However, these materials require curing above 250 °C for films with good electrical characteristics.

Figures 3a and b show the dielectric constant and the loss tangent of the Ultradel® material with different types of ceramic particles. Ceramic type C has the highest dielectric constant at 35% volume loading as compared to other fillers. Further, the loss tangent achieved using ceramic type A is the lowest. Ceramic type C was used in the making of a test vehicle due to its large dielectric constant values.

Figure 4 shows the capacitance and loss tangent of a parallel plate capacitor with a dielectric film thickness of 5.75um and dielectric constant of 47 at 100kHz (49% loading) as a function of both temperature and frequency. The temperature was changed by ramping down from 180 °C (temperature hold for 15min. at every 10 °C change) to room temperature. At low frequencies the loss tangent increases with increasing temperature and no significant changes are noticed at higher frequencies. At higher frequencies a decrease in capacitance (8%) for temperature changes from 25 °C to 180 °C is noted. With such small changes in capacitance (dielectric constant) and loss tangent with frequency (100KHz) and temperature, polyimide with filler type C can be used for making devices required for decoupling purposes. Decoupling capacitors require large capacitance and a change in capacitance (10%) does not perturb the performance significantly.

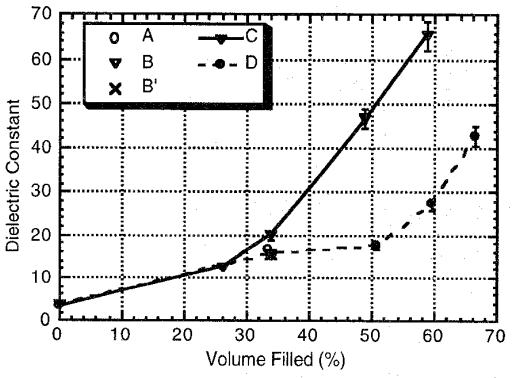

Figure 3a. Dielectric constant as a function of volume filled.

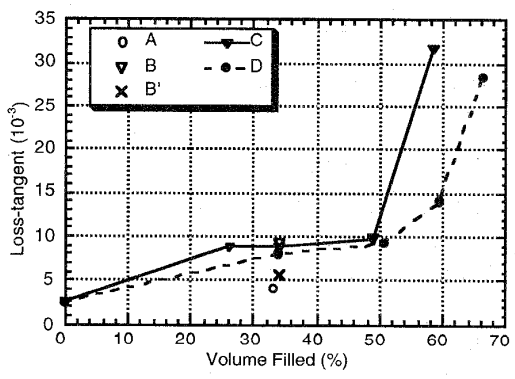

Figure 3b. Loss-tangent as a function of volume filled.

Specific capacitance of 22nF/cm^2 was achieved using filler type C (58% volume) in a photodefinable polyimide matrix. The dielectric breakdown and volume resistivity of all polyimide-based composite materials were determined to be >50X10^{6}V/m (using a 100V DC supply) and >10^9 Ω-cm (using a Keithley high input impedance meter) respectively.

It is important to note that in all the filled polymer materials, no visible voids (under 1000X magnification) or cracks were detected despite the stress generated (under processing and test conditions) due to the difference in the thermal expansion coefficient between the filler and the PD-PI material.

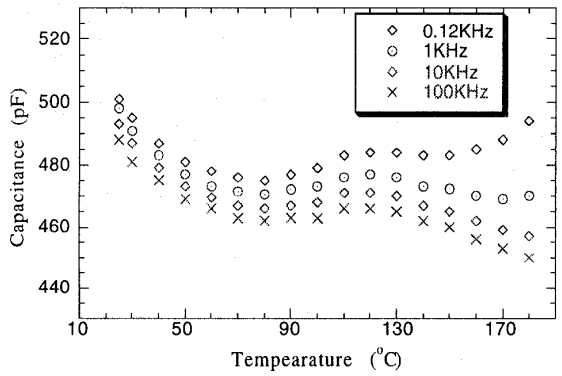

Figure 4a. Capacitance as a function of temperature and frequency for the PD-PI based material.

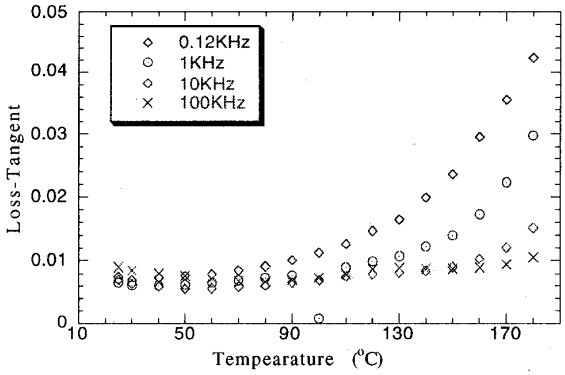

Figure 4b. Loss tangent as a function of temperature and frequency for a PD-PI based material.

IV. Test Vehicle:

A test vehicle was developed using photodefinable material (Ultradel® 7505 Coating) filled with type C filler (42% volume). The dielectric constant and loss tangent of the material measured at 10MHz was 32 and 0.0097 respectively. A film thickness of 4.1um ±0.25um (after cure) was achieved.

For the bottom electrodes Cr/Cu/Al layers were used and for the top electrode Al/Cu/Al layers were deposited. The thickness of the electrode materials was 1.5um for Cu and 0.5um for the Al layers. A 500Å Cr layer on glass substrate was used to improve adhesion with the glass substrate. The electrode materials were deposited using a filament evaporator. The fabrication technique of the capacitor structures is outlined in Figure 5.

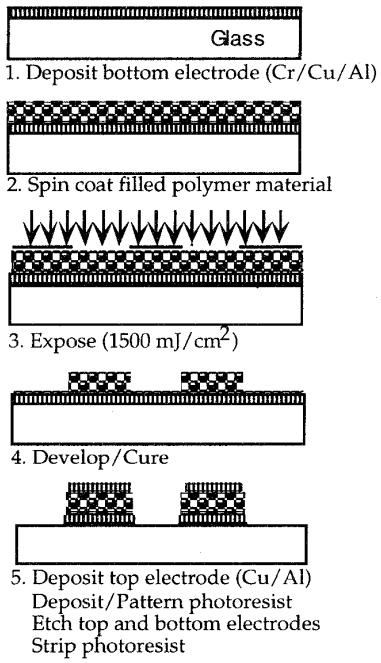

Figure 5. Processing steps used in making a test vehicle on glass substrate.

The test vehicle contains several capacitor structures with varying via diameter and dimensions. Pads at the end of the capacitor structure are incorporated for high frequency probing. Several, well known and studied test structures are also included on the vehicle for comparative study. The fabricated test vehicle is shown in Figure 6. The via diameters on the test vehicle range from 50 - 500um to study processing conditions of the photosensitive composite material.

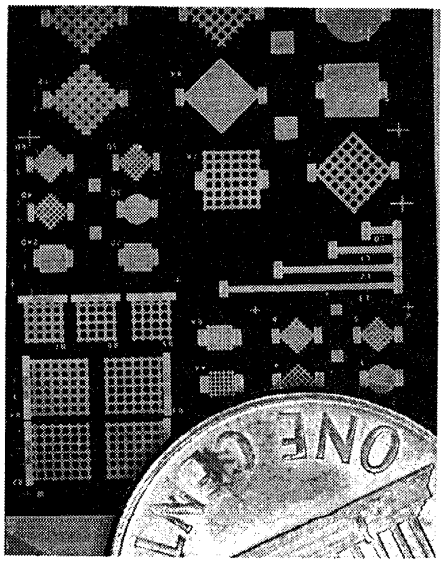

Figure 6. Test Vehicle on a glass substrate using PD-PI filled material (42% volume).

Figures 7 and 8 show a close-up view of the array type and the grid type capacitor structures. Metal is not covered over the whole dielectric material to avoid shorts with the bottom electrode. The substrate (glass) is visible through the opened via.

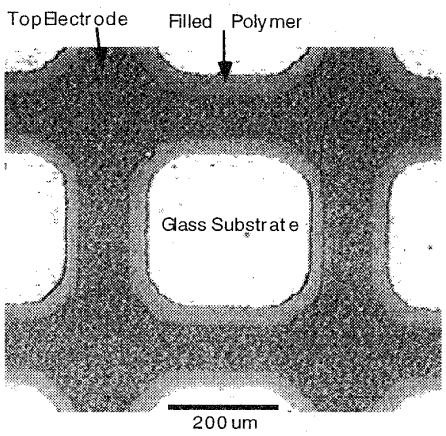

Figure 7. Section of an array-type structure.

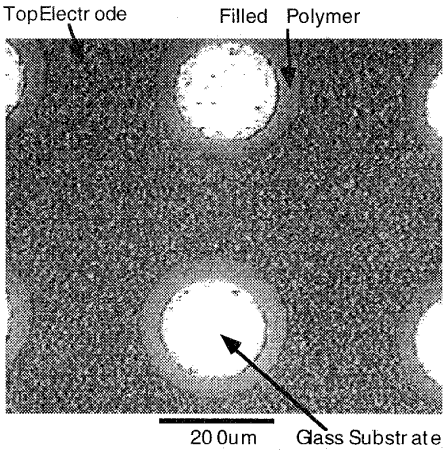

Figure 8. Section of a grid type capacitor structure.

IV.1. Test/Rework:

Two kinds of defects can occur on the capacitor array:
(1) Opens that reduce the capacitance of the array.
(2) Shorts between the top and the bottom electrodes.
The first defect is of minimum consequence due to the large array of capacitors that are fabricated. However, the second defect is fatal since the shorting of the two electrodes leads to the shorting of power for the entire substrate. Hence, defects producing shorts must be detected and repaired.

Shorts can easily be detected using a capacitance or a resistance meter. The most common type of short noted in this study was the shorting of the top and the bottom electrode from the sides of the filled polymer structures. In order to repair these shorted devices, two approaches were investigated: not to connect the capacitor array with a short to the chip I/Os, and to disconnect the section of the array with the faulty area as shown in Figure 9. In Figure 9 the copper line is disconnected around the shorted device by photodefining and copper/Al etching solutions. However, many other techniques can be applied to achieve this as explained in reference [3].

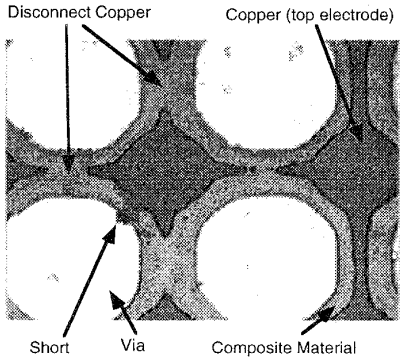

Figure 9. Repair of a shorted capacitor array built on top of a glass substrate.

IV.2. Measurement of the capacitor structures:

The fabricated capacitor structures were used for carrying out high frequency measurements. Since a maximum value capacitor is produced by electrodes with no via holes, these structures were also incorporated to provide a relative comparison. All these capacitor structures were fabricated on the same substrate. Scattering parameters (S-parameters) were measured from 50MHz to 20GHz using a network analyzer. A 50 Ohm coaxial cable and a coplanar ground-signal-ground (G-S-G) probe was used for measurement. The signal was launched onto the structure at two ends (two port measurement) using a conductor backed coplanar waveguide as shown in Figure 10.

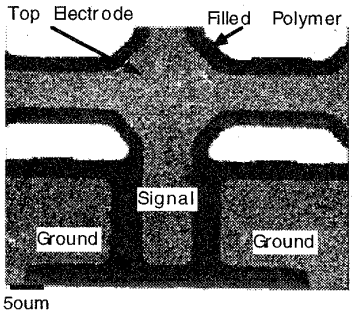

Figure 10. A typical coplanar probing structure for high frequency measurements of capacitors.

Figure 11 shows the measured devices. The dimensions of the capacitors used in the measurement are 1.3mm x 1.3mm and 2.6mm x 2.6mm for the grid-type capacitors (36 vias) and 1.3mm x 1.3mm for the array-type capacitor. A second type contains 49 capacitors (diameter = 100um) interconnected with a 35um wide line of 200um pitch. The via diameter of the grid-type capacitor used in measurement is outlined in Table 6, where the bottom electrode diameter is the same as that of the high

dielectric constant material. The capacitance values reported in Table 6 were measured at 100KHz using an LCR meter. Two sizes of capacitors were fabricated to study the scaling effect on performance. Scaling was done by multiplying the 1.3mm x 1.3mm devices by two times for the overall dimensions including the via diameters.

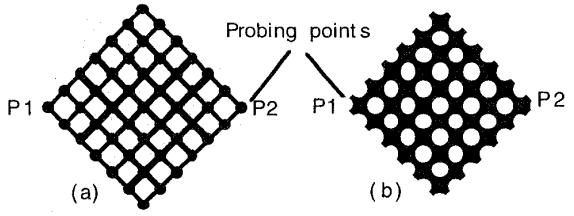

Figure 11. Capacitor structures used in measurement, (a) array-type capacitor, (b) grid-type capacitor

Table 6. Via diameters of devices used in measurement.

Dev.	Top electrode	Bottom electrode	C (pF)
A	0um	0um	98
B	130um	90um	73
C	190um	130um	44
D	2X190um	2X130um	395

Smith charts, Figure 12, show the measured (50 ohm terminated) S-parameters between 50MHz and 20GHz for different structures. Figure 12a shows the measured S-parameters for the solid plane (1.3mm x 1.3mm and 2.6mm x 2.6mm) and Figure 12b shows the S-parameters for structures with vias (devices C and D). In comparing these figures it can be noticed that there is no significant difference between solid electrodes and electrodes with via holes. In addition, Figures 12a and b indicate that the device can be scaled while maintaining low impedance in the GHz range. Figure 12c compares the S-parameters for an array-type capacitor and the solid plane capacitor (device A). Both the curves follow a similar path and thus indicating a similar input impedance pattern for the grid-type capacitor as the solid plane capacitor. From a simple equivalent model consisting of series resistance, inductance and capacitance derived for different structures (from 1-5GHz range using MDS), an increase in inductance with increase in the via size was noted. The array-type capacitor had the highest inductance value and the solid plane had the lowest. All structures showed inductance values below 0.5nH. The equivalent capacitance values derived on MDS were found to be near the 100KHz measured values. Note that since the lumped series RLC model does not perfectly depict the actual test structure, a more sophisticated model must be developed. In addition, the probing effect must be fully decoupled from the results (which was not carried out for these measurements). However, the results obtained give a good comparison for the fabricated structures and indicate that such structures built using composite materials can be used in decoupling.

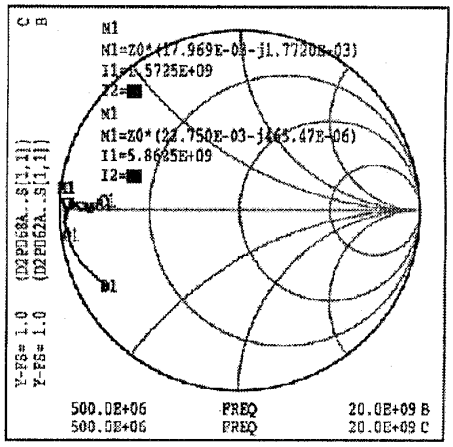

Figure 12a. S11-Parameters for solid plane capacitor (Devices A and 2XA parameters).

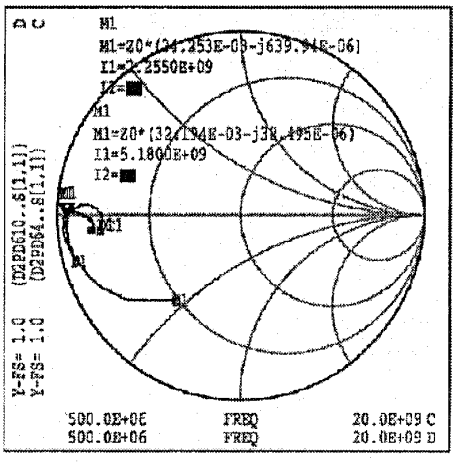

Figure 12b. S11-parameters for capacitor with large vias (devices C and D).

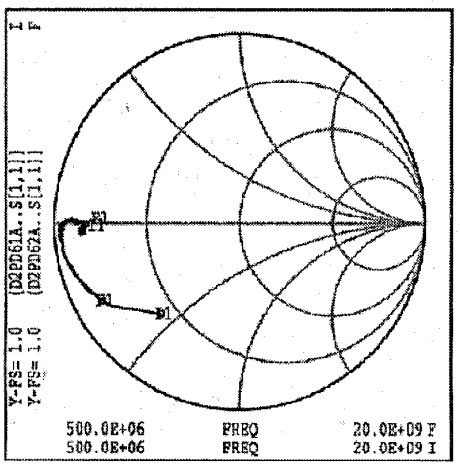

Figure 12c. S11-Parameters for a solid plane capacitor (device D) and array-type capacitor.

V. Conclusions:

A new technique of integrating decoupling capacitors near the chip is introduced with a reworkability scheme and minimum delay on the signal line. Based on modeling using the SIA Roadmap, it has been estimated that 13-72nF/cm^2 of decoupling capacitance is required for next decade. Filled polymer materials can be used to satisfy this need. The limitations imposed in integrating decoupling capacitors near the chip for MCM-L based technology has led to making of composite materials in thin film form (<5um) and using photodefinable polymers. A dielectric constant of 65 and a specific capacitance of 22nF/cm^2 with a loss tangent of 0.032 at 100 KHz has been achieved. This can further be increased with increase in volume filled at a cost of increase in loss tangent of the material. The dielectric loss tangent of the filled polymer material was found to be higher than the polymer matrix material used (except for polyacrylonitrile cured at 250 °C). A significant advantage in using composite materials in packaging is compatibility with polymer or laminate based MCM technology. For a test vehicle, a filled polymer material (PD-PI) cured at 225 °C (consistent with MCM-L requirements) with dielectric constant of 32 and loss tangent of 0.0097 was used. Measured scattering parameters of the capacitor structures in the test vehicle indicate that the devices can easily be scaled up without changing the performance significantly and also low input impedance is achieved into the GHz range for different structures as required of decoupling capacitors.

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