A Novel Integrated Decoupling Capacitor for MCM-L Technology

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***Abstract*— This paper discusses the design, materials, fabrication, and measurements of a novel integrated decoupling capacitor for MCM-L-based substrates. Based on modeling using the Semiconductor Industry Association Roadmap, it has been estimated that 13–72 nF/cm^2 of specific decoupling capacitance will be required for the next decade. The capacitor in this paper addresses this need. The fabrication of the capacitor has been achieved using filled polymer materials in thin film form, with via diameters of 100 μm and below, through photodefinable processes. Dielectric constant as high as 65 with loss tangent below 0.05 and specific capacitance of 22 nF/cm^2 have been achieved. The scattering parameters were measured up to 20 GHz using a network analyzer for various capacitor structures (varying geometry and dielectric thickness) to study input impedance and scaling of the devices.**

***Index Terms*—Barium titanate ($BaTiO_3$), decoupling capacitor, filled-polymer, integrated, large-area, lead magnesium niobate, MCM-L, polyimide, polynorbornene.**

I. Introduction

DECOUPLING capacitors, which act as a charge reservoir, are required to suppress the power distribution noise which arises due to numerous drivers switching simultaneously in digital or mixed signal applications. Most multichip modules (MCM's) fabricated today rely on surface mount capacitors for decoupling [1], [2]. However, surface mount devices are large in size, occupy space (resulting in low packaging efficiency) and have large parasitics which reduce their efficiency for decoupling. These bottlenecks can be overcome using a decoupling capacitor integrated into the substrate beneath the chip. Some benefits of integrated decoupling capacitors are:

1) better electrical performance;
2) increased packaging efficiency;
3) decrease in effective capacitance required as compared to surface mount devices due to reduced parasitics;
4) elimination of a separate package and its assembly to the board.

The Semiconductor Industry Association (SIA) Roadmap provides details for the next decade of silicon feature size, power, bus width, frequency of operation, and voltage levels, based on handheld, telecom, and cost performance (e.g., computer) applications. This information was used to compute the decoupling capacitor requirements for two applications, namely, hand held and cost performance, using the equation [3]–[5]

$$P = p(C_T V_{DD}^2 f)$$

where, P = power consumed, p = probability that a power transition occurs, f = clock frequency (Hz), C_T = effective chip capacitance, and V_{DD} = device voltage (V). Assuming a maximum voltage variation of 10% (peak–peak), the decoupling capacitance was computed as illustrated in Table I. From the table, capacitance in the range 13–72 nF/cm^2 is required over the next decade for hand held and cost performance applications.

TABLE I
CAPACITANCE (nF/cm^2) REQUIRED FOR NEXT DECADE

Years ---> / Product	1995-1997	1998-2000	2001-2003	2004-2006
Hand Held	13	14	13	20
Cost Performance	39	43	51	72

Integration of decoupling capacitors in multichip modules has been pursued by many authors for various base substrate technologies. Some of these are as follows.

1) *MCM-C Related*: Some of the earliest work reported was on capacitor integration into MCM-C substrates. This has largely been pursued by IBM [6], [7]. The difficulty lies in attaining a large capacitance which is an absolute requirement for decoupling capacitors for high performance systems [1], [8], [9].
2) *MCM-D Related*: Several authors are pursuing capacitor integration into MCM-D substrates. Some of the methods that have been used are as follows.
   a) Discrete and integrated capacitors fabricated using sol-gel technology. A deposition temperature near 650 °C is used with a resulting dielectric constant of >900 [10].
   b) Integrated capacitors fabricated on silicon substrates with solid top and bottom electrodes and Al_2O_3 (anodized aluminum, $\varepsilon_r = 9$) dielectric layers. These dielectrics are formed by anodizing evaporated aluminum films to typical thickness of 0.15 μm. Capacitance value of 50 nF/cm^2 have been achieved using this technology [11].

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c) Ta_2O_5 (Tantalum oxide) was previously introduced as a thin film surface mount decoupling capacitor [12]. Integrated capacitors using this material as a dielectric have been achieved by sputtering techniques [13]. In this work, thin films of Ta_2O_5 were deposited on top of alumina substrates which had been smoothed by bright copper plating to improve yield.

3) *MCM-L Related*: Benefits of using printed wiring board (PWB) as a substrate combined with other packaging techniques such as MCM-D type technology (a "D-on-L" approach) include the possibility of fabricating large numbers of MCM's on a single, large area substrate. These MCM's can have through vias that allow for area array connection to the next level of packaging. This packaging approach has the potential of providing improved performance while maintaining low cost. This method is gaining attention in the packaging community [14], [15]. However, no significant work is reported regarding integration of decoupling capacitors in such a technology for high speed switching applications. The fundamental bottleneck of a MCM-L technology is low-temperature processing requirements (<230 °C, optimum temperature ∼180 °C) and the aforementioned techniques used in MCM-D and MCM-C technologies are difficult to implement with MCM-L to achieve integrated capacitors at low temperatures and low cost.

To gain further insight into the material requirements that will satisfy the capacitance values of Table I, the capacitance data was converted into dielectric constant values assuming a 2 μm dielectric film thickness (single layer) and is outlined in Table II. From this table, a material with relative dielectric constant in the range of 25–170 is required to satisfy decoupling capacitance need. These values are not sufficiently large so as to require the use of high dielectric constant ceramic materials, and are not small so as to be satisfied using the interlayer dielectric materials alone. Thus, the best approach to achieving these values is to combine these technologies through the use of polymer-ceramic composite materials. Further, polymers have the advantage of being processable at low temperatures while ceramics have good electrical properties needed for capacitors [16]. The filled polymers, therefore, can be expected to meet electrical and processing needs for MCM-L based technology. The approach taken in this paper is to extend this filled polymer technology to thin film form to achieve the large specific capacitance required to satisfy decoupling requirements as per the SIA roadmap. Apart from the dielectric material challenge, a good technique of integrating decoupling capacitors (capacitor structures and fabrication technique) near the chip is required and this is discussed in the following section.

II. Design Issues

The important criterion in designing a power distribution system is to provide a low impedance network with minimum equivalent series inductance (L_s) and small equivalent series resistance (R_s) over a broad bandwidth [1], [3], [8], [11]. Since decoupling capacitors form an important part of the power distribution system in a package, this criterion directly applies to capacitor design. Low impedance can be achieved by using thin film structures. The parasitic inductance and resistance are dictated by effective thickness and effective length the charges must travel during switching activity from the decoupling capacitor to the switching devices [17].

TABLE II
Dielectric Constant Required for Next Decade

Years --> Product	1995-1997	1998-2000	2001-2003	2004-2006
Hand Held	30	32	30	46
Cost Performance	88	96	116	164

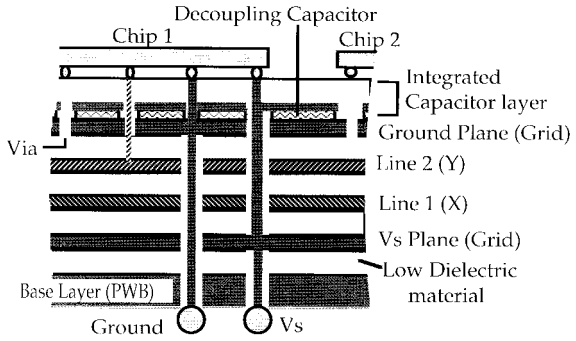


Fig. 1. MCM built on top of a PWB substrate with integrated decoupling capacitors beneath the chips.

Minimum L_s can be achieved by placing the decoupling capacitor close to the chip with multiple vias and lines connecting to the chip I/Os (porting of decoupling capacitor). The multiple vias and lines in parallel provide the necessary low inductance path to the switching device. Damping is required in decoupling capacitors to quiet resonance generated during switching. This can be achieved through the use of lossy electrodes or lossy dielectric. Use of lossy dielectric is not recommended because of the associated dc leakage current.

Fig. 1 shows the MCM thin film structure on top of a printed wiring board (PWB) base layer with through vias. To allow for decoupling, the capacitors are designed in such a way that they are placed beneath the chips at the topmost layer. This technique allows for multiple porting and which in turn allows for ease of control of impedance seen by the chip. The dielectric layer of the capacitor is patterned into regions of high and low dielectric constant material. The low dielectric constant material provides the path for signal I/Os and the high dielectric constant material is used to form the capacitor.

Two layouts for integrating the capacitor near the chip are shown in Fig. 2(a) and (b). Fig. 2(a) is a capacitor array consisting of several capacitors connected together in a matrix through top and bottom electrodes. This structure is easy to process because the vias required are large. The structure also has rework capabilities and the ability to precisely control the capacitance value by disconnecting selected lines interconnecting the capacitor array. In order to maintain high capacitance per unit area and for ease of processing the dielectric material is laid beneath the lines interconnecting the

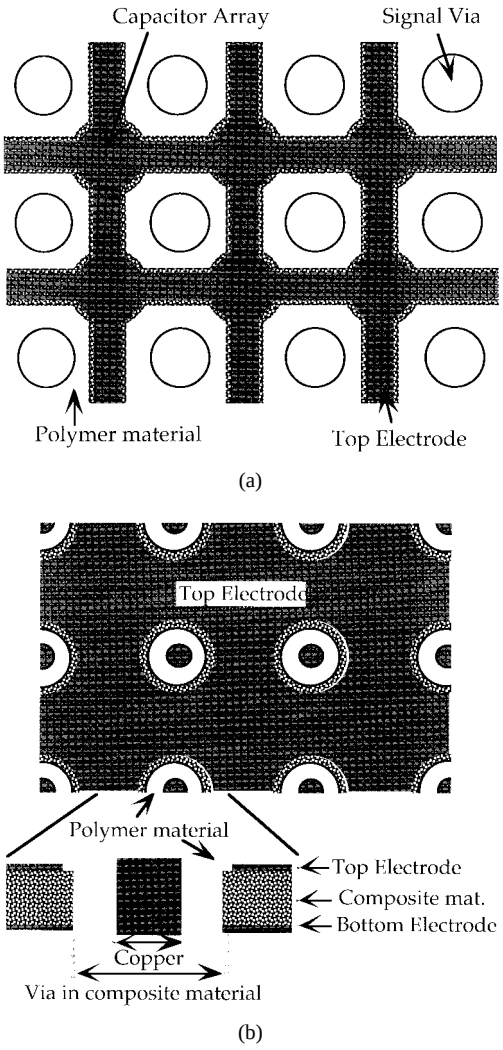


Fig. 2. (a) Integrated array-type capacitor (interconnecting several small capacitors) and (b) top and side view of a grid-type capacitor.

capacitors. Fig. 2(b) is a grid-type interconnection structure where with the exception of signal interconnect vias the entire capacitor layer is formed from high dielectric constant material. The advantage of the grid-type structure lies in its increased capacitance in comparison to the array-type due to larger metal area. The difficulty, however, is in the fabrication of small vias in the high dielectric constant material. In this paper, both structures are built and tested. In both the structures the areas of the top electrodes are made slightly smaller than the areas of the high dielectric constant material in order to prevent shorting between the electrodes.

From the design point of view, the minimum via size in the high dielectric constant material [Fig. 2(b)] will be dictated by the capacitive discontinuity that can be tolerated on the signal line. This is produced by fringing fields and is dependent on:

1) thickness of the high dielectric material;
2) diameter of the via in the low dielectric material;
3) dielectric constant ratio of the two materials.

The capacitive discontinuity experienced by a signal via passing through the high dielectric layer was computed to be in the range of 0.3–0.15 pF (dielectric thickness of 1–5 μm and ε_r of $\sim$32) and thus has negligible effect in most applications [18]. Another problem associated with the capacitor structure is the standing wave resonance that can limit the performance of the capacitor (thereby decreasing decoupling efficiency) [4]. In order to maintain the standing wave resonance of the capacitor structure above the chip operating frequency, it may be necessary to use several individual capacitor structures (array-type or grid-type) integrated beneath the chips. The resonance frequency can also be shifted to higher values by using the minimum dielectric thickness (dictated by processing) and dielectric constant that will suffice the capacitance value requirements.

The effect of electrode material on the dampening of resonance has been studied in [19] and has been found that copper electrode with thickness of about 1 μm with a capacitor of 1 cm $\times$ 1 cm dimensions and evenly probed simultaneously at 28 points is sufficient to dampen the resonance. Thus, indicating that the losses required to dampen the resonance can be achieved through the thickness control of the Cu electrodes and by probing at multiple points simultaneously. The structures proposed in this paper allow for multiple connections and the use of Cu metal for electrodes is also preferred for its compatibility with PWB through electroless plating. Benefits associated in using distributed thin film capacitor structure for decoupling has also been discussed by Ray *et al.* [20] and Lee *et al.* [21].

III. Polymer-Ceramic Composite Materials

Polymers filled with ceramics have been studied for use as dielectric materials in thick film capacitors [16], [22] and have been used in the manufacturing of electronic substrates for high frequency operations [23]. Two approaches are available to achieve high dielectric constants using these composite materials: ceramic-filled dielectrics [16] and partially conductive-filled materials (i.e., grain boundary capacitors) [22]. In this paper, the first approach is taken due to its inherent benefit of low leakage current. There are several challenges associated with using composite materials, as highlighted below, and some of these challenges were considered in evaluating materials for decoupling capacitors.

1) Determining an appropriate combination of materials to achieve good electrical and mechanical properties. A stable dielectric material for operation into the GHz region is desired for decoupling capacitors.
2) Achieving a uniform thin film of the composite over a large area of PWB.
3) Patterning of the composite.

In this study several ceramic filler materials were chosen on the basis of their good electrical characteristics and small particle sizes ($<$2 μm). Table III lists the high dielectric constant ceramic particles selected. The electrical properties are of sintered materials. The polymer materials were selected on the basis of their good electrical characteristics, high thermal stability, low processing temperatures ($\sim$250 °C), and good mechanical properties. Uniform dispersion of the ceramic particles in the polymer matrix was ensured through viscosity control and ball-milling over 100 h at 2–4 rpm. Thin films of

TABLE III
CERAMIC FILLERS USED

Filler	Dielect. Const. (25 °C)	loss-tangent (25 °C)	Surface Area (m^2/g)	Average size (um)	Bulk Density g/cc
A	4,425	0.010	2.0 - 3.1	1.43	5.5
B	N/A	N/A	2.9 - 3.9	1.24	5.38
B'	N/A	N/A	----	~0.7	5.38
C	17,800	0.015	1.65-2.65	1.10	7.8
D	N/A	N/A	2.21	1.39	5.37

composite materials were deposited using a spin coat technique on metal coated glass substrates. The films were then soft-baked at 70 °C (15 min) and 130 °C (30 min) on hot-plates to remove solvents, and finally cured at the respective curing temperatures of the polymer materials (shown in the table below for each polymer used in this study). Low frequency electrical characterization of the films was carried out using several parallel plate capacitors. The bottom electrode was maintained the same for all these capacitors and the top electrode was patterned, photo-processing, to several area electrodes (0.42 cm $\times$ 0.42 cm). Film thickness was measured using a Tencor profilometer and uniform film thickness across the substrate was assured.

In composite materials, the volume fraction of ceramic in the polymer matrix is an important parameter which dictates the dielectric constant of the composite. The dielectric constant increases with increase in volume loading [16], [22], [23]. Composites with varying volume loading have been studied in this work. The volume loading in the composite was calculated from the measured weight percent of polymer (solid content) and ceramic powder used in the composite mix and their respective nominal density. A brief discussion and results are given below for each of the composite materials studied.

A. Polyacrylonitrile (PAN)

Polyacrylonitrile is a relatively low cost material and requires only the removal of solvent after casting onto a substrate. Two PAN homopolymer samples were filled with Types C and D ceramics, respectively, and cured at different temperatures. Both composite materials using PAN were found to have a high dielectric loss (loss tangent). The films were porous in nature (possibly related to the molecular weight of the material) and had a rough surface ($\sim$1 mm for 8 μm thick films) and films below 5 μm were difficult to achieve with minimum pin-hole defects. An approximate dielectric constant and loss tangent for C type filled material cured at different temperatures for 0.5 h on a hot plate is shown in Table IV. The dielectric constant was found to increase with curing temperature due to oxidation. The loss tangent of the material was found to be a minimum when cured near 250 °C.

B. Polynorbornene (PNB) Based Polymer

Polynorbornene with added functional groups (currently a proprietary product of BFGoodrich) has a very low loss tangent, is moisture insensitive, and has a glass transition temperature above 380 °C. Table V outlines the results obtained using this material for two different volume percent loading. Several capacitor structures were made with wet etching techniques using dichlorobenzene as the etching solution; however, this wet etching technique still requires further optimization.

TABLE IV
POLY(ACRYLONITRILE) COMPOSITE (100 KHz)

Filler type (vol. % filled)	Cure Temp °C	ε_r	tan-δ
None	200 °C	3.86	0.026
C (55%)	150 °C	~33	0.042
C (55%)	250 °C	~37	0.025
C (55%)	300 °C	~39	0.043

TABLE V
POLY(NORBORNENE) BASED MATERIAL (100 KHz)

Filler type (volume)	Cure T (°C)	ε_r	tan-δ
None	300	2.65	0.0008
C (31%)	250	15	0.011
C (50%)	250	22	0.008

C. Polyimides (PI)

1) Non-Photodefinable: PI2555 (Dupont Electronics) was investigated as a matrix material for filled polymer composites. Although successful films and structures were realized, typical problems experienced were incomplete via opening and the development of cracks in the filled polymer during wet etching. Further experiments on this material were not carried out in light of successful results obtained with photodefinable polyimide materials (described below).

2) Photodefinable (PD): When considering photodefinable composite materials, the issue of the transparency of the filler material to the wavelength of light used to expose the polymer matrix material must be addressed. Barium titanate is transparent to UV radiation (the region of interest). An additional problem is the scattering of light by the filler particles. In order to determine if highly loaded photodefinable composite material is a feasibility, several experiments with various volume loading (25–65%) were carried out for thickness ranging from 5–18 μm. Ultradel® 7505 Coating (Amoco) was used as the polymer matrix material. It can be cured between 200–300 °C. All films were cured at 225 °C (1/2 h) on a hot plate. An increase in exposure (1500–2500 mJ/cm^2) with increase in volume loading and thickness was required to obtain structures with 100 μm vias. Photodefinable polyimide PD-2721 and PD-2722 (Dupont Electronics) also showed promising results. However, these materials require curing above 250 °C for films to ensure good electrical characteristics.

Fig. 3(a) and (b) show the dielectric constant and the loss tangent of the Ultradel® material with different types of ceramic particles. Ceramic type C has the highest dielectric constant at 35% volume loading as compared to other fillers.

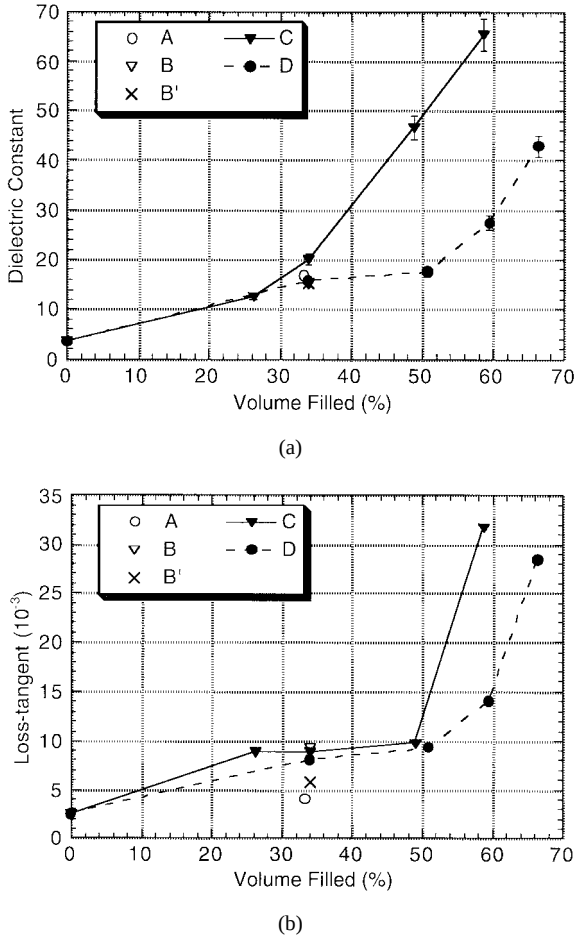


Fig. 3. (a) Dielectric constant as a function of volume filled and (b) loss-tangent as a function of volume filled.

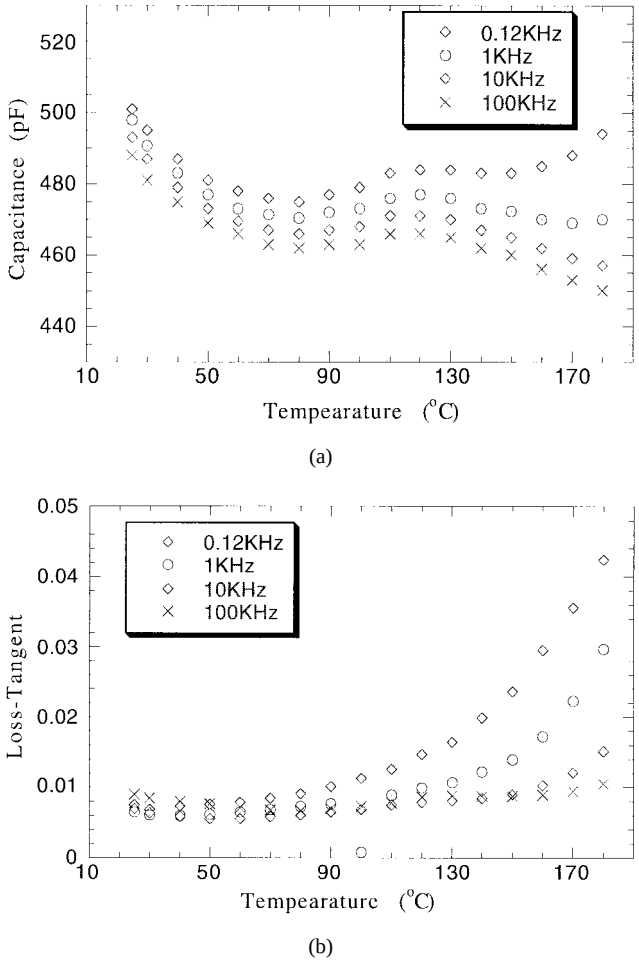


Fig. 4. (a) Capacitance as a function of temperature and frequency for a PD-PI based material and (b) loss tangent as a function of temperature and frequency for a PD-PI based material.

Further, the loss tangent achieved using ceramic type A is the lowest. Ceramic type C was used in the making of a test vehicle due to its large dielectric constant values. Fig. 4 shows the capacitance and loss tangent of a parallel plate capacitor with a dielectric film thickness of 5.75 μm and dielectric constant of 47 at 100 KHz (49% loading) as a function of both temperature and frequency. The temperature was changed by ramping down from 180 °C (temperature hold for 15 min at every 10 °C change) to room temperature. The loss tangent increases with increasing temperature at low frequencies and no significant changes are noticed at higher frequencies. At higher frequencies a decrease in capacitance (8%) for temperature changes from 25 to 180 °C is noted. With such small changes in capacitance (dielectric constant) and loss tangent with frequency (100 KHz) and temperature, polyimide with filler type C can be used for making devices required for decoupling purposes. Decoupling capacitors require large capacitance values and allow for large tolerances ($\sim$20%), and a change in capacitance below 10% will not perturb the performance significantly.

Capacitance of 22 nF/cm^2 with a loss-tangent of 0.032 was achieved (satisfying hand held application need) using filler type C (58% volume) in a photodefinable polyimide matrix. The dielectric breakdown and volume resistivity of all polyimide-based composite materials were determined to be $>50 \times 10^6$ V/m (using a 100 V DC supply) and $>10^9$ Ω-cm (using a Keithley high input impedance meter), respectively. Further increase in dielectric constant is required to satisfy the decoupling capacitance for cost performance product applications over the next decade.

IV. Decoupling Capacitor Test Vehicle

A test vehicle was designed to study processing conditions and dielectric properties of the composite materials, and geometrical effects of the capacitor structures. The structures included in the test vehicle are:

1) different via sizes (50–500 μm), along with varying dielectric thickness, in the composite material to study the processing conditions;
2) solid parallel plate capacitors and microstrip lines with varying lengths to evaluate the dielectric properties;
3) grid-type and array-type capacitors with varying dimensions to study the geometrical effects.

The fabrication steps for the test vehicle are outlined in Fig. 5. Glass substrates were used in this study for their uniformity as compared to PWB's. Photodefinable material (Ultradel® 7505 Coating) filled with type C filler (42% volume) was used as the dielectric material. The electrode metals

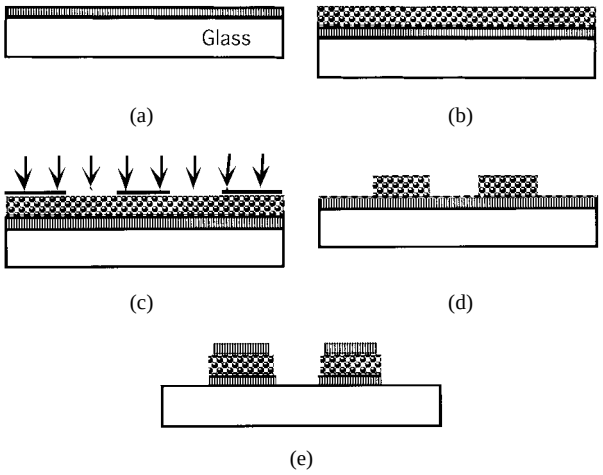


Fig. 5. Processing steps used in making a test vehicle on glass substrate: (a) deposit electrode (Cr/Cu/Al), (b) spin coat composite material, (c) expose (1500 mJ/cm^2), (d) develop/cure, and (e) deposit top electrode (Al/Cu/Al) deposit/pattern photoresist etch top and bottom electrodes strip photoresist.

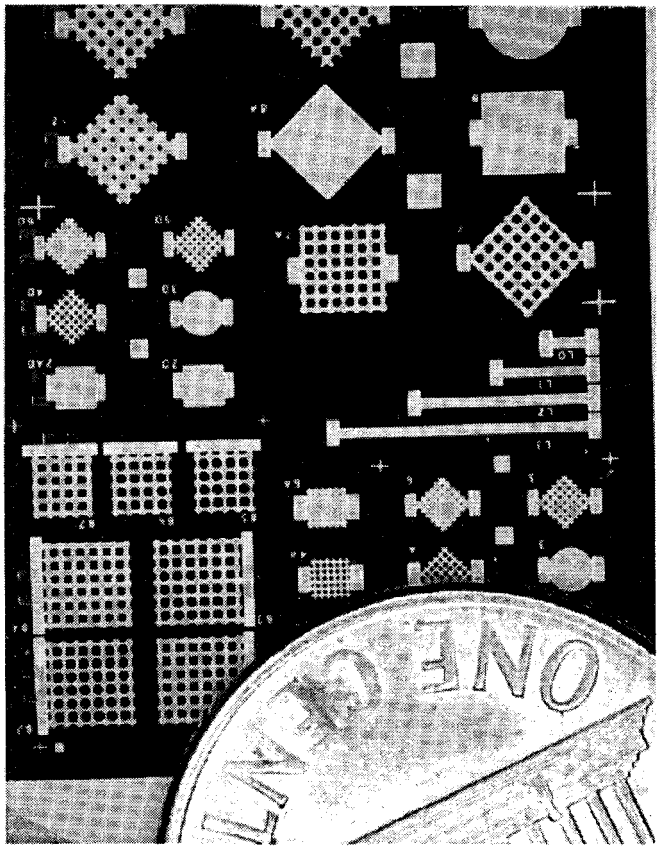


Fig. 6. Photomicrograph of a test vehicle fabricated on a glass substrate using PD-PI filled material (42% volume).

were deposited using a filament evaporator. For the bottom electrode Cr/Cu/Al layers were used and for the top electrode Al/Cu/Al (0.5 μm/0.5 μm/0.5 μm) layers were deposited. A Cr layer with the bottom electrode was used to improve adhesion with the glass substrate and adhesion promoter was required to improve adhesion of the composite film to the bottom metal electrode.

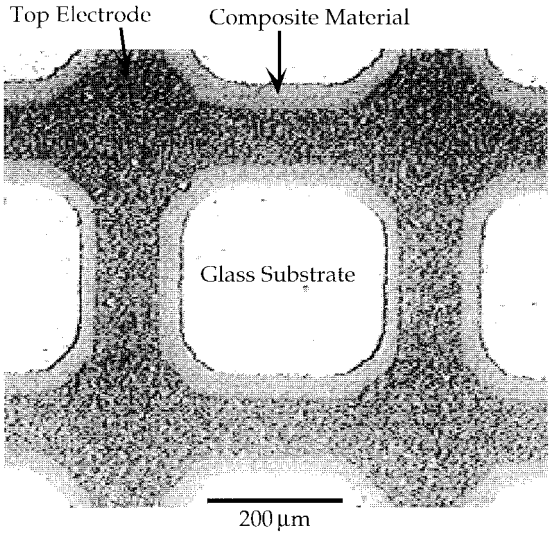


Fig. 7. Section of an array-type capacitor structure.

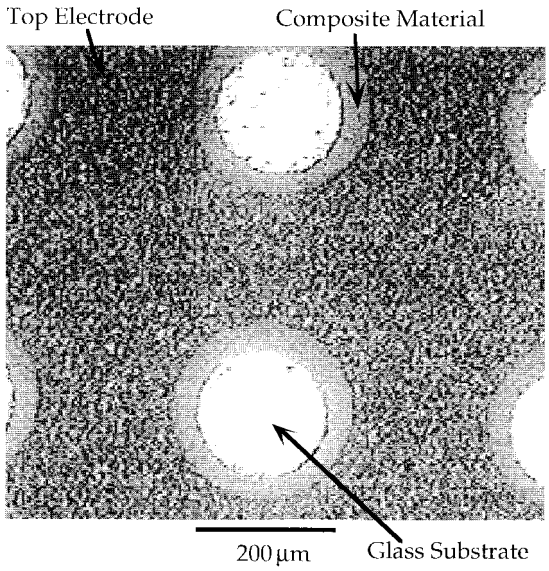


Fig. 8. Section of a grid-type capacitor structure.

Photograph of a fabricated test vehicle is shown in Fig. 6. A close-up view of the array type and the grid type capacitor structures is shown in Figs. 7 and 8, respectively. These figures indicate good feature definition of the composite film. Metal is not covered over the whole dielectric material to avoid shorts with the bottom electrode. The substrate (glass) is visible through the opened via. In all the test structures the via diameter in the top electrode is made larger than the bottom electrode vias. The bottom electrode vias are of the same dimension as that of the dielectric material. Two samples with film thickness (after cure thickness) of 4.1$\pm$0.25 μm and 2.4$\pm$0.35 μm were fabricated using the same composite material and electrode metals. The resulting dielectric constant and loss tangent of the material measured at 10 MHz was 32$\pm$3 (stable in the GHz range) and 0.01, respectively, for both the samples.

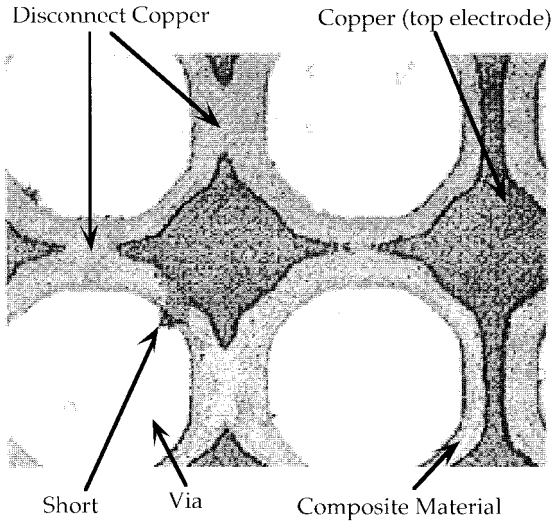


Fig. 9. Repair of a shorted capacitor array built on top of a glass substrate.

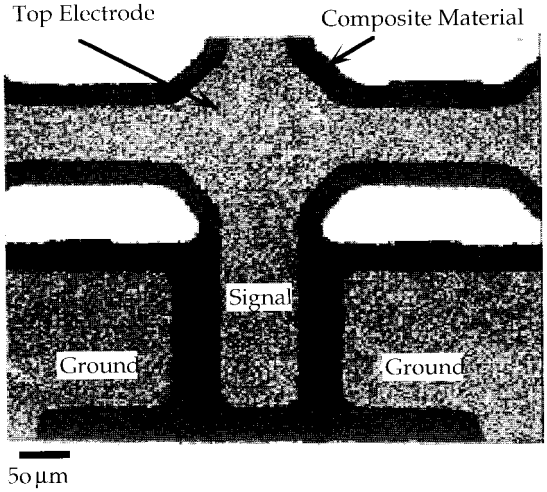


Fig. 10. A typical coplanar probing pad for high frequency measurement of capacitor structures.

A. Test/Rework

Two kinds of defects can occur on the capacitor array:

1) opens that reduce the capacitance of the array;
2) shorts between the top and the bottom electrodes.

The first defect is of minimum consequence due to the large array of capacitors that are fabricated. However, the second defect is fatal since the shorting of the two electrodes leads to the shorting of power for the entire substrate. Hence, defects producing shorts must be detected and repaired.

Shorts can easily be detected using a capacitance or a resistance meter. The most common type of short noted, visually under a microscope, in this study was the shorting of the top and the bottom electrode from the sides of the filled polymer structures. In order to repair these shorted devices, two approaches were investigated:

1) not to connect the capacitor array with a short to the chip I/Os;
2) to disconnect the section of the array with the faulty area as shown in Fig. 9.

In Fig. 9 the copper line is disconnected around the shorted device by photodefining and copper/Al etching solutions. However, many other techniques can be applied to achieve this as explained in [3]. Determining the exact location of the shorts in a capacitor plane is difficult and requires further work.

V. Measurement of Capacitor Structures

Scattering parameters (two port s-parameters) were measured from 500 MHz to 20 GHz using a HP8510C Vector Network Analyzer and Cascade Microtech air coplanar waveguide probes with ground-signal-ground configuration (150 μm pitch). On-wafer line-reflect-match (LRM) error correction calibration were carried out using commercially available impedance standard substrate (ISS). The signal was launched onto the structure at two ends (two port measurement) using a conductor backed coplanar waveguide as shown in Fig. 10. Note that the effect of probe pads has not been decoupled from the measured data.

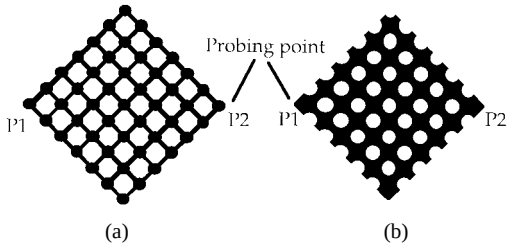


Fig. 11. Capacitor structures used in measurement: (a) array-type capacitor and (b) grid-type capacitor.

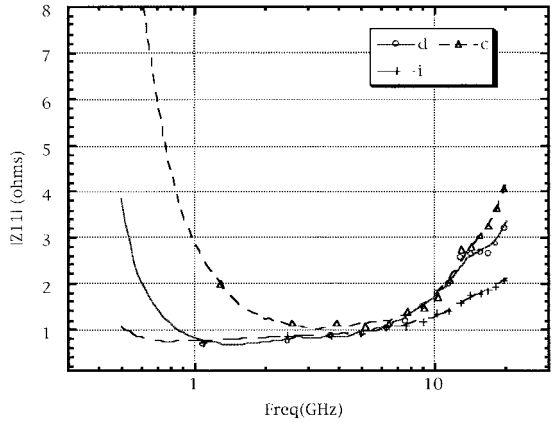
Fig. 11 shows the layout of measured devices and the probe points (high frequency measurement). The outer dimensions of the capacitors used in the measurement are 1.2 mm $\times$ 1.2 mm and 2.4 mm $\times$ 2.4 mm for the grid-type capacitors (36 vias), and 1.3 mm $\times$ 1.3 mm and 2.6 mm $\times$ 2.6 mm for the array-type capacitors. The second type contains 49 capacitors (100 and 200 μm diameter for 1.3 and 2.6 mm capacitors, respectively) interconnected uniformly (same spacing between the capacitors as the capacitor diameters) with microstrip lines (35 and 70 μm wide). Some of the capacitor structures used in the measurement (varying geometry and dielectric thickness) are highlighted in Table VI. This table also highlights the capacitance values (measured at 100 KHz using a LCR meter), dc series resistance (R_s) and measured input impedance at different frequencies. Capacitors a- through g-type are made with a dielectric thickness of 4.1 $\pm$ 0.25 μm and capacitors h- through k-type are with 2.4 $\pm$ 0.35 μm dielectric thickness.

A. Comparison of Different Capacitor Structures

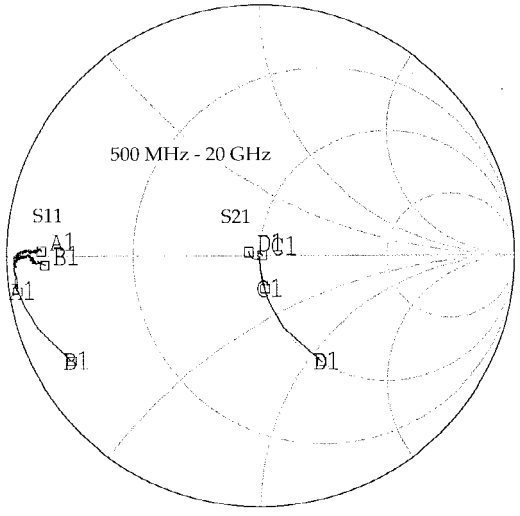
A comparison of the input impedance (derived from s-parameters), Fig. 12(a), of solid plane capacitor structures (c, d, and i-type) indicate that the larger capacitor structure (d-type) have lower impedance over a broader frequency range in comparison to its smaller counter part (c-type). Similarly the thinner capacitor structure (i-type) have lower impedance over a broad frequency range as compared to their thicker counter-

TABLE VI
CAPACITOR STRUCTURES USED IN MEASUREMENTS

Cap. Type	Grid (G) Array (A)	Dimensions	Via Diam. (μm)	C (pF)	Rs (Ω)	|Z11| (Ω) ~1 GHz	|Z11| (Ω) ~10 GHz	dB(S12) ~1 GHz
a	A	1.3 X 1.3	—	51	—	5.5	2.5	-14
b	A	2.6 X 2.6	—	210	0.30	1.1	2.6	-26
c	Solid	1.2 X 1.2	NA	98	0.07	2.5	1.8	-20
d	Solid	2.4 X 2.4	NA	395	0.09	0.8	1.6	-30
e	G	2.4 X 2.4	242	300	0.11	0.9	2.1	-29
f	G	2.4 X 2.4	288	263	0.12	1.0	2.4	-27
g	G	2.4 X 2.4	348	188	0.24	1.3	3.2	-24
h	Solid	1.2 X 1.2	NA	255	—	1.2	—	-27
i	Solid	2.4 X 2.4	NA	802	0.30	0.7	1.2	-38
j	G	2.4 X 2.4	288	464	0.15	0.8	2.1	-33
k	G	2.4 X 2.4	348	333	0.26	1.0	2.7	-30



(a)



(b)

Fig. 12. (a) Measured input impedance of different structures (c-, d-, and i-type) and (b) measured s-parameters of thin film capacitors (c- and d-type).

part (d-type). In the impedance plot the impedance at lower frequency is dominated by the effective capacitance, near the resonance it is dominated by the effective series resistance and in the higher frequency region it is dominated by the effective

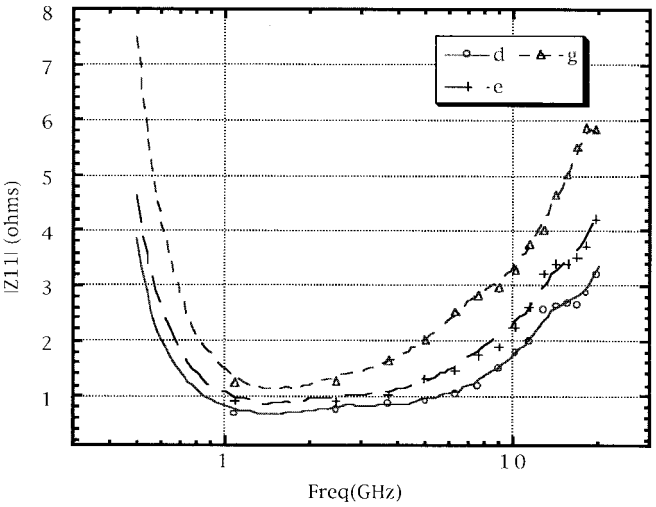


Fig. 13. Measured input impedance of capacitor structures with varying via diameters (d-, e-, and g-type).

series inductance. The thinner capacitor structure has lower impedance over a broad spectrum and thus indicating higher capacitance and lower self-inductance associated with such a structure. To further improve the impedance characteristics of these structures the series resistance should be reduced by using thicker Cu electrodes. The same data (for capacitors c and d-type) is shown on the Smith chart in Fig. 12(b).

The data given in Table VI indicate that the grid-type capacitors have better performance (lower impedance over a broad frequency range) over the array-type. Thus the grid-type capacitor should be used over the array-type for decoupling purpose. The self-inductance of the structures in the table were found to lie below 5 pH. This was computed using the measured capacitance values and the frequency at which the phase change in measured $S12$ parameter occured.

Fig. 13 compares the measured input impedance for grid-type capacitors (d, e, and g-type) with varying via diameter in the top electrode. This figure indicates that the effective series resistance and self-inductance increase with the increase in via diameter, and the capacitance decrease with the increase in via

diameter. Higher attenuation of through signal, see $S12$ values in Table VI, is achieved with decreases in via size. Thus, in order to achieve good decoupling efficiency, smallest vias allowed by processing and design (capacitive discontinuity on transmission lines through the vias) should be used. Further improvement in the decoupling capacitor is achieved through the use of thin high dielectric constant material.

The above measurements were made at the diagonal points of the capacitor structures. Further decrease in the input impedance over a broad frequency range (lower R_s and self-inductance) will be attained when the capacitor structures are probed in the middle and also if probed simultaneously at multiple points on the capacitor plane [19]. The capacitor structures in this paper allows for probing at many places and at multiple points simultaneously and thus the effective impedance as seen by the chip can easily be controlled.

VI. Conclusion

A new technique of integrating decoupling capacitors near the chip is introduced with a reworkability scheme and minimum delay on the signal lines. Based on modeling using the SIA Roadmap, it has been estimated that 13–72 nF/cm^2 of decoupling capacitance is required to satisfy the handheld and cost-performance application needs in the next decade. The limitations imposed in integrating decoupling capacitors near the chip for MCM-L based technology has led to making of composite materials in thin film form (<5 μm) and using photodefinable polymers. In this study, dielectric constant as high as 65 and a specific capacitance of 22 nF/cm^2 (satisfying handheld application need) with a loss tangent of 0.032 at 100 KHz has been achieved. Major advantages of using composite materials in integrated capacitors are:

1) compatibility with polymer or laminate based MCM technology;
2) ease of coating over a large area substrate using compatible tools;
3) allows for ease of tailoring of dielectric constant values which is useful in the design of a good decoupling capacitor.

For the test vehicle, filled polymer material (PD-PI) cured at 225 °C (consistent with MCM-L requirements) with dielectric constant of 32 and loss tangent of 0.01 was used. Low input impedance was achieved, as required for decoupling capacitors, into the GHz range for different structures using thin high dielectric constant composite layer. The solid capacitor structure provides the lowest impedance and this increases upon the increase in via diameters in the top electrode.

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