

Silicon-Embedded Toroidal Inductors with Magnetic Cores: Design Methodology and Experimental Validation

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Abstract—An approach to the ultimate integration and miniaturization of MEMS-based 3-D magnetic components involves embedding the volume of the magnetic structures within the volume of the silicon wafer itself, exploiting microfabricated windings to create current paths, and utilizing embedded magnetic cores within the limited footprint of these components to boost the magnetic performance. However, this embedding approach imposes volumetric and microfabrication constraints that require an unusual magnetic component optimization methodology compared to wire-wound inductors and PCB inductors. These constraints dictate embedded toroidal inductors with non-overlapping windings and thin magnetic cores, and impose additional limitations on inductor design parameters such as pattern resolution, the number of winding turns and winding thickness; these constraints complicate the trade-offs to be made in designing core-integrated inductors. A design methodology encompassing these constraints is therefore needed. For a targeted inductance value within a given footprint, our design methodology addresses an inductor with a maximized quality factor based on the trade-offs between copper loss and core loss. To illustrate this methodology, silicon-embedded inductors with iron powder cores are designed and fabricated; a quality factor of 24 is achieved at 30 MHz.

I. INTRODUCTION

The miniaturization and integration of power electronics on a single silicon chip to form a so-called ‘power chip’ [1] exploits high-frequency switched-mode power conversion circuitry, together with integrated inductors, to create ultra-compact energy conversion systems. The increase in the switching frequency reduces the required value of inductance and therefore the inductor volume in these systems, rendering the integration of microfabricated inductors with these chips possible. Inductance requirements vary depending on circuit topologies and power/voltage levels; however, in general, they fall into the range of hundreds of nanohenries for power converter circuits that switch at frequencies of 10 MHz to 100 MHz [2-3].

For microfabricated air-core inductors, the realization of hundreds of nanohenries of inductance within a limited volume is often infeasible due to microfabrication constraints. Even when feasible, such inductance values are usually achieved at the expense of the DC resistance of the inductor due to the large number of turns employed and also their current handling capability. To address this problem, soft magnetic material can be employed as a magnetic core to enhance the inductance. Monolithic fabrication processes for integrating inductors with various magnetic materials have been reported [4-6]. However, there is a lack of systematic methods in guiding the core integration process and understanding the performance optimization of these devices.

In 2012, Han et al., reported a design procedure for integrating low-permeability ferrite cores into printed circuit board (PCB) coils for high-frequency power applications [7]. Extrapolating this procedure directly to the microfabrication regime, however, poses challenges due to the presence of different constraints. Embedding toroidal inductors into silicon [8], which has been proposed for the ultimate miniaturization of on-chip power conversion systems, imposes volumetric and microfabrication constraints that require an unusual optimization methodology compared to wire-wound inductors and PCB inductors. These constraints dictate embedded inductors with non-overlapping windings and thin magnetic cores, and impose additional limitations on inductor design parameters such as pattern resolutions, the number of windings and copper thickness; these constraints complicate the trade-offs to be made in designing core-integrated inductors.

In this paper, a methodology for designing silicon-embedded inductors with magnetic cores as well as validation of the methodology by fabrication and experimental characterization is presented. Since many magnetic materials become extremely lossy in the megahertz regime, core-associated losses must be understood and appropriate

magnetic materials suitable for the target frequency must be selected. The resistive losses originated from the microfabricated inductor windings are also non-negligible; therefore, an optimization between core loss and copper loss is needed to achieve the best inductor performance.

II. CORE INTEGRATION PROCESS

Before discussing the inductor design methodology, the microfabrication technique that is used to implement the core-integrated silicon-embedded inductor is first presented. The inductor windings are fabricated based on a 3-D shadow-mask approach as reported in [8], and the core integration is achieved by dropping in appropriately-shaped core materials at the midpoint of the winding fabrication process. Since the magnetic cores are prepared separately from the winding fabrication process, the drop-in approach allows the use of various well-developed magnetic materials, including those that might require fabrication steps incompatible with CMOS processes.

Fig. 1 illustrates the fabrication process of the core-integrated inductor. A partially-completed inductor with lower and vertical windings fabricated within a silicon trench is first prepared as shown in step (a) using a 3-D shadow-mask approach [8]. In parallel, in step (b), a toroidal magnetic core with appropriate magnetic properties and thickness is identified. The commercial magnetic cores, as employed in this paper, are typically thicker (millimeter scale) than the silicon wafer (hundreds of micrometers), and so should be

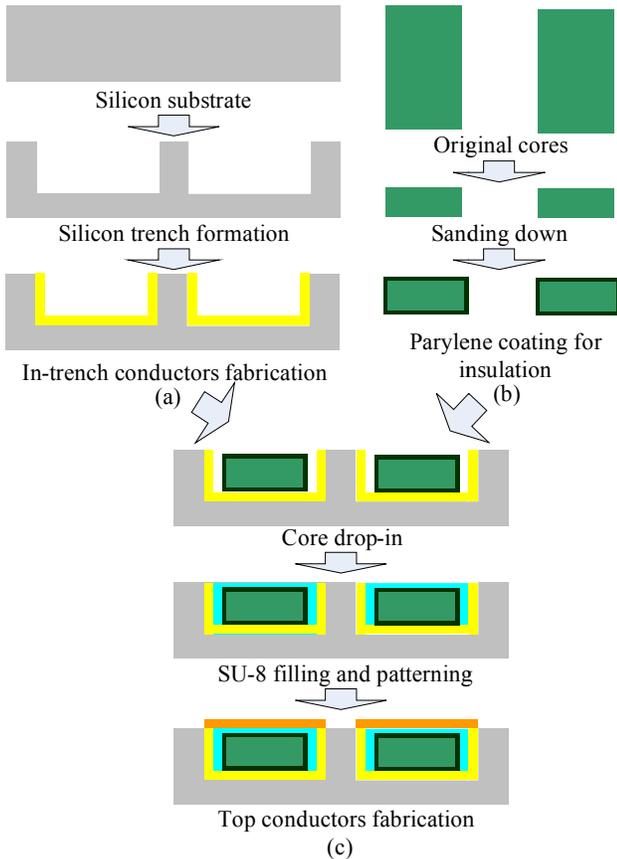


Figure 1. Fabrication process of silicon-embedded inductors with dropped-in magnetic cores.



Figure 2. An iron powder core from Micrometals®: before (left) and after (right) lapping. The core thickness is 1.78mm before lapping and 200 -250 μm after lapping. The inner diameter of these cores is 2.24 mm, and the outer diameter is 5.08mm.

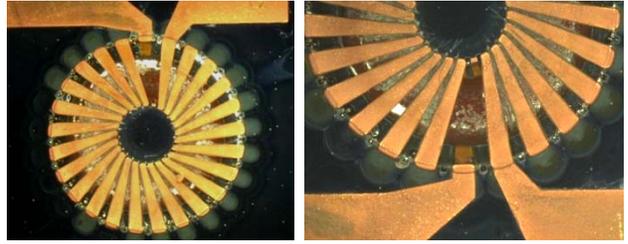


Figure 3. A fabricated silicon-embedded toroidal inductor with an integrated magnetic core. The inner diameter of the inductor is 2 mm and the outer diameter is 6 mm. The inductor height is in the range of 250-300 μm and the total thickness of the core is approximately 200-250 μm . The copper thickness is 30 μm .

thinned prior to integration, which is achieved by lapping. A photomicrograph of the magnetic core before and after lapping is shown in Fig. 2. Upon completion of the lapping, a 5- μm -thick parylene layer is deposited onto the core to ensure electrical insulation between the inductor windings and the core. This insulation layer may not be necessary if the selected magnetic core has high resistivity, and it may need to be thickened when low-resistivity metallic cores are employed. After the magnetic core is insulated, it is dropped into the partially-completed inductor as shown in step (c). Solid SU-8 epoxy pieces are then melted at 130 $^{\circ}\text{C}$ to fill in the trench; lapping of SU-8 is conducted to achieve planarization and crosslinking follows to secure the core. Fabrication of the top conductors then completes the device [8]. Photomicrographs of a fabricated inductor with an integrated magnetic core are shown in Fig. 3.

III. INDUCTOR DESIGN METHODOLOGY

Designing the optimal silicon-embedded inductors with magnetic cores requires careful consideration of the microfabrication and volumetric constraints:

- The achievable copper thickness for the embedded inductor windings is often limited by fabrication technology such as lithography processes and metal deposition processes, which leads to a non-negligible winding resistance, which is less frequently a concern in PCB inductors and wire-wound inductors.
- On-chip integration and silicon embedding of the toroidal inductors puts volumetric constraints on the device footprint and height. The inductor should

neither occupy an area larger than the chip, nor possess a height exceeding the thickness of a silicon substrate.

- Due to the intrinsic complexity of 3-D toroidal structures, only single-layer non-overlapping windings are employed in microfabrication. A limited footprint and patterning resolution therefore implies that only a limited number of turns can be fabricated, imposing a limit on the maximum inductance that can be achieved. In addition, a tradeoff between the inductance and resistance needs to be considered since squeezing more turns into the inductor results in increased resistive loss that may eventually affect the power conversion efficiency.
- Integrating magnetic cores into the inductor introduces additional core losses that originate from the magnetic material itself, as well as the coupling between the magnetic core and the silicon substrate. Without careful design and optimization, unacceptable core losses could overwhelm the gain of inductance enhancement.

For a targeted inductance value and given footprint area, our design methodology addresses a magnetic-core inductor realized using microfabrication techniques with a maximized quality factor, based on these equations,

$$L_{core} = L_{air} \cdot \mu_r \cdot \frac{t_{core}}{h}, \quad (1)$$

$$L_{air} = \frac{\mu_0 N^2 h}{2\pi} \ln\left(\frac{d_o}{d_i}\right), \quad (2)$$

$$Q_{core} = \frac{\omega L_{core}}{R_{Cu} + R_{core}}, \quad (3)$$

where L_{core} is the overall inductance of the magnetic-core inductor, L_{air} is the inductance of the corresponding air-core inductor, μ_r is the relative permeability of the magnetic material, t_{core} is the thickness of the core, h is the height of the inductor (the ratio $\frac{t_{core}}{h}$ represents the fraction of the inductor volume comprised of magnetic material given the assumption that the core has the same lateral dimension as the inductor), N is the number of turns, d_o and d_i are the outer and inner diameter of the toroidal inductor respectively, Q_{core} is the quality factor of the magnetic-core inductor, R_{Cu} denotes the copper losses in the inductor windings including both DC and AC losses, and R_{core} denotes the losses in the magnetic core at the frequency of interest.

Given the targeted inductance value (L_{core}), the relative permeability of the magnetic material (μ_r), the inductor outer and inner diameter (d_o , d_i), and the fraction of the inductor volume to be occupied by the magnetic material ($\frac{t_{core}}{h}$), the required number of turns in the core-integrated inductor (N) can be calculated from (1). The achievable quality factor can therefore be estimated using (2) providing that the copper loss in the copper windings (R_{Cu}) and the loss in the magnetic core (R_{core}) are understood for the calculated number of turns at the frequency of interest. To optimize for best device

performance, the key is to understand the trade-offs between the copper loss and core loss and therefore determine the core volume to be integrated and the number of turns to be fabricated in the inductor. The optimization space can be divided into three regimes.

- Regime 1: If $R_{Cu} \gg R_{core}$, which is often the case for microfabricated inductors with limited copper thickness working at low frequencies, or with low-permeability magnetic materials, the design strategy should be to maximize the core volume in the integrated inductor and minimize the number of turns to reduce the copper loss.
- Regime 2: If $R_{Cu} \ll R_{core}$, which is often the case for core-integrated inductors at high frequencies, or with high-permeability magnetic materials, the core thickness should be reduced with the number of turns increased (to maintain the same inductance) until a minimum total loss is obtained or core saturation limit is reached. In the cases of having extremely lossy magnetic material, changing the material or removing it to obtain an air-core design could be favorable alternatives.
- Regime 3: If R_{Cu} is comparable to R_{core} , an optimization should be obtained for a turn number and a core thickness that enables $R_{Cu} + R_{core}$ to be a minimum.

To estimate the copper losses R_{Cu} in the windings, finite element modeling (FEM), analytical models, or experimental characterization of a fabricated inductor with the desired number of turns can be conducted at the frequency of interest. Core losses in the magnetic materials vary significantly depending on the materials and frequencies. For commercial magnetic cores, volumetric power loss versus frequency is usually provided in the material technical information. If not, impedance characterization of the cores with wound wires (negligible resistive loss) can be performed under the desired excitation condition to obtain R_{core} . To eliminate the possible electric-coupling-induced losses and minimize the complexity of the design process, only magnetic cores with reasonably high resistivities are considered in this paper.

IV. METHODOLOGY VERIFICATION

As an example to demonstrate the methodology, silicon-embedded inductors integrating iron powder cores are designed for two different inductances as shown in Table I. Material mix -2 and -6 from Micrometals® [9] are selected due to their stable performance for frequencies up to 100 MHz. These materials have permeability in the range of 8.5-10 and are specially designed to have low losses for operation at tens of megahertz. Since the copper loss is related to the number of turns in the inductor and the core loss can be affected both by the number of turns and the thickness, the inductor design procedure is actually an iterative process following our design methodology. First, assuming the core loss is negligible compared to the copper loss at 10 MHz, following the strategy discussed in Regime 1, a maximized core thickness of 250 μm is selected and the number of turns is calculated using (1), as shown in Table I. Second, estimations of the copper loss and

core loss at the calculated number of turns are performed and the results are shown in Fig. 4. In this paper, the copper losses are obtained from measurements of fabricated air-core inductors with the desired number of turns. The core losses are obtained from measurements of wire-wound inductors with the desired thickness and number of turns. As can be seen from Fig. 4 and summarized in Table I for the frequency of 10 MHz, the copper loss is approximately 0.4 Ω for Design I and 0.8 Ω for Design II while the core loss is approximately 0.07-0.08 Ω for Design I and 0.24-0.32 Ω for Design II, depending on the materials to be integrated. This verifies our assumption and validates our choice of maximizing the core thickness. Therefore an optimized design has been achieved. The quality factor can then be estimated using (2) based on the inductance and the loss information, which is also shown in Table I. If the core losses are estimated to be larger than the copper losses at the calculated number of turns, the core thickness should be reduced and the losses should be re-estimated based on the re-estimated number of turns. This process should be iterated

until an optimization point is reached, as discussed in Regime 2 and 3.

To verify the design results, silicon-embedded inductors with integrated iron powder cores are fabricated and the characterization results are shown in Fig. 5, with the key information also summarized in Table I. For design I, since the integrated iron powder cores have a nonmagnetic factory-coated passivation layer of approximately 100 μm in thickness and their lateral dimension is approximately 30% smaller than the inductor lateral dimension, the resulting effective core thickness in the fabricated inductors is only 150 μm , preventing the inductor from achieving the optimized design results. However, they do show results consistent with the design methodology considering the fabrication constraints. For Design II, the fabricated devices match well with the optimized design results. The device integrating material -2 demonstrated an inductance of 620 nH and a quality factor of 37 at 10 MHz. In conclusion, the methodology is shown to guide the inductor design procedure well.

TABLE I. OPTIMIZED INDUCTOR DESIGNS AND FABRICATION RESULTS

	Design I		Design II	
	Case 1	Case 2	Case 1	Case 2
Optimization results				
Targeted inductance (nH)	300	300	600	600
Inductor height (μm)	300	300	300	300
Inductor outer diameter (mm)	6	6	8	8
Inductor inner diameter (mm)	2	2	3.6	3.6
Core material	-2	-6	-2	-6
Core permeability	10	8.5	10	8.5
Desired core thickness (μm)	250	250	250	250
Estimated turn No.	23	25	39	42
Estimated Cu loss (Ω) @10MHz	0.4	0.4	0.8	0.8
Estimated core loss (Ω) @10MHz	0.08	0.07	0.32	0.24
Estimated Q @10MHz	39	40	34	36
Fabrication results				
Integrated core thickness (μm)	150	150	250	230
Fabricated turn No.	25	25	40	40
Calculated inductance (nH)	188	159	607	475
Estimated Q @10MHz	17	15	34	29
Measured inductance (nH)	167	140	620	470
Measured total loss (Ω) @10MHz	0.58	0.75	1.1	1.5
Measured Q @10MHz	17.5	12	37	19

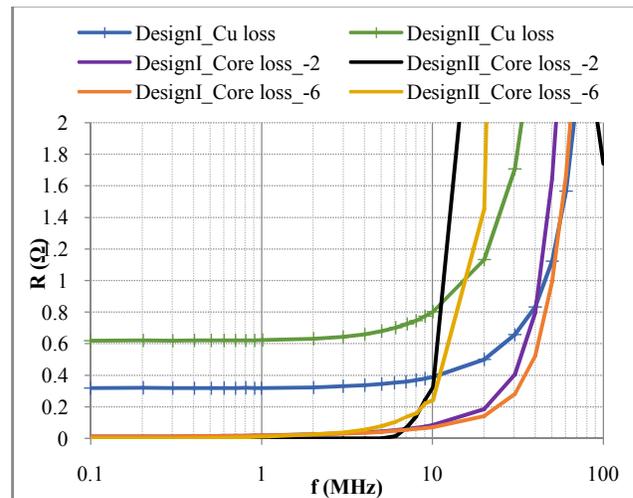
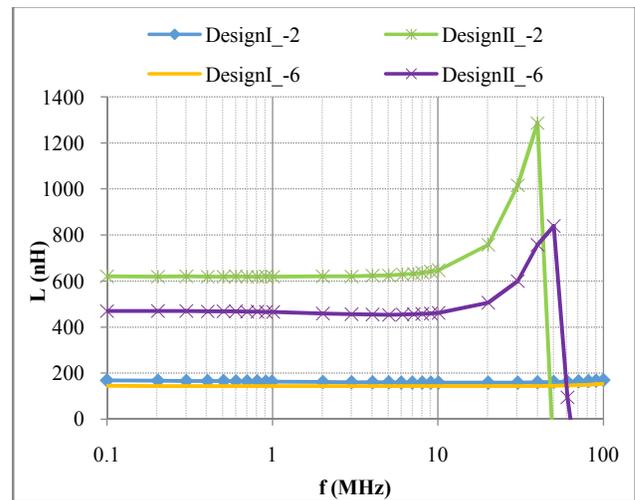
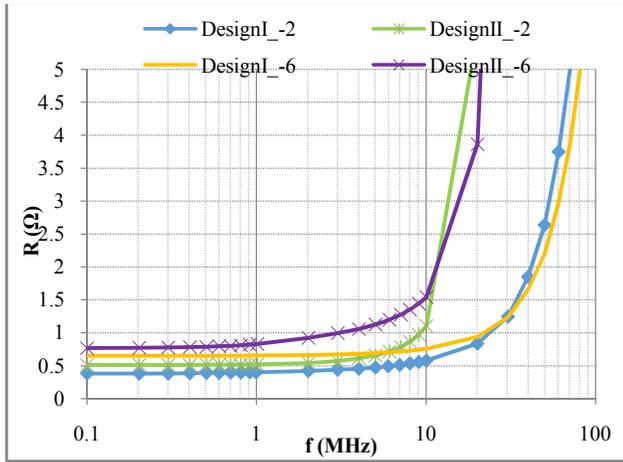


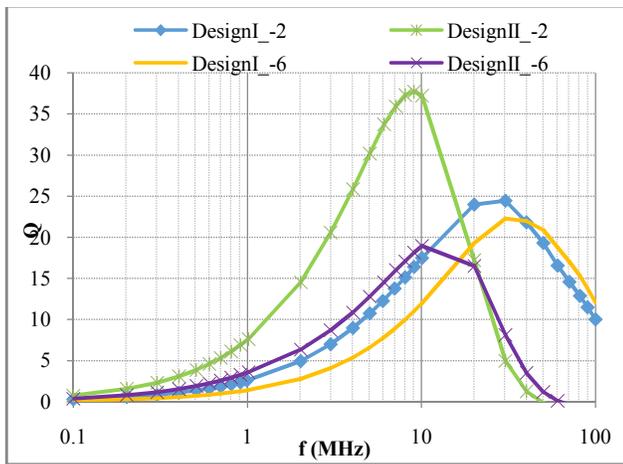
Figure 4. Measured copper loss in the microfabricated windings and core loss in the magnetic core under low voltage excitation condition.



(a)



(b)



(c)

Figure 5. Measured inductance (a), resistance (b), and quality factor (c) of the silicon-embedded core-integrated inductors.

V. CONCLUSION

An inductor design methodology for optimizing silicon-embedded core-integrated inductors is presented. By understanding the loss characteristics, the magnetic volume to be integrated and the inductor geometric design can be optimized. The methodology is validated by exploiting a drop-in approach to integrate commercial magnetic cores into the silicon-embedded toroidal inductors.

REFERENCES

- [1] M. Araghchini, C. R. Sullivan, etc., "A technology overview of the PowerChip development program," *IEEE Trans. Power Electronics*, vol. 28, pp. 4182-4201, 2013.
- [2] S. C. O. Mathuna, T. O'Donnell, N. Wang, and K. Rinne, "Magnetics on silicon: an enabling technology for power supply on chip," *IEEE Trans. Power Electronics*, vol. 20, pp. 585-592, 2005.
- [3] J. Hannon, R. Foley, J. Griffiths, D. O'Sullivan, K.G. McCarthy, and M.G. Egan, "A 20 MHz 200-500 mA monolithic buck converter for RF applications," *24th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 503-508.
- [4] D.V. Harburg, X. Yu, F. Herrault, C.G. Levey, M.G. Allen, and C.R. Sullivan, "Micro-fabricated thin-film inductors for on-chip power conversion," *7th Intl. Con. on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1-6.
- [5] D.W.Lee, K. Hwang, and S. X. Wang, "Design and fabrication of integrated solenoid inductors with magnetic cores," *ECTC2008*, pp. 701-705.
- [6] X. Fang, R. Wu, L. Peng, and J.K.O. Sin, "A novel silicon-embedded toroidal power inductor with magnetic core," *IEEE Electron Device Letters*, vol. 34, pp. 292-294, 2013.
- [7] Y. Han, and D. J. Perreault, "Inductor design methods with low-permeability RF core materials," *IEEE Trans. Industry Applications*, vol. 48, pp. 1616-1627, 2012.
- [8] X. Yu, M. Kim, F. Herrault, J. Kim, C-H. Ji, and M.G. Allen, "Silicon-embedding approaches to 3-D toroidal inductor fabrication," *J. Microelectromech. Sys.*, pp. 1-9, 2013.
- [9] Micrometals, "<http://www.micrometals.com/>".