High Density Electroplating Bonding Interconnect Technology: Chip Packaging and High Aspect Ratio Passive Elements

Yeun-Ho Joung and Mark G. Allen
School of Electrical and Computer Engineering, Georgia Institute of Technology
791 Atlantic Drive, Atlanta, GA 30332, USA
Phone: (404) 894-9909; Fax: (404) 894-5028; E-mail: gt7432d@mail.gatech.edu

Abstract

Electroplating bonding technology for the fabrication of micro-electro-mechanical (MEMS) structures as well as interlayer bonding structures in the gap between two substrates is described in this paper. Electroplating bonding is a fabrication approach in which two conductors on differing substrates are electrically and mechanically joined by an additional growing layer of electrodeposited conductive material. Chip-scale interconnects fabricated with 256 150um tall, micromachined copper (Cu) posts on glass and printed wiring board (PWB) substrates were bonded using electroplating bonding technology. A simple electrical continuity test on a row of 16 interconnects yields resistances of 0.097 ohm per test bed, where the values agree well with calculated electrical resistances of 0.092ohm per test bed. A simulation of the thermal properties of the electroplating bonded chip interconnects was done using ANSYS 5.6, with particular attention paid to stresses arising from mismatched coefficient of thermal expansion (CTE) of the substrates. The simulation results indicate that the adhesion layer between the structure and the substrate exhibit stresses when a 100°C temperature rise was applied. The stress comparison was performed by observing the integrity of the adhesion relative to the presence or absence of polymer passivation on the interconnect pads. Simulations were confirmed with experiment by thermal testing over the range –55 ~ 125°C. After the thermal test, the electrical properties of the test bed were again measured with the same result as the aforementioned electrical resistance data.

Using the electroplating bonding method, high performance MEMS solenoid inductors were fabricated. These inductors were fabricated using an epoxy-core method that greatly reduces fabrication time while maintaining performance. The electroplating bonded inductors were fabricated with 3, 5, 7 and 10 turns. The inductors are 500um high with 50 um width and with a 100um gap between posts. The effective inductances were 6.1nH, 10.5nH, 15.0nH and 24.4nH, and the corresponding Q-factors were 82.1, 59.6, 53.2, and 43.3, respectively, depending on the number of turns, as extracted using an equivalent electrical circuit model.

Introduction

Modern microelectronics technology has sought ever thinner, smaller, higher density, and lighter chip systems [1-4], and packaging is a key component to the ultimate commercial success of these systems. Flip chip technology has received much attention in the chip packaging world due to its good performance in terms of electrical characteristics, compactness in its design scheme, and its high I/O density [5]. Flip chip technology has been challenged by issues related to lead (Pb)-based solder bumps, the cost of polymer interposers, and reliability. Regulations have been established to slowly eliminate Pb from electronic devices [6]. Pb can be replaced by Pb-free solder bumps such as Sn-Ag-Cu (SAC) in chip packaging [6-7]. However, several considerations still need to be satisfied such as thermal reliability, interposer cost, and multi-layer under bump metal (UBM).

Wafer Level Packaging (WLP) of microelectronic circuitry, in which critical package elements are formed on the silicon wafer prior to dicing, has several advantages over conventional packaging techniques, such as one-step testability of multiple chips on a silicon wafer prior to dicing, and the possibility of high input-output (I/O) density. In the case of Flexible WLP, surface micromachined flexible interconnects can remove the interposer in the packaging and thermal reliability can be improved by free movement of the interconnects [8-11]. Further, WLP wafers can be bonded to substrates in a non-solder based method known as *electroplating bonding*, in which two conductors on differing substrates are electrically and mechanically joined by an additional growing layer of electrodeposited conductive material.

Three electroplating bonding applications for WLP are examined in this paper. First, electroplating bonded chip interconnects are demonstrated as a potential solder bump replacement. Second, flexible WLP structures are formed by surface micromachining techniques and bonded using electroplating bonding technology. The flexibility of the interconnects and the robustness of the bonding part may allow removal of the interposer which can help address thermal mismatch that exists in conventional packaging bumping method. Third, micromachined solenoid inductors were fabricated in the interconnect layer between the chip and board. The interconnect layer, which has been an unused area in the conventional chip packaging concept, can be utilized for the fabrication of passive elements, thereby reducing the real estate consumed in conventional Si chip or board fabrication while simultaneously minimizing the parasitic effects often associated with off-chip passive elements.

Electroplating Bonding

Electroplating bonding is an extension of the electroplating technique for the purpose of making connections or contacts between two microstructures.The connections, built using this electroplating bonding process, can be applied to create interconnections in chip packaging. Figure 1 shows a schematic of the electroplating bonding procedure. Two substrates bearing metallic structures to be connected are brought together as in the flip-chip method. When this combination is then submerged in a plating solution and an electric potential is applied to the substrates, an electroplated metal layer grows between the two separate structures on the two separate substrates, thus bonding them and forming a connection. A variety of metallic-electroplating solutions are available for electroplating bonding, including Cu, Au, Ni, Ni/Fe, and a variety of other metals.

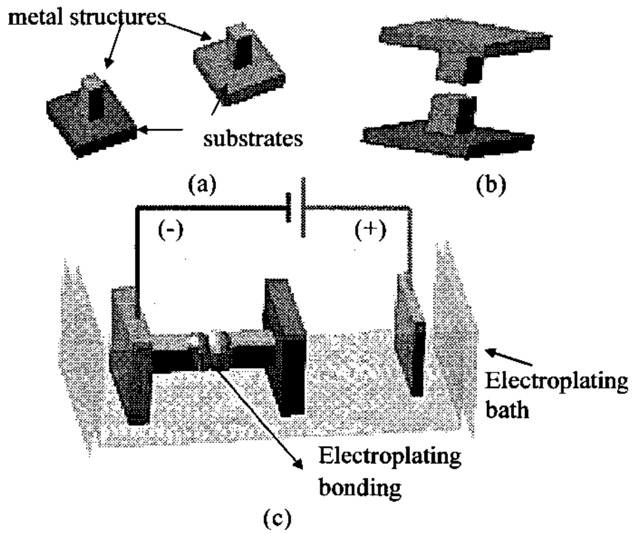


Figure 1. Schematic of electroplating bonding procedure. (a) surface micromachined metal structures (b) structure alignment (c) electroplating bonding in electroplating bath.

As shown in Figure 1, the electroplating bonding structures can be formed by three simple steps. First, the metal structures on each substrate are formed by surface micromachining and conventional microelectronics electroplating techniques. Usually, electroplated metal structures are fabricated from copper because of already well-developed processes for its electrodeposition as well as its good electrical and mechanical characteristics. Second, the metal structures on a substrate are flipped and aligned. The aligning method can be the same as for flip chip technology; however, in this paper, the alignment was performed manually under a stereoscope for simplicity. Third, the entire system was clamped together, immersed in the electroplating bath, and the tips of the metal structures are bonded with applied DC current and subsequent electrodeposition.

Chip Interconnects with Electroplating Bonding

Design and fabrication

In conventional chip-scale packages, interconnects are usually formed by lead or lead-free solder bumps. The solder bumps and solder bump adhesion metal layer (UBM) is the part most susceptible to thermal stress effects when heat is applied to the system [1, 6-7]. The failure of reliability usually occurs in the ductile solder bump or on the interface of the UBM and solder bump due to the different coefficient of thermal expansion of the two substrates (Si wafer and PWB). As Figure 2 illustrates, the multilayer electroplating bonded structures display substantial mechanical strength. Fabricated multibond, multiturn inductor structures [12] used as mechanical test structures are resistant to breakage and act like springs in the macro-world when large tensile forces are applied.

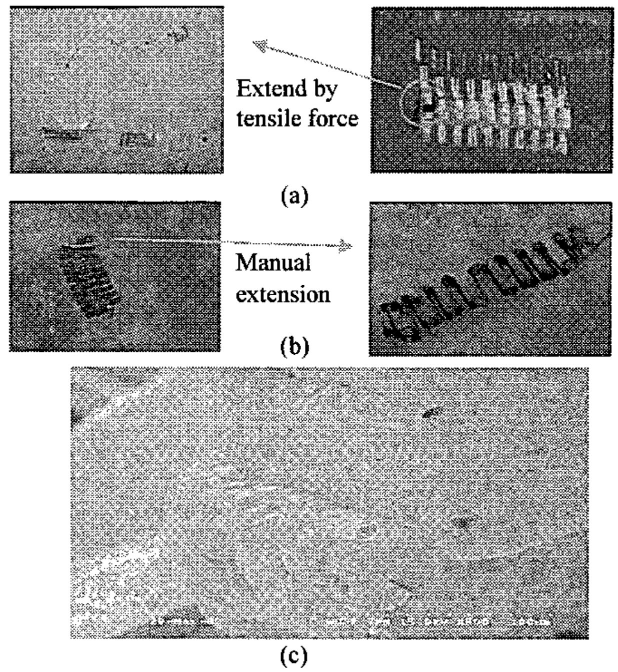


Figure 2. Pictures of electroplating bonded structures undergoing simple mechanical test. (a) easy approach extension test of an electroplating bonded 10 turn inductor. (b) inductor structure acting like spring (c) SEM picture of electroplating bonded part of inductor post.

Also Figure 2 (c) shows an SEM picture of the electroplating bonding part of the structure. The electroplating bonding technology applies for the transformation of two Cu posts on separate substrates into a single, robust Cu bonded structure. With the positive mechanical properties of the electroplating bonding structures confirmed, a chip interconnect test structure (glass to printed wiring board (PWB)) was designed and fabricated. In the design step, thermal reliability testing and the seed layer adhesion property were considered. The electrical test lines on PWB were embedded within epoxy polymer to ensure good adhesion. On the glass substrate, the test lines were not encapsulated by any polymer so as to be able to make a comparison of the passivation effect of the polymer during the thermal test. The schematic of the electroplating chip packaging is shown in Figure 3. In this initial work, glass was utilized instead of silicon chips, but the design and fabrication using Si would remain unchanged. The primary goal of the design is to obtain Cu chip-interconnects in the gap between the two substrates (glass and PCB) using the electroplating bonding packaging interconnection method.

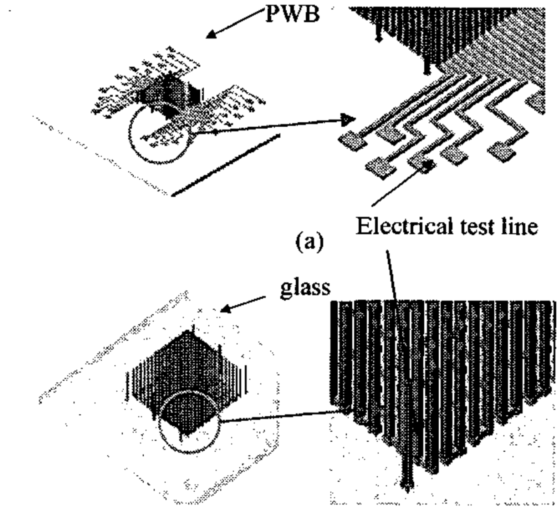
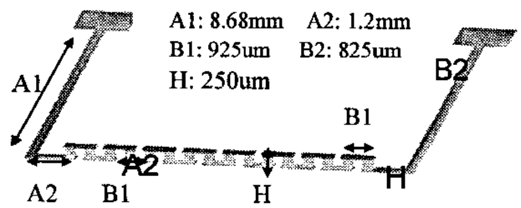


Figure 3. Schematic of electroplating bonding chip interconnects (a) on PWB and (b) on glass substrates.

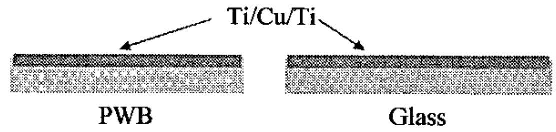


Areas of A1,A2,B1 and B2 : 25umX250um
Area of H: 250umX250um

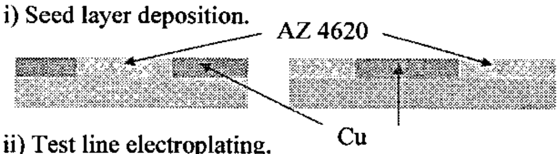
Figure 4. Schematic of the test line.

The two substrates to be connected were a 2.5x2.5 cm^2 glass substrate (as an initial test) and a 5x5cm^2 epoxy-glass composite printed wiring board (PWB). The calculated resistance of a Cu electroplated test row was 0.092[ohm].

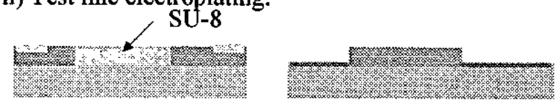
The electroplating bonding chip packaging used photosensitive epoxy (SU8-25, Microchem, Inc,), AZ 4620, a standard Cu–electroplating technique, and the Cu electroplating bonding method. The fabrication process is based on a CMOS-compatible plating-through-mold technology, followed by standard surface micromachining, and is described in Figure 5. A seed layer of Ti/Cu/Ti (30 nm /250 nm /30 nm) is deposited as described in Figure 5 (i). On this layer, an electroplating mold 25 μm in thickness is formed using AZ4620 postive photosensitive polymer and patterned using a conventional CMOS photolithography process. The mold is then filled to the top using a Cu electroplating bath as shown in Figure 5 (ii). When the mold is filled with electroplated Cu, a layer (25 μm) of epoxy is spin-cast on the bottom sustrate and patterned to create the mold for the polymer passivation as shown in Figure 5 (iii).



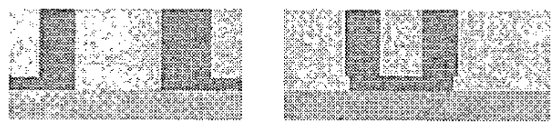
i) Seed layer deposition.



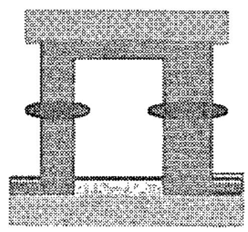
ii) Test line electroplating.



iii) AZ 4620 removal. SU-8 passivation and seed layer etching on bottom substrate.



iv) Seed layer deposition on bottom substrate. SU-8 mold and Cu electroplating.

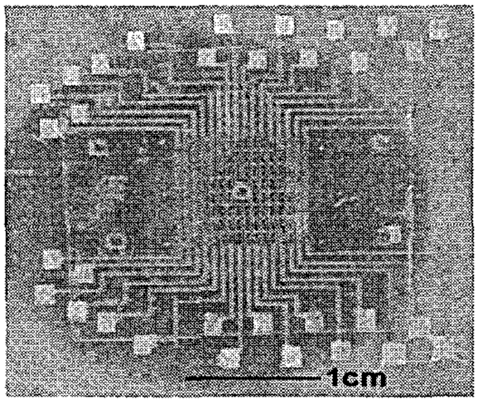


v) SU-8 etching, structure alignment and electroplating bonding.

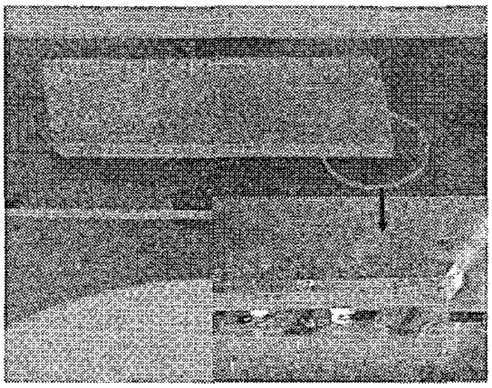
Figure 5. Fabrication process schematic of electroplating bonded chip interconnects.

For the next via formation and electroplating, a Ti/Cu/Ti seed layer is sputtered on the polymer passivation layer. A thick layer (150 μm) of epoxy is spin-cast on both substrates and patterned to create the mold for the via. This via mold is then filled with electroplated Cu. Figure 5 (iv) shows the electroplated Cu via which is 150um in height. After the formation of the electroplated Cu structures, the polymers are etched away as shown in Figure 5 (v). The flipping of the substrate - which is the same method as the conventional flip chip method - and aligning of the posts on each substrate, are performed as shown in Figure 5(v). Finally, electroplating bonding is done using a Cu electroplating bath.

Figure 6 shows a photomicrograph of the fabricated electroplating bonding chip interconnect.



(a)



(b)

Figure 6. Photomicrograph of fabricated electroplating bonding chip interconnect. (a) top view (b) side view.

Result and discussion

Electrical continuity of the chip interconnects was tested using the 4-probe method. Measurement was executed with 2 testbeds. Each testbed had 16 test rows. 14 test rows of testbed A had good electrical continuity and testbed B had 13 good test rows. The average electrical resistance of the chip interconnect testbed showed 0.097ohm/test bed. The values agree well with the calculated electrical resistances of 0.092ohm/testbed.

As shown in Figure 7, the thermal property of the chip interconnects was calculated using the finite element method (FEM) program ANSYS 5.6, with particular attention paid to stresses arising from mismatched coefficient of thermal expansion (CTE). The simulation result showed that the interface of the adhesion layer between the interconnects and the seed layer had large stresses due to CTE mismatch in the Si (2.62 ppm/°C) and the PWB (20 ppm/°C) [11]. The simulation was performed using a 100°C temperature differential. An actual thermal test was also performed in a thermal chamber with a cycle range of –55 ~ 125°C with a 5 minute dwell at –55°C and 125°C and a 1 minute transition time. The thermal test was cycled 100 times using the thermal chamber setup. After the thermal test, the electrical properties of the test bed were again measured with the same result as the aforementioned electrical resistance data. Figure 8 shows the system after the reliability test. In the figure, many non-embedded seed layers on the glass substrate were detached from the substrate.

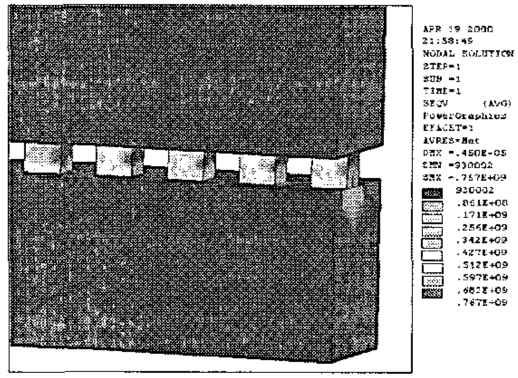


Figure 7. FEM simulation of chip interconnects.

Figure 8 shows that the glass had fissures due to thermal shock. However, the polymer-passivated electrical test lines were not detached from the substrate. It shows that the passivation layers after the back-end processing provide sufficient durability to the adhesion layer to compensate for the thermal effect.

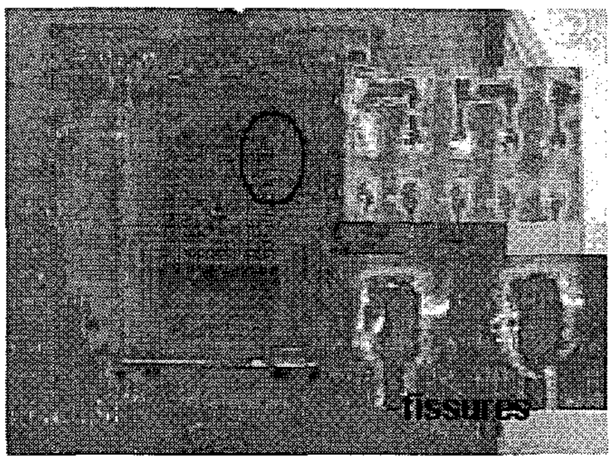


Figure 8. Chip interconnect system after thermal reliability test.

Micromachined Solenoid Inductors with Electroplating Bonding

Design and fabrication

Previously we reported that high inductance and Q-factor micro solenoid inductors were built in the chip interconnect layer using electroplating bonding [12]. In the paper, the inductor posts, which can be interconnects in the chip packaging, were fabricated based on a CMOS-compatible plating-through-mold technology and electroplating.

Traditionally, the electroplating time to form tall structures is proportional to the structure height. In fabricating tall, micro solenoid inductors, the epoxy core approach [13] was developed to reduce the electroplating time. In this approach, the cores of the metal lines are made from nonconducting epoxy to aid in fabrication; due to the skin effect at high frequencies, no deleterious effect on quality factor or other electrical performance of devices fabricated in this fashion is observed as long as the metal coating the epoxy cores is at least a few skin depths in thickness. As an example of the fabrication simplification, a many-hour electrodeposition to create a 250um-tall structure using conventional plating-through-mold technology is reduced to tens of minutes using the epoxy-core method. Using this method, 500um-tall electroplating bonded inductor structures were fabricated to obtain high inductance and Q-factor calculated from equation (1).

$$L = \frac{N^2 \mu w_c h_c}{l_c} \qquad (1)$$

where N is the number of coil turns , μ is the permeability of the core, w_c is the width of core with, h_c is the core height, and l_c is the core length. The schematics of the inductors are shown in Figure 9.

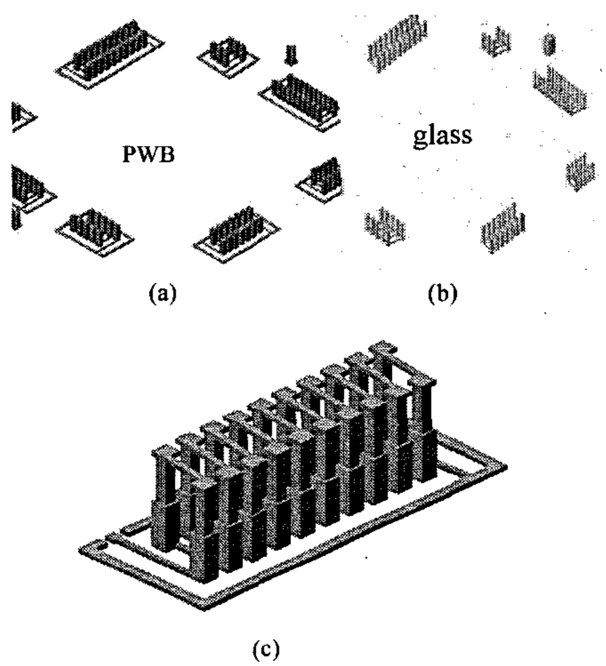


Figure 9. Schematic of micro solenoid inductor. (a) bottom and (b) upper Cu structure before electroplating bonding. (c) electroplating bonding of epoxy-core, micro solenoid inductor.

Two pairs of 3, 5, 7 and 10 turn inductors (equivalent to 100 posts) were designed with a 100um gap between the posts on the perimeter of 1x1cm^2 substrates. For measurement consideration, one-port inductors were designed. The configuration of the inductors is summarized in Table 1.

Table 1. Configuration of micro solenoid inductor

Post number	100
Via height	250um each
Pitch of turns	250um
Conductor width	50um
Conductor thickness	20um
Measurement method	1 port
Gap of posts	100um
Flux area	400 x 500 um^2

Fabrication began by preparing a 5x5cm^2 PWB and 2x2cm^2 glass substrate. For measurement purposes, a 2um Al sacrificial layer was deposited on the glass substrate with a Ti adhesion layer. The fabrication process of the epoxy core interconnect layer is shown in Figure 10.

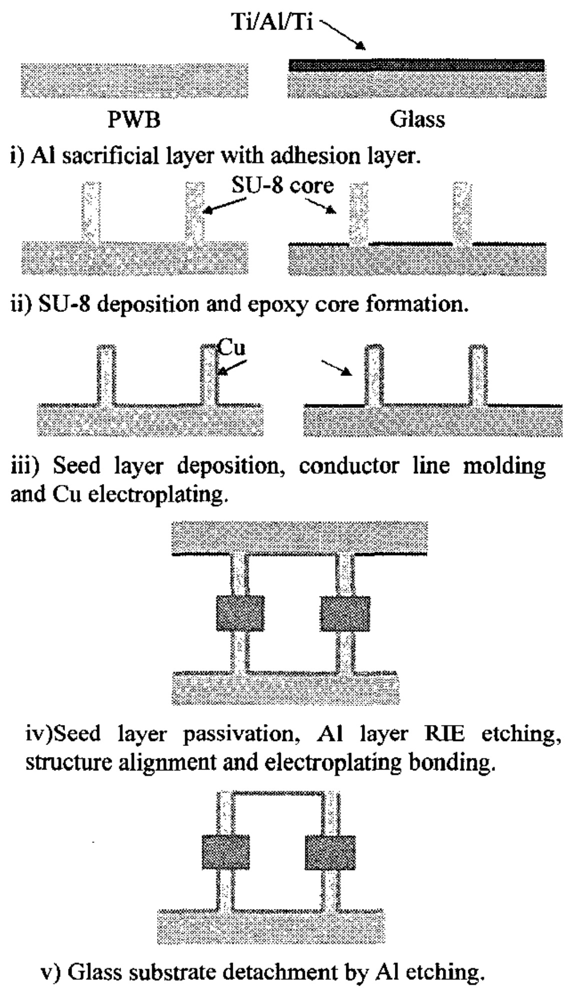


Figure 10. Process schematic of the electroplating bonding epoxy-core inductors.

To make a 250um epoxy core post, SU-8 was spun and exposed as in Figure 10 (ii). A Ti/Cu/Ti seed layer was deposited for the electroplating. Futurrex negative photoresist (NR9-800) was then coated and photolithographically patterned for the Cu line molding. The Cu line was then electroplated as described in Figure 10(iii). An Al sacrificial layer was then patterned with RIE to aid in the visibility during aligning. The planar portions of the seed layer on the PWB were covered to prevent the deposition of copper on the PWB surface during the electroplating of the posts. The structures on both substrates were manually aligned, then clamped together and electroplating bonded as shown in Figure 10(iv). After the bonding process, to facilitate the measurement process, the glass substrate was detached by removing the Al sacrificial layer and the Ti adhesion layer by wet etching as shown in Figure 10(v). The electroplating bonding time was 30 minutes. SEM figures for 3, 5 and 7 turn inductors that were fabricated in the interconnect layer are shown in Figure 11. The profile of the electroplated bonds on the interconnects are also shown in Figure 11(d).

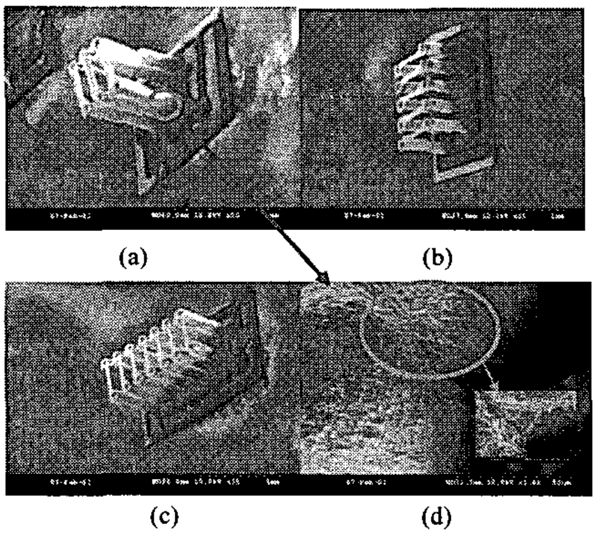


Figure 11. SEM micrographs of micro solenoid epoxy-core inductor in interconnect layer. (a) 3 turn, (b) 5 turn and (c) 7 turn inductor. (d) SEM of the electroplated bonds formed in the copper.

Result

The characteristics of the interconnect layer inductors were measured and analyzed. The measurements were performed using an HP 8510 network analyzer. The S-parameters, which were extracted from the network analyzer, were converted to Q-factor and effective inductance (L_{eff}) using the software package HP ADS. The probe tip itself was calibrated to within 0.1 dB to ensure a more precise measurement prior to regular port calibration. The value was analyzed with a one-port inductor equivalent circuit in Figure 12.

The model consists of an ideal inductor L in series with a resistor R to account for the conductor loss. The dielectric loss

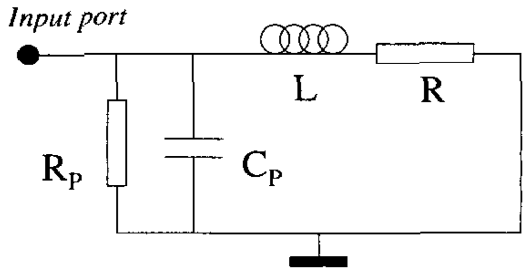


Figure 12. One-port inductor electrical model used for the performance optimization.

and the parasitic capacitance are represented by R_P and C_P, respectively. C_P results from the substrate capacitance and coupling capacitance between turns. Figure 13 shows measured and modeled effective inductances (L_{eff}) and the Q of the 3, 5, 7 and 10 turn inductors, while Table 2 summarizes the performance of the inductors. The extracted lumped element values for the inductors are shown in Table 3.

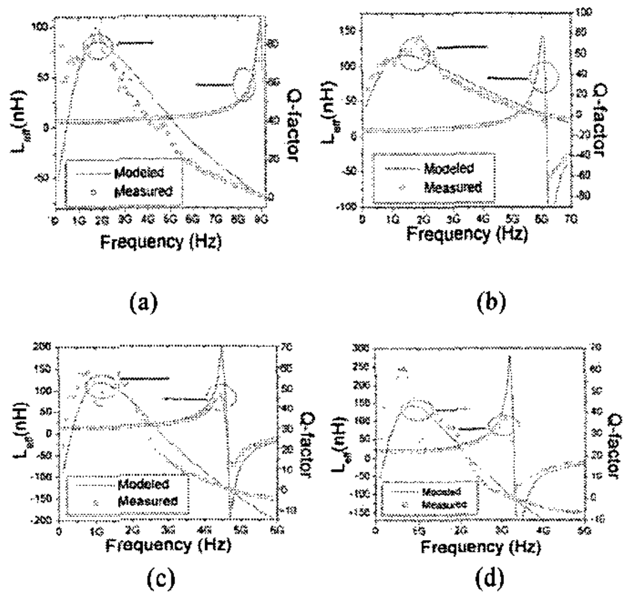


Figure 13. Measured and modeled L_{eff} and Q of the inductors. From upper (a)3 turn, (b)5 turn, (c) 7turn and (d)10 turn inductor.

Table 2. Inductor performance.

No. of turns	L_{eff} (nH)	Q_{MAX}	SRF(GHz)
3	6.1	82.1@1.8GHz	9.15
5	10.5	59.6@1.4GHz	6.15
7	15.1	53.2@1.1GHz	4.62
10	24.4	43.3@0.8GHz	3.25

Table 3. Summary of extracted circuit parameters.

No. of turns	L (nH)	R (Ω)	C_P (fF)	R_P (kΩ)
3	5.9	0.43	52	12.7
5	10.0	0.8	67	12.9
7	14.2	1.0	84	13
10	22.9	1.5	102	13.2

Conclusions

Cu electroplating bonded chip interconnects, and high Q-factor, epoxy-core micro solenoid inductors, were designed and fabricated in the chip interconnect layer. The electroplating bonding technology was found to form an excellent bond between copper posts on two separate substrates. Moreover, electroplating bonding technology is compatible with conventional CMOS processing and electroplating technology. Electroplating bonded chip interconnects have shown promise in addressing the conventional solder bump thermal weakness issue as well as the issues related to the use of lead based solder bumps. A simple electrical continuity test on a row of 16 interconnects yields resistances of 0.097 ohm/test bed, where the values agree well with calculated electrical resistances predicted frm bulk copper of 0.092ohm per/test bed. Thermal reliability tests were performed in a thermal chamber with a cycling range of –55 ~ 125°C with a 5 minute dwell at –55°C and 125°C and a 1 minute transition time. The test results showed that electroplating bonded Cu interconnects have a robust bonding structure and the adhesion of the seed layer with polymer back-end processing maintains good adhesion after the thermal tests. High Q and inductance micro solenoid inductors with epoxy cores have also been realized in the chip interconnect layer with the electroplating bonding technology. The inductors were fabricated using the epoxy core method to reduce the plating time for tall structures. Characteristics of the inductors were measured with an HP 8510 network analyzer and the results were compared to simulation values of the equivalent circuit model using HP ADS. Large magnetic flux, which is produced by tall interconnects, makes possible high inductances and Q-factors. The inductors were designed with different number of turns: 3, 5, 7, and 10. The effective inductances were 6.1nH, 10.5nH, 15.0nH and 24.46nH, and the corresponding Q-factors were 82.1, 59.6, 53.2, and 43.3, respectively, depending on the number of turns.

Acknowledgments

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