characteristics in a wide variety of "band-gap engineered" devices.

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Alignable Epitaxial Liftoff of GaAs Materials with Selective Deposition Using Polyimide Diaphragms

C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen

Abstract—**In this letter we report the selective and alignable deposition of patterned thin-film epitaxial GaAs/GaAlAs devices onto a host substrate such as silicon for low cost, manufacturable hybrid integrated optoelectronic circuits. We use a thin polyimide diaphragm as the transparent transfer medium for these patterned epitaxial devices. Each of these devices or a group of these devices on the polyimide is then optically aligned and selectively deposited onto the host substrate. Using this technique, a light emitting diode 50 × 50 μm in area and 2 μm thick was grown on a GaAs substrate, lifted off, aligned and selectively deposited onto a silicon host substrate, and electrically contacted and tested. Using this method, the sparse distribution of costly photonic devices or the deposition of aligned arrays of devices to fabricate larger arrays without large area growth of photonic devices can be achieved on a variety of smooth host substrates.**

INTRODUCTION

THE monolithic integration of gallium arsenide (GaAs) photonic and electronic materials and devices with host substrates, such as silicon (Si), glass, and polymers, will enable the fabrication of the next generation of optoelectronic integrated circuits (OEIC's). These OEIC's are currently costly and complicated to fabricate in comparison to silicon integrated circuits. If conventional microelectronic processing techniques could be used in the fabrication of such OEIC's, their cost would be reduced and their manufacture would become more attractive to industry. In this letter, we discuss an improved method for the alignment, selective deposition, and interconnection of thin-film epitaxial GaAs devices onto host substrates such as Si.

A standard technique for GaAs on Si integration is heteroepitaxial growth [1]. However, the crystal quality of this material is often insufficient for many optical applications. One integration method which seeks to preserve the high material quality of lattice-matched growth is the epitaxial liftoff (ELO) process as described by Bellcore [2]. A thin aluminum arsenide (AlAs) sacrificial layer is grown on a GaAs substrate, and GaAs device epilayers are grown on top of this AlAs layer. The GaAs lattice matched epilayers are separated from the growth substrate by selectively etching the AlAs sacrificial layer. These device layers are then mounted in a hybrid fashion onto a variety of substrates. This ELO material is very high quality [2] and is currently being used for the integration of GaAs materials onto host substrates such as Si, glass, lithium niobate, and polymers [2]–[5].

Although the Bellcore technique yields high quality material, it has several problems, including the inability to align

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The authors are with the School of Electrical Engineering, Microelectronics Research Center, Georgia Institute of Technology, Atlanta, GA 30332.

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and selectively deposit the devices and difficulties in contacting both sides of the patterned device. In this letter, we report a modified ELO technique which enables the alignment and selective deposition of the device or array of devices onto a host substrate, and also allows the devices to be processed on both the top and bottom of the epitaxial sample while under substrate support.

Process Description

As described above, ELO proceeds by growing epitaxial device layers on a sacrificial layer and selectively etching the sacrificial layer, releasing the epitaxial layers from the substrate. The Bellcore technique for GaAs ELO and deposition uses Apiezon W, which is optically opaque, to support the layer during and after the liftoff process. The ELO epilayer is then attached to the host substrate through Van der Waals (VDW) bonding or through adhesion layers between the host and the ELO epilayer. Since the Apiezon W is opaque, the final alignment with respect to the host substrate is performed by post etching the ELO material.

The fundamental problems with this process which need to be addressed include: 1) the ELO samples are not alignable with the host substrate prior to deposition; 2) most of the expensive GaAs material is wasted through post deposition etching; 3) double-sided processing of ELO material while the material is not under substrate support is difficult due to the strain caused by deposited layers [6]. We have addressed these issues through the modifications of the ELO technique which are described below.

In the Georgia Tech ELO technique, the device layers [Fig. 1(a)] are first defined on the growth substrate using mesa etch processing [Fig. 1(b)]. The mesa etch uses a photoresist mask and is performed using H_2SO_4:H_2O_2:H_2O (1:8:160) as a fast gross etch with a final selective etch of NH_4OH:H_2O_2 (1:200) which stops at the AlAs layer. Processing steps such as contact definition can also occur on these mesa defined devices either before or after the mesa etch [Fig. 1(c)]. These devices are then coated with Apiezon W [Fig. 1(d)] and are exposed to a standard HF:H_2O (1:10) etch solution to separate the epitaxial devices from the growth substrate [Fig. 1(e)]. High Al-composition layers can be included in the ELO devices since these layers are protected from the ELO etch solution [7]. The array of mesa defined epitaxial devices is embedded in the surface of the Apiezon W carrier, which is approximately 100 μm thick and can be easily handled. At this point it is not possible to align these ELO devices with respect to features on a host substrate since the Apiezon W is opaque. We have also demonstrated ELO directly with polyimide instead of Apiezon W [8].

To overcome this difficulty, the ELO devices are VDW bonded to a transparent polyimide diaphragm which serves as an alignment and selective deposition transport for the ELO devices [Fig. 1(f)]. The polyimide diaphragm is fabricated using standard micromachining techniques. Silicon wafers are coated with approximately 4 μm of polyimide, which is spin-cast from a commercially available polyamic acid solution (DuPont PI-2611), baked at 150°C in air for 30 min, and cured at 400°C in nitrogen for 1 h. The central portion of the wafer is then etched from the backside using a single sided etching technique [9] and 6:1:1 HF:HNO_3:H_2O as the etchant to form a polyimide diaphragm approximately 4 μm thick and ranging from 3 to 25 mm in diameter, supported by a silicon "ring" at its perimeter. The diaphragm fabricated in this manner is transparent, taut, and mechanically tough, and is thus ideal as a carrier for the liftoff layers. A low-power oxygen plasma etch is performed on the polyimide surface immediately prior to deposition of the GaAs layers to enhance the adhesion of the ELO devices to diaphragm. The ELO devices on the Apiezon W carrier are then brought into contact with the polyimide, and through VDW bonding, the ELO devices are attached to the polyimide [Fig. 1(f)]. The Apiezon W is dissolved with trichloroethylene, leaving the ELO devices bonded to the top of the polyimide. Note that the preliftoff processing (for example, contacts) applied to these devices now lies on the top of the ELO devices supported by the polyimide diaphragm. The devices can now be aligned through the transparent diaphragm and selectively deposited to the host substrate (e.g., a circuit-containing silicon substrate) in a cleanroom, as shown in Fig. 1(g).

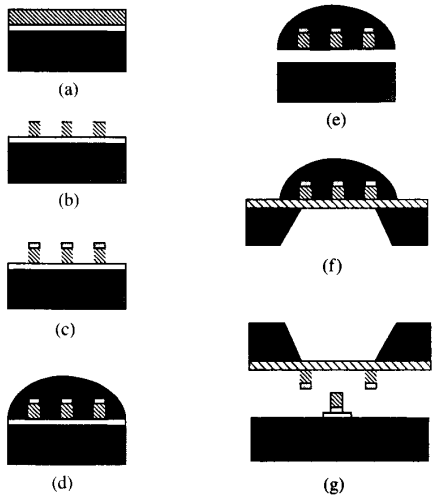

Fig. 1. Georgia Tech epitaxial liftoff process. (a) Starting substrate with grown layers; (b) after mesa etching; (c) after contacting; (d) after Apiezon W application; (e) after selective etch; (f) after adhesion to silicon supported polyimide diaphragm and removal of Apiezon W; (g) after selective deposition onto host substrate. Individual devices or the entire array can be aligned and deposited onto host substrates.

Results

Fig. 2 shows a pair of photomicrographs of six AlGaAs/GaAs/GaAlAs double heterostructure devices mounted on a polyimide transfer diaphragm, both (a) in a top view with top illumination and (b) in a top view with illumination through the transparent diaphragm. This transparent diaphragm enables the user to align the ELO devices with respect to the host substrate prior to deposition. After deposition, the uncontacted side of the ELO devices faces up, and conventional photolithographic and processing techniques can be used to apply contacts to this side of the devices. This process

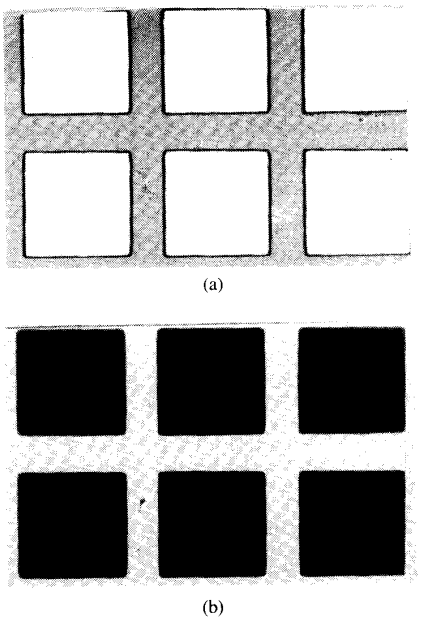

Fig. 2. AlGaAs/GaAs/AlGaAs 100 × 100 × 2 μm thick epitaxial liftoff material supported on a 4 μm thick polyimide diaphragm. (a) Top illumination of the devices on top of the diaphragm; (b) backside illumination through the diaphragm.

sequence is important, as we have noted some difficulty with processing steps such as contact deposition if these thin ELO samples are not supported by a substrate during deposition.

Since the ELO devices are on the order of 2–3 μm thick, the surface profile of the devices on the host substrate is nearly monolithic, and conventional processing techniques can be used to electrically connect the devices to the host substrate. Fig. 3 shows a photomicrograph of a GaAs/GaAlAs light emitting diode (LED) structure grown with a 50 nm AlAs sacrificial etch layer which has been mesa etched, preprocessed, lifted off, transferred, deposited onto Si and post processed using the Georgia Tech ELO technique. This LED structure was grown p-side up on a GaAs substrate and patterned into mesas [Fig. 1(b)]. The patterned devices are square, 100 μm on a side, and 2.5 μm thick. A broad area ohmic contact of AuZn was deposited while the ELO sample was still on the growth substrate [Fig. 1(c)]. After liftoff and adhesion to the polyimide diaphragm, the devices were adhered to a Si-host substrate which had previously been coated with 150 nm of Au.

A conventional mask aligner was used to position and VDW bond the Au/Zn contacted p-side of the device to the Si/Au host substrate. The diaphragm containing the GaAs ELO material was placed in the mask holder and the host substrate into the substrate holder of the mask aligner. A droplet of water was placed upon the host substrate for VDW bonding. The ELO device was aligned with respect to the host substrate using the mask aligner. The GaAs and the host substrate were brought into contact using the mask aligner as if for contact lithography. Uniform pressure was applied across the GaAs device(s) to be deposited using a probe. Current alignment accuracy is within 2 μm.

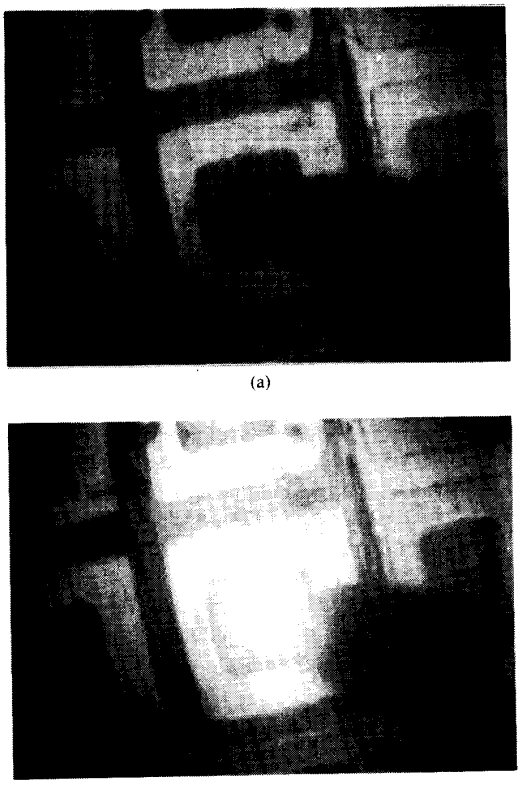

Fig. 3. An epitaxial liftoff LED which has been selectively deposited from the polyimide diaphragm onto a Si-host substrate. Both top and bottom ohmic contacts have been applied to the device. The top contact to the LED has been post processed after deposition of the liftoff device onto the Si-host substrate. (a) Under no bias; (b) under forward bias. Infrared radiation is emitted from the device under forward bias.

The n-type material, now available on the top of the device, then had an ohmic contact of AuGe/Ni/Au (50/10/70 nm) deposited onto it, and a 50 × 50 μm window was opened in the contact using liftoff photolithography. The contact was rapid thermal annealed, which also bonded the AuZn contact to the Au on the Si host substrate for enhanced adhesion of the ELO device to the host substrate. Although the bond strength has not been quantitatively measured, annealed metal contact bonding generally exhibits greater adhesion than VDW bonding [10]. Fig. 3(b) shows this device emitting infrared light under forward bias, illustrating the successful liftoff, transfer, and electrical contacting of this device. Since the device is inverted from the grown structure to facilitate double-sided processing, a performance comparison of the device before and after ELO was not performed, although the ELO material should maintain the high quality demonstrated in other ELO processes [2].

Since arrays of devices can be fabricated on one small piece of GaAs material, frugal use of expensive GaAs material and devices can be accomplished by selective deposition of devices or arrays of devices from the polyimide diaphragm. For example, if one laser is needed on each of 1000 silicon IC's to form an OEIC, then only one array of

1000 lasers (i.e., one small area growth) is necessary to produce the number of lasers needed for all of the Si-integrated circuit requirements. The entire array of 1000 lasers can be located on one polyimide transfer diaphragm, and each laser can be aligned with respect to the Si-host substrate and selectively deposited from this diaphragm onto the Si. This will decrease the cost of manufacturing OEIC's since the expensive GaAs devices will only be deposited where needed, and wafer-scale growths can be avoided.

Conclusion

A modified epitaxial liftoff process which utilizes a transparent polyimide diaphragm has been developed to realize the alignable, selective deposition of epitaxial GaAs liftoff material onto host substrates such as Si, glass, and polymers. This transparent diaphragm can be used to align and selectively deposit the GaAs ELO devices as individual devices from the array or as an entire array onto the host substrate. The use of the polyimide transfer diaphragm also allows both the bottom and the top of the device to be processed while under substrate support. With the alignment and selective deposition capabilities inherent in this process, the frugal use of photonic materials is possible, heralding inexpensive, manufacturable OEIC's.

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Wavelength Discriminating Optical Switch

M. Selim Ünlü, *Student Member, IEEE*, S. Strite, *Student Member, IEEE*, A. Salvador, A. L. Demirel, *Student Member, IEEE*, and H. Morkoç, *Fellow, IEEE*

Abstract—**A novel wavelength discriminating bistable optical switch (WDOS) with completely optical input-output capabilities is presented. The WDOS is a three-terminal AlGaAs/GaAs N-p-n-p structure with an InGaAs/GaAs quantum well light emitting diode at the n-p junction. The WDOS can be switched to stable ON and OFF conditions by optical excitations at different wavelengths which allows the use of a single optical window. The optical switching threshold can be adjusted by the external bias. Depending on the external bias, the WDOS functions as an optical inverter, an electrically programmable optical AND/OR gate, or an all-optical read-write memory element.**

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The authors are with Coordinated Science and Materials Research Laboratories, Urbana, IL 61801.

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Introduction

RECENTLY, interests in new device technologies for digital optoelectronic circuits has been mounting. Optical switches will be necessary elements for optical signal processing and digital communication systems. Most of these optoelectronic switches are two terminal p-n-p-n devices similar to the Shockley diode. Several theoretical analyses of p-n-p-n devices have been carried out [1]-[3]. Two terminal switches with optical input and electrical output based on bipolar inversion channel field-effect transistors in the AlGaAs/GaAs [4] and SiGe/Si [5] material systems were demonstrated. An optical inverter consisting of an heterojunction phototransistor (HPT) laterally integrated with an N-p-n-p light emitting diode (LED) has also been realized [6]. We have described the characteristics of an heterojunc-